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*****
*
*          OPTICAL ISOLATOR          *
*
*          FOR THE HYTEC 1330 PC-TO-  *
*
*          CAMAC INTERFACE and CRATE  *
*          CONTROLLER                 *
*
*          TECHNICAL MANUAL           *
*
*          and CIRCUIT DESCRIPTION    *
*
*****
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HYTEC ELECTRONICS LTD  
5 CRADOCK ROAD, READING, RG2 0JT, U.K.

Doc: UM1330ISOL  
Issue: A  
Date: 16/10/00  
Author: PJM

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## 1. Introduction

The 1330 Isolator is a special board produced to provide 2kV isolation in the cable which normally connects the 1330 ISA personality card to the 1330 CAMAC Controller. It performs two main functions: the optical isolation of the signals in both directions and the control of the timing and strobe signals, which require manipulation due to the characteristics of the optical isolators used and the length of the cables on each side, which are longer than normal.

Before the isolator can be used, both the 1330 and the personality card need to be modified. Firstly, this is to provide 5-volt power to either side of the isolator: normally only the ground power signal is connected to the cable. Secondly, on the 1330, terminating resistor packs are changed to match the optoisolator outputs and some signal timing components are taken out of circuit.

## 2. 1330 Modifications

Locate RN1, RN2, RN3 and RN4, which are on sockets on the front card of the left-hand side of the unit. Remove all four networks, which are normally 1K x 13 DIL resistor packs. Now fit two 470R x 13 networks in locations RN1 and RN3.

Remove R1 and C1 on the left-hand front card and fit a piece of Kynar wire between IC pins 5 and 12. This reduces the delay on the incoming Data Strobe (/DS) signal.

Now locate the 34-way connector at the front of the left-hand card and wire VCC to pins 12, 16 and 26 on this 34-way connector. This provides 5-volt power to this side of the isolator.

## 3. Personality Card Modifications

Using a scalpel, disconnect pins 12 and 16 of the 34-way IDC header from Ground. Now, using Kynar wire, link pins 12, 16 and 26 together. Modify the card bracket to allow a small right-angle connected toggle switch to be fitted in the PCB, protruding just above the 34-way connector. Drill three holes 1.5mm diameter in the PCB to accommodate this switch. Wire one side of the switch to VCC on the board and the other side to pins 12, 16 and 26 on the 34-way connector. You have now placed a switched VCC signal onto three wires in the cable, as required by the 1330 isolator.

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#### 4. Functional Description

Looking at the circuit diagram, we see that the isolator has two sides, A and B. The signals on each side are distinguished by A and B in the signal names. The main signals to look for are as follows:

##### A-Side:

VCCA	VCC A-side
GNDA	GND A-side
R/WA	Read/write A-side
EA	Enable A-side
/STARTA	Start (cycle in progress) A-side
/INTRA	Interrupt A-side
/DSA	Device Select A-side
/INITA	Initialise A-side
DB0-7A	Data Bus 0-7 A-side
A0-5A	Address (crate and register select) A-side

A similar set of signals is found for the B-side.

The circuitry consists basically of optical isolation for all these signals, plus some special control and timing circuitry in the bottom left-hand corner of the circuit diagram, comprising IC6, a GAL16V8, and IC2, a dual monostable timing pulse generator. The PAL, IC6, produces a number of signals:

/GOA	An enable signal for the data buffer which sends data to the personality card (IC12).
/GOB	An enable signal for the data buffer which sends data to the 1330 (IC10).
/STARTA	A BUSY signal, sent to the personality card to delay the end of a read or write cycle.
/DSI	The internal DEVICE SELECT signal which is then isolated and goes to the 1330 as /DSB. The timing of this signal is controlled by the PAL.
RWOUT	Read/Write signal to the 1330.
CLOCK	An output derived from other signals, to clock logic in the PAL.
TRIG1 and TRIG2	are outputs to trigger the two halves of the dual monostable IC2. These provide timing pulses as inputs to the PAL, Q1 and Q2.

The rest of the circuit diagram mostly comprises decouplers for either side of the isolating logic and pull-up resistors for the inputs and outputs of the opto-isolators.

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5. Parts List

Part	Type	Outline
IC1	HCPL2630,HCPL2630	DIL8
IC2	74123,LS123	DIL16
IC3	HCPL2630,HCPL2630	DIL8
IC4	HCPL2630,HCPL2630	DIL8
IC5	HCPL2630,HCPL2630	DIL8
IC6	GAL16V8,GAL16V8	DIL20
IC7	HCPL2630,HCPL2630	DIL8
IC8	HCPL2630,HCPL2630	DIL8
IC9	HCPL2630,HCPL2630	DIL8
IC10	74245,LS245	DIL20
IC11	HCPL2630,HCPL2630	DIL8
IC12	74245,LS245	DIL20
IC13	HCPL2630,HCPL2630	DIL8
IC14	HCPL2630,HCPL2630	DIL8
IC15	HCPL2630,HCPL2630	DIL8
IC16	HCPL2630,HCPL2630	DIL8
IC17	HCPL2630,HCPL2630	DIL8
IC18	HCPL2630,HCPL2630	DIL8
IC19	HCPL2630,HCPL2630	DIL8
R1	RES-VERT,470	SIL2
R2	RES-VERT,470	SIL2
R3	RES-VERT,470	SIL2
R4	RES-VERT,4K7	SIL2
R5	RES-VERT,470	SIL2
R6	RES-VERT,470	SIL2
R7	RES-VERT,4K7	SIL2
R8	RES-VERT,470	SIL2
R9	RES-VERT,470	SIL2
R10	RES-VERT,470	SIL2
R11	RES-VERT,470	SIL2
R12	RES-VERT,470	SIL2
R13	RES-VERT,470	SIL2
R14	RES-VERT,470	SIL2
R15	RES-VERT,470	SIL2
R16	RES-VERT,470	SIL2
R17	RES-VERT,470	SIL2
R18	RES-VERT,470	SIL2
R19	RES-VERT,470	SIL2
R20	RES-VERT,470	SIL2
R21	RES-VERT,470	SIL2
R22	RES-VERT,470	SIL2
R23	RES-VERT,470	SIL2
R24	RES-VERT,470	SIL2
R25	RES-VERT,470	SIL2
R26	RES-VERT,470	SIL2
R27	RES-VERT,470	SIL2
R28	RES-VERT,470	SIL2

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Parts List, continued.

R29	RES-VERT, 470	SIL2
R30	RES-VERT, 470	SIL2
R31	RES-VERT, 470	SIL2
R32	RES-VERT, 470	SIL2
R33	RES-VERT, 470R	SIL2
R34	RES-VERT, 470R	SIL2
C1	CAPR2W2, 100N	CAPR2W2
C2	CAPR2W2, 100PF	CAPR2W2
C3	CAPR2W2, 100N	CAPR2W2
C4	CAPR2W2, 22PF	CAPR2W2
C5	CAPR2W2, 100N	CAPR2W2
C6	CAPR2W2, 100N	CAPR2W2
C7	CAPR2W2, 100N	CAPR2W2
C8	CAPR2W2, 100N	CAPR2W2
C9	CAPR2W2, 100N	CAPR2W2
C10	CAPR2W2, 100N	CAPR2W2
C11	CAPR2W2, 100N	CAPR2W2
C12	CAPR2W2, 100N	CAPR2W2
C13	CAPR2W2, 100N	CAPR2W2
C14	CAPR2W2, 100N	CAPR2W2
C15	CAPR2W2, 100N	CAPR2W2
C16	CAPR2W2, 100N	CAPR2W2
C17	CAPR2W2, 100N	CAPR2W2
C18	CAPR2D4E, 10uF/16V	CAPR2D4E
C19	CAPR2D4E, 10uF/16V	CAPR2D4E
J1	IDC34VL, IDC34VL	IDC34VL
J2	IDC34VL, IDC34VL	IDC34VL
TP1	TESTPIN	SIL1
TP2	TESTPIN	SIL1
TP3	TESTPIN	SIL1
RN1	RN8COM, 470R	SIL9
RN2	RN8COM, 470R	SIL9
FS1	FUSECMC	FUSECMC
FS2	FUSECMC	FUSECMC

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6. PALASM Design Description

----- Declaration Segment -----

TITLE 1330 ISOLATOR PAL  
PATTERN 1  
REVISION A  
AUTHOR P. MARSHALL  
COMPANY HYTEC ELECTRONICS LTD.  
DATE 10/16/00

CHIP \_1330iso PALCE16V8

----- PIN Declarations -----

PIN 1	ICLOCK	COMBINATORIAL ;
PIN 2	/DSA	COMBINATORIAL ;
PIN 3	R_WA	COMBINATORIAL ;
PIN 4	/ISTART	COMBINATORIAL ;
PIN 9	Q1	COMBINATORIAL ;
PIN 11	Q2	COMBINATORIAL ;
PIN 12	TRIG2	COMBINATORIAL ;
PIN 13	TRIG1	COMBINATORIAL ;
PIN 14	CLOCKOUT	COMBINATORIAL ;
PIN 15	R_WB	COMBINATORIAL ;
PIN 16	/DSB	COMBINATORIAL ;
PIN 17	/STARTA	COMBINATORIAL ;
PIN 18	/GOB	COMBINATORIAL ;
PIN 19	/GOA	COMBINATORIAL ;

;

----- Boolean Equation Segment -----

EQUATIONS  
GOA.TRST = VCC  
GOB.TRST = VCC  
STARTA.TRST = VCC  
DSB.TRST = VCC  
R\_WB.TRST = VCC  
CLOCKOUT.TRST = VCC  
TRIG1.TRST = VCC  
TRIG2.TRST = VCC

;Q1 is 100nS wide, triggered by TRIG1  
;Q2 is 250nS wide, triggered by TRIG2  
;DSA should be at least 650nS wide

TRIG1 = DSA ;Trigger first monostable immediately  
TRIG2 = /Q1 ;Trigger second monostable when first ends  
CLOCKOUT = DSB + (CLOCKOUT \* DSA) ;Flag to say we have started  
DSB = (/R\_WA \* DSA \* Q2) + (R\_WA \* DSA \* /CLOCKOUT) + (DSB \* R\_WA \* DSA)  
;For a write, we generate a nice strobe pulse well away from either end  
;of the incoming DS pulse. For a read, we give it the full width pulse

R\_WB = R\_WA  
STARTA = ISTART  
GOA = DSA \* R\_WA  
GOB = DSA \* /R\_WA

DEVICE: GAL16V8; CHECKSUM: 52EE.