1330/IBM

IBM PC/AT and Compatibles

CAMAC INTERFACE and CRATE CONTROLLER

TECHNICAL MANUAL

and CIRCUIT DESCRIPTION

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1. Introduction

The 1330/IBM PC Interface Set consists of a 1330 Personal Computer CAMAC Interface module, an IBM personality card and an interconnecting cable two metres long. The 1330 supplied without the IBM Personality card can only be used with the BBC Micro directly and a suitable cable for this is also supplied.

Normally, the interface (and personality card) will be supplied set up as the "first crate" i.e.

IBM	Address - Hex 280 I/O PAGE Crate 0 R/G Mode Master Controller Interrupt Request to IR5
BBC Micro	Address FC00 (HEX), Page FC on 1MHz Bus. Crate 0, R/G Mode, Master Controller.

2. 1330 Setting Up

The unit consists of three printed circuit boards:

- Station 24 Front
- Station 24 Rear
- Station 25

Since this controller is configurable as an Auxiliary Controller (ACB) it can be placed anywhere in the crate: even so, referring to these boards by their 'Master' station numbers is convenient and unambiguous. Note that if not in Stations 24, 25 then those positions must be occupied by a suitable Master.

These boards are set up as follows: -

2.1 Station 24 Front

2.1.1 Crate Select Switch. This is a DIP Slide switch.

For single-crate applications, select Crate 0 as marked on the silk screen, that is IGNORE the markings on the switch itself!

2.1.2 Link 1

Link "a" inserted - for use with BBC Micro only -special circuit used.

Link "b" inserted - Any micro except BBC - i.e. IBM personality card.

2.1.3 Link 2

Special address decode links - not normally used - should not be fitted.

2.1.4 Link 3

Acknowledge - not fitted.

2.1.5 Private Bus Termination

Except where multiple 1330's are "daisy-chained" onto the same private bus cable, the 1330 will be the only device on this or the BBC 1MHz bus, so terminating packs RN1, 2,3,4 should be fitted. In multi-crate situations only the last crate on the bus should have the resistor packs fitted. The maximum recommended length for the bus is 20 feet.

2.1.6 Standard Configuration Stn 24 Front

For IBM PC/AT:

Link 1 Position "b" inserted
Link 2 Not fitted
Link 3 Not fitted

Crate Select Set to 0
RN1-4 Fitted

For BBC Micro:

As IBM above but Link 1 in Position "a".

2.2 Station 24 Rear

2.2.1 Dataway Pull-up Resistor Packs

These 4 packs of 13 x 560 ohm pull-up resistors per DIL socket RN1 - RN4 should be fitted if the 1330 is in stations 24 and 25. If the 1330 is an Auxiliary Controller they must be removed.

2.3 Station 25 (see Sect. 3 for access)

2.3.1 Dataway Pull-Up Resistor Packs

If the 1330 is an Auxiliary Controller i.e. not in Stations 24 and 25, then SIL Resistor Packs RP1 to RP9 should be removed, along with discrete resistors R19, R20. The Resistor Packs are 8 x 560 ohm, and R19, R20 are 120 ohms.

2.3.2 Link 1 R/G or ACL

For Normal operation, R/G Mode, leave this link OUT. For ACL Mode Insert Link 1. Note that only one device is allowed to be in ACL Mode. See Section 9 for further information on ACB configuring.

2.3.3 Switch 1 A, B, C, D

SW1 A, B, C control the top 3 bits of the Encoded LAM Register. Switch OPEN='1', CLOSED='0'.

SW1C controls bit 5
SW1B controls bit 6
SW1A controls bit 7

The purpose of these switches is to enable the Encoded LAM number to be used as a Vector for a Service Routine. Normally ALL CLOSED.

SW1D controls the Subaddress Auto Increment Feature in conjunction with SOFT LAM, (see Sect. 7.5) and appears as Bit 6 in the Status Register. Open = '1'.

2.3.4 Standard Configuration Station 25

Link 1 OUT, Pull-ups IN, SW1 A-D all Closed.

3. 1330 Maintenance Access

For access to the component side of board 25, for example to remove the pull-up resistor packs, first remove the left-hand side cover from the module, pull the two interconnecting ribbon cable sockets to Station 25 off their pin headers, then remove the securing screws from the top rail of Station 25 at front and rear. Loosen the screws securing the bottom rail of Station 25 front and rear and gently swing this board away from the rest of the unit, taking care that the sockets do not snag on the connector pins as you do this.

To reassemble, simply reverse the procedure.

Always store the resistor packs in a safe place if you do take them out, so that they can be replaced if necessary.

4. 1330 Front Panel

The 1330 Front Panel has an access hole for the 34-way private bus, 3 holes for access to the PCB-mounted Request/Grant Connectors, four LED's and a reset button.

4.1 Private-bus Connector

Bump-polarised 34-way right-angle header with ejector clips. Pin 1 is top left.

4.2 Indicator LEDs

4.2.1 Request/Grant LED - shows that R/G mode is selected by link 1 being OUT on Station 25. Will normally be on all the time.

4.2.2 Inhibit LED - shows the state of the internal inhibit flip-flop rather than the Dataway Inhibit line. Comes on after Power Up or Reset.

4.2.3 Addressed LED - flashes when the 1330 detects its own address. Stretched to 10mS.

4.2.4 Interrupt LED - comes on to show that an interrupt is being sent to the computer. This will happen if an Un-Masked LAM or FAIL is detected while Interrupts are Enabled.

4.3 Reset Button - This performs a "Power-on-Reset" on the whole module. In particular, it resets the following:

The Soft-LAM Flip-Flop
The Write-Data Latches
The Function-Code Register
The Q and X stores
The CAMAC-Cycle generator
The Interrupt-Enable Flag
The Inhibit (SET), C and Z Flip/Flops

Whilst pressed, therefore, it stops the 1330 doing anything.

5. 1330 Rear Panel

5.1 ACB Connector
This is the standard 40-way ACB connection to other controllers in the crate. It is a 40-way plug.

6. IBM Personality Card - Setting Up

Base Address - selectable by switches to one of 4 addresses in the I/O page as follows:

SW1A	SW1B	ADDRESS (HEX)
Closed	Closed	200
Open	Closed	280 (Standard)
Closed	Open	300
Open	Open	380

NOTE: THERE IS A KNOWN ADDRESS CLASH BETWEEN A PERSONALITY CARD SET TO ADDRESS 300 HEX AND ISA NETWORK CARDS AND SOUND CARDS. TO AVOID THIS, ALWAYS SET THE PERSONALITY CARD TO ADDRESS 280 HEX WHEN FITTING IT INTO ONE OF THESE COMPUTERS.

Normally, the address range is from Base Address to Base Address plus 7F HEX for up to 8 crates. However, in some computer installations, other peripheral devices do reside at the top of some pages, which restricts the area available to CAMAC to Base plus 5F locations. To cater for this, a Link is fitted on the personality card to limit the address range:

Link 2 IN....6 Crates Maximum Link 2 OUT....8 Crates
The Standard Setting is Link 2 IN.

Interrupt Request Selection, Link 1: This allows you to select any one of nine IR lines on the System Board through which to interrupt the processor. IR 10, 11, 12, 14 and 15 are only available on the AT machines. The choice of IR line is beyond the scope of this manual, except to say that the ESONE Subroutines use IR5 for interrupts.

7. Operating and Programming

7.1 IBM PC/XT/AT and Compatibles

Remove the top cover of the computer and install the personality card in a free expansion slot. If the machine is an AT or AT compatible, then some of the slots will have two edge connector sockets rather than one. These are the A/B C/D slots, which carry the full 16-bit data bus. This is not important to the operation of the personality card since it is only an 8 bit port, but the A/B C/D slots also carry extra Interrupt lines which you may wish to use.

Having chosen the expansion slot in which to fit the card, set the Base Address Switches as desired, select the Interrupt Request Link and the address range link as appropriate and fit the card, securing it with the fixing screw. If fitting seems awkward, loosen the bracket fixing screws where some latitude is available for accommodating slight mechanical differences.

Plug in the private bus cable, observing bump polarity. Before replacing the cover, check that the personality card is seated correctly.

Set the links and switches on the 1330 and install it in the crate. Fit the private bus cable observing bump polarity and connect up the Request/Grant chain (see Sect. 9). Also fit the rear 40 way ACB cable between controllers, if there is more than one.

Switch ON the computer, VDU and crate. Note that powering down the crate and 1330 will not affect the computer.

IF THE COMPUTER FAILS TO BOOT, CHECK THAT THE REQUEST/GRANT CHAIN IS INSTALLED CORRECTLY, SINCE THE 1330 MAY POWER UP WITH A CAMAC CYCLE PENDING AND IF THIS HAPPENS, THE I/O CHANNEL CHECK WILL FAIL SINCE "START" IS TRUE.

When the computer has booted up into DOS, run BASIC (or GW BASIC if it is not an IBM PC) and type in this program:

```
10   FUN=&H28A           'Function code register at base + 10
20   OUT FUN,0           'Send Function code 0, do CAMAC cycle
30   FOR I=1 TO 1000     'Delay loop
40   NEXT I
50   GOTO 20             'Do it again
```

Running this program should flash the Addressed LED, provided the base address is selected to be HEX 300 (otherwise change line 10) and the 1330 should now be doing CAMAC cycles. If you have a Dataway Test Module, you will be able to observe this happening.

If all is not well, check all your selections on the 1330 and on the personality card and try again. Also check the Request/Grant chain.

You are now ready to write your Application Program, possibly using the high-level-language-callable-subroutines or maybe using Compiled BASIC.

Remember that the registers in the 1330 are on WORD boundaries, so as to give correct operation on 16 bit machines, so their addresses are:

WRITE	Address	READ
Function Code	28A	
Station Number	288	Encoded L
Subaddress	286	Status Register
Data High Byte	284	Data High Byte
Data Middle Byte	282	Data Middle Byte
Data Low Byte	280	Data Low Byte

7.2 BBC Micro

Plug the private bus cable into the 1MHz bus connector in the base of the machine, observing bump polarity. Plug the private bus cable into the 1330 and install it in the crate, having set all its switches and links as desired, and switch on the crate, computer and monitor. Switching off the CAMAC will not affect the BBC Micro.

Key in this program under BASIC:

```
10   FUN=&FC05           'Function Code Register at base + 5
20   ?FUN=0              'Write 0 to F code reg, do CAMAC cycle
30   FOR I=1 TO 1000     'Delay loop
40   NEXT I
50   GOTO 20             'Do it again
```

When this program is run, the addressed LED on the front of the 1330 should flash, if not, check the link and switch selections and the Request/Grant chain. CAMAC cycles should now be taking place, and a Dataway Test module will be able to confirm this.

Note that the 1330's registers are addressed on consecutive BYTE boundaries, starting at HEX FC00 (Page FC on the 1MHz bus):

WRITE	Address	READ
Funct. Code	FC05	
Station No	FC04	Encoded L
Subaddress	FC03	Status Register
Data High Byte	FC02	Data High Byte
Data Middle Byte	FC01	Data Middle Byte
Data Low Byte	FC00	Data Low Byte

7.3 General Programming Considerations

It is important to appreciate that it is not always necessary to load all parameters for a command every time you wish to do a CAMAC cycle. For example, reading the same module at the same subaddress repetitively need only involve sending the F code and reading out the data. You may also, of course, read the Status Register to monitor X and Q etc.

Note also that when the Function Code is written, the 1330 will try to perform a CAMAC cycle immediately. It may well be prevented from doing so in multi-controller ACB systems by other units, through Request Inhibit or Auxiliary Controller Lockout. It is, however, quite unlikely that even under these circumstances the 1330 will not have completed its CAMAC cycle by the time the software accesses the unit again. If the unit is accessed before it has completed its CAMAC cycle, the Fail bit will be set in the Status Register.
*** See Section 10 - Fast Access Modification ***

7.4 Interrupts

One very important aspect of the handling of all interrupts should be well understood before you write your software.

Imagine that you wish to perform a CAMAC command. You enter a sub-routine, which starts to load the registers of the 1330. Halfway through, you get an interrupt. The Interrupt Service Routine accesses the relevant module, clears the LAM etc. and exits. You will then return to your CAMAC command subroutine, but the Interrupt Service Routine has overwritten some or all of your registers. How do you recover this situation?

One way, of course would be to disable interrupts on entry to the CAMAC command subroutine, and re-enable on exit.

Another way might be to save all your parameters on entry, count your way through the subroutine, and make the interrupt service routine save the Read Data and Status Register on entry. Thus when you return to the Command subroutine, knowing that you have been interrupted, you can assess how far you got and restart if necessary.

Remember to Read the ENCL (Encoded LAM) before exiting the Interrupt Routine in order to clear out the stored LAM and FLAG and restart the LAM scan.

7.5 LAM Mask

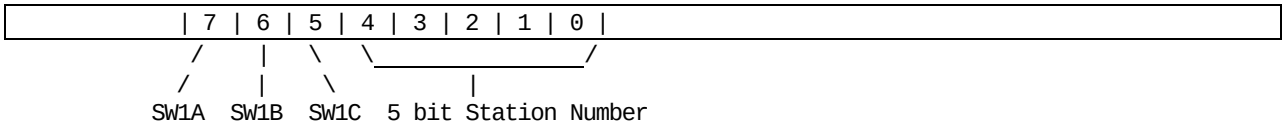
- Access to the LAM Mask is through Function Codes 64 and above:

F(64 + N)	Set Mask bit to '1' (Enable) for Stn. N (0 - 23)
F(128 + N)	Clear Mask bit to '0' (Disable) for Stn N (0 - 23)
F(192 + N)	Leave Mask bit unchanged for Station N (0 - 23), allow examination of Mask bit and L line state through ENCL.

Note: Station number 0 refers to the Software LAM, set by F(49) and cleared by F(48). Setting the Software LAM while SW1D is open will invoke the Auto-subaddress Increment Feature. LAM 0 should be Masked OFF, of course, when using this feature.

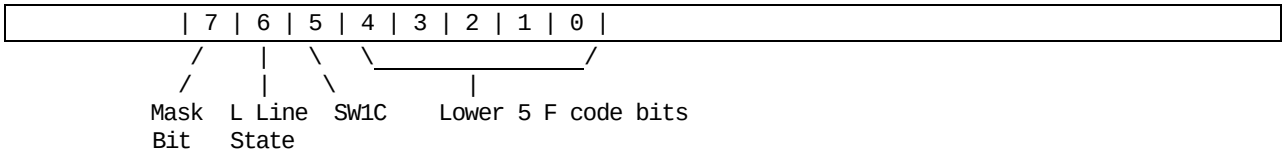
The presence of a Function Code of 64 or more stops the LAM scanner and switches the bottom 5 bits of the Encoded L Register to become the lower 5 Function Code bits as follows:

Encoded L Register - Normal Operation



Note that reading the Encoded L Register when no unmasked LAM is present will give a random number, so check the Status Register Interrupt Flag first.

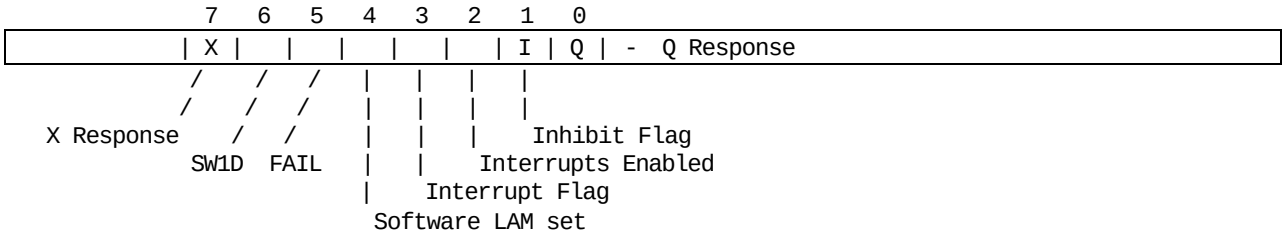
Encoded L Register - LAM Mask Access Operation



Note: The LAM Scanner is restarted once a Function Code of less than 64 has been written to the 1330.

7.6 Status Register

The Status Register format is as follows:



Note: FAIL means that the last attempted access to the 1330's registers was not permitted since a CAMAC cycle was pending at the time. This bit is reset by F(40) or F(41). FAIL will cause a Direct Interrupt (that is to say an Interrupt with no associated Encoded L) if Interrupts are enabled.

Note that the Fast Access Modification described in Section 10 should always prevent I/O cycles being performed by an IBM PC/AT machine or compatible and so the FAIL bit should never be set.

7.7 Special Function Codes

Code(s)	Purpose	Code(s)	Purpose
0-31	Normal CAMAC cycle	40	Disable Interrupts
32	Clear Inhibit	41	Enable Interrupts
33	Set Inhibit	48	Clear Soft LAM
34	Z cycle, clear I	49	Set Soft LAM
35	Z cycle, set I		
36	C cycle, clear I		
37	C cycle, set I		

8. Circuit Description

This circuit description should be read in conjunction with the following Circuit Diagrams:

HL 1014 IBM Personality Card Circuit Diagram
HL 1015 1330 Station 24 Front and Rear Circuit Diagram
HL 1016 1330 Station 25 Circuit Diagram

8.1 Personality Card

Starting at the top left of the diagram, the card is powered from the System Board +5V power rails. It consumes about 200 mA.

Just below the decoupling capacitors we see the Base Address Comparator and Selection Switches. Looking for equivalence on either side of the LS85 comparator, we must have -AEN low and SA9 high, then SA7 and SA8 must equal the states of SW1 A and B. These two switches select the Base Address to be one of four values; HEX 200, 280, 300 or 380. The comparator is enabled by a High on A=B IN, pin 3, and this comes from IC4 pin 8 which will go high when either -IOW or -IOR goes low, that is the Processor is doing either an I/O Write or an I/O Read. The output of the LS85 comparator is output as notDS (Device Select low) from IC4 pin 11, provided that IC4 pin 12 is high. This will be true if either Link 2 is OUT or IC4 pins 1 and 2 are NOT both high. This gate, IC4 pins 1,2 and 3 is looking for a Crate Address of 6 or 7 so as to avoid possible clashes with other I/O page devices at the top of some Base Address pages. Notice at this point the gating which prevents DS being output if START is TRUE as described in section 10 and also the gate, which sends out IOCHRDY (I/O channel ready) in the false state at this time.

We will, therefore, get Device Select and also enable the bi-directional Data Buffer, IC 1, when our Base Address is present and the crate address is in the range 0 to 5 (unless Link 2 is OUT).

Notice that the OR of -IOW and -IOR is output as ENABLE (E), and that the addresses for crate and register address decoding are shifted by one bit so as to put registers on Word Boundaries.

Notice also that we generate the Read/Write signal (R/notW) from -IOW.

The Direction signal for the bi-directional data buffer is obtained from -IOR and decides whether data flow is FROM or TO the processor.

Below the data buffer, we see the RESET line from the System Board, which is inverted to give notINIT to the controller. Below that is the Interrupt connection system, where the active LOW INTR line from the controller can be patched to one of 9 System Board IR (Interrupt Request) lines.

8.2 Station 24 Front and Rear

Starting again at top left, we see first the Crate Address decoder, IC6, which is enabled by notGO on pin 4. The two other enable inputs, pins 5 and 6 are not normally used and are held in the active state by R5 and R6. Addresses A3, A4 and A5 are then decoded, and if the Crate Select slide switch is in the right position, then the common output line, pulled up by R11 will go LOW. This then triggers the Addressed LED flasher, IC9, D1, C3 etc., and enables the Register Read decoder, IC3, the Register Write decoder, IC4 and the bi-directional data buffer, IC5.

The Read and Write decoders are enabled by E, and are selected, as you might expect, by R/notW. Register selection is based on address lines A0, A1 and A2.

The signals R0 to R4 and W0 to W5, all active LOW, go off the board via the 34 way ribbon cable connector to Station 25, along with the Data Bus, D0 to D7.

The notGO signal mentioned above comes from bottom left on the diagram, and is generated as follows:

After de-glitching by R2 and C2, the notDS signal is fed to Link 1. This selects either the "pure" version (link 1 b) or a "cleaned-up" version (link 1 a). The "cleaned-up" version is incorporated to cope with a "double E pulse" problem on the BBC Micro, and need not concern us when using the 1330 on an IBM PC.

The selected DS pulse is then fed to the "collision detector", IC9, which detects an attempt to Read or Write the Interface while a CAMAC cycle is pending. The output of this latch is fed to Station 25 as FAIL after latching again in the cross-coupled gates, IC8. The Fail detector, IC9, is reset as soon as a valid access is attempted. The cross-coupled gates are reset by K6+PONR, which is pulsed by Function codes 40 or 41 (Disable or Enable Interrupts) or Power-on-Reset.

In this area we also see the active low INTR open-collector output, which is the AND of INTEN (Interrupt Enable) and LSUM (unMasked LAM Present) with the FAIL signal diode-ORed in for good measure.

The right hand side of the circuit concerns itself exclusively with the Dataway READ and WRITE lines.

The READ lines are pulled up by removable resistor packs and are fed to inverting tri-state output latches (ALS534), IC's 11, 12 and 13. These are all clocked by READS2, which comes from Station 25 and denotes that the 1330 is READING and that S2 strobe is present. Their outputs are enabled by R0, R1 and R2, the decoded Register Read signals from Station 24 Front, in order to allow the computer to obtain the READ Data from the last CAMAC cycle.

Notice that the internal Data Bus is HIGH TRUE, as opposed to the Dataway, which is LOW TRUE.

To the right of the Read Latches are the Write Latches, which are strobed by Register Write signals W0, W1 and W2 and whose outputs are driven onto the Dataway Write lines, which are again pulled up by removable resistor packs, by 48mA drivers enabled by the signal WRITE. This is generated when the 1330 is doing a CAMAC cycle involving Write Data and is asserting BUSY.

Station 24 Front is powered from station 25 via the 34-way ribbon cable, while Station 24 Rear takes its own power from the Dataway.

8.3 Station 25

The Circuit Diagram for Station 25 splits neatly into sections:

Top left	LAM Scanning, LAM Mask
Top right	Function Code Decoding, C,Z,I control, Interrupt Enable, Status Register
Bottom left	Station Number decoding and buffering, Subaddress output
Bottom right	ACB Arbitration, CAMAC cycle generation

Top left we see the L lines from the Dataway, buffered by IC's 4, 5 and 6 and fed to the multiplexers, IC's 7, 8 and 9 and to the ACB AL lines. When the 1330 is NOT in Stations 24 and 25, the buffers are turned OFF, so as not to see the Data on the Read and Write lines, by signal MAS. This signal is High, i.e. the buffers are Enabled, when the resistor packs are IN. When they are removed for use of the 1330 as an Auxiliary, MAS goes LOW, switching OFF the buffers and also disabling the N line decoders.

The AL signals are scanned in turn by the LS355 multiplexers, along with the Software LAM, SLAM, fed in as LAM 0. The open-collector outputs of the multiplexers are "Wire-ORed" together (pins 19), and pulled up by R9. The scan oscillator, IC18 (LS393), which is clocked by the master 10MHz clock, controls the scanning of the multiplexers. Each L line is therefore selected in turn and its state presented to IC25 pin 8. The scan address is also fed to the Mask RAM, IC19 (74S201), whose active low output is presented to IC25 pin 9. If IC25 pins 8 and 9 are ever both low together, that is to say the LAM is present and the Mask output is True, then the LSUM Latch IC39 pin 9 will be set high. This has two effects; first it causes an Interrupt, if Interrupts are enabled, because LSUM goes to Station 24 Front for output as INTR; second, it stops the scan oscillator through IC 27, pins 13, 12, 11. The LAM Scanner is now "frozen", with its scan address pointing to the unMasked LAM.

The computer can read this address by reading ENCODED L (R4). This enables the buffer IC23, which outputs 5 bits of LAM scanner address plus three bits of switch data from SW1 A to C. We have not yet touched on the address multiplexers, IC's 16 and 17, which are normally selecting their B inputs in the absence of signal MT. This signal will be active LOW whenever Function code bits F64 or F128 are present, which denotes "Mask Twiddling", hence the name MT. When this takes place, the scan address becomes equal to the bottom 5 bits of the function code. The corresponding bit in the Mask RAM can thus be written to '0' or '1' and the state of both Mask RAM output and L line observed through reading the encoded L.

Writing to the Mask RAM works as follows:

On power-up, the Function Code latch IC22, top right, is cleared to ensure that MT is not true.

A burst of scan oscillator pulses QB is fed to the write (W) pin on the Mask RAM while the data is zero. (IC28 pins 3,2,1 write pulses; IC17 pin 13 to pin 12 for zero data). This clears all elements in the Mask RAM. When either F64 or F128 is present, but NOT both (IC30 pin 11 conditions IC28 9,8,10), the pulse which strobes the Function Code decoder PROM, generated from W5, puts a Write pulse on pin 12 of the Mask RAM, writing the state of F64 into it on DIN (F PROM pulse IC49 pin 13, F64 to IC17 pin 14 to pin 12 to DIN on RAM).

Notice that the scan oscillator is stopped when MT is true, so after altering the mask one must send a Function Code less than 64, to free it, and also that the scan oscillator resets itself on 24, through IC30 pins 4,5,6, so that it scans 0 to 23 and back to 0 again.

Notice that reading the Encoded L with R4 generates a short reset pulse for the LSUM latch, freeing the scan oscillator. The LAM scanner will then search for another unMasked LAM. It will thus either go right the way round to the original LAM, or may find another. Scan time is 400nSec per LAM, i.e. 10 microseconds per complete scan. The purpose of the LSUM latch and the "release-scan" system is twofold:

To detect and hold "fleeting" LAMS

To allow an Interrupt service routine to find out not only which station caused the Interrupt, but also if any other modules, possibly higher priority ones, have requested service since the original request was made.

Bottom Left we see the N Store and its decoders, IC's 20 (store) and IC's 1, 2 and 3. The N Store is clocked by W4 and its output is enabled by AFGO, a version of Dataway BUSY. The N value from the store is fed to the decoders and also OUT onto the ACB EN lines while it is doing a CAMAC cycle. At all other times it accepts EN data from the ACB and feeds it to its decoders. Thus, if it is Master (Stations 24 and 25) then the 1330 will decode any valid ACB EN given to it. When it is not Master, the decoders are disabled anyway.

Just to the right of the N Store we see the Subaddress Store/Counter. This is normally simply loaded with the desired subaddress value, which is output onto the Dataway as usual. If, however, the Software LAM is set (remember that it should be Masked OFF to avoid an Interrupt), then the Count Enable pin of the chip, pin 7, will be high allowing the End Pulse from the CAMAC cycle generator to increment the subaddress, provided, of course, that Switch 1D is open to enable IC43 pins 4,5,6. This is intended for applications where a lot of subaddresses need to be scanned in turn, for example a 16 channel ADC, to save having to reload the subaddress each time.

Top Right we see the Function Code latch, IC22, and its decoding PROM, IC26 "IBM V2". After the new F Code has been latched in, a 100nS pulse delayed by 100nS strobes the PROM via pin 15. The outputs of the PROM function as follows:

Function Code	Action	Result
0-7	pulse pin 2	generate READS2
16-23	pulse pin 1	generate WRITE
40-41	pulse pin 6	set or clear INTEN
48-49	pulse pin 4	set or clear SLAM
32-37	pulse pin 7	set/clear I, generate C or Z
0-31, 34-37	pulse pin 5	set START latch, cause a CAMAC cycle

Notice how the flip-flops for READS2, WRITE, C and Z, set by the various pulses from the PROM are all knocked down by End Pulse from the CAMAC cycle generator. Note also that if either the C or the Z flip-flop is set, then NOBUSY is generated, IC45 pins 13,12,11, to inhibit all the A, F and N outputs.

At the bottom of this section of the circuit, on the right, we see the Q and X latches, which sample these lines at S1 time. The outputs of these latches go to the SR buffer (Status Register), IC24, whose outputs are enabled onto the Data Bus by R3.

Bottom Right we see the CAMAC cycle generator, set in motion as described above by the START signal, and clocked by the 10MHz master oscillator, IC40, RV1. The operation of this state machine is beyond the scope of this manual, but suffice it to say that it conforms to all the specifications of EUR6500, including aborting on ACL etc. and can operate in either R/G or ACL modes.

The monostable IC46 and flip-flop IC47 act to ensure that End Pulse is only generated on the trailing edge of a complete BUSY pulse, and therefore that ACL aborted cycles are ignored from the point of view in particular of resetting the START latch.

Also in this corner of the circuit is the power-on-reset system, which generates active low and active high reset pulses for all parts of the circuit for about 200mSec after power-on and also in response to the front panel reset button and the reset line from the computer.

The rather complicated system of zener and transistor etc. ensures that even a brief interruption of the supply will be recognised and mal-operation avoided.

9. ACB Configuration Information

On the front of the 1330, there are three LEMO sockets, labelled REQUEST, GRANT IN and GRANT OUT. When constructing a multi-controller ACB system, very careful thought must go into the way that each device is included in the arbitration scheme, which these sockets construct.

Some devices are very fast indeed and, if placed at the top of the arbitration hierarchy, would effectively "lock" everybody else out. These devices, although they must be reasonably high in priority so as to achieve optimum throughput, must not be allowed to prevent other more important devices from performing essential control actions. These "more important" devices will usually be computer interfaces, which, although their access rate may be relatively slow, will nevertheless require to "get in" whenever they need to, in order to service Interrupts, for example.

When connecting up the Request/Grant chain, therefore, always remember to put the main computer interface if not first, then certainly second in line. The faster devices, although they may experience interruptions in their streams of activity, will be only slightly affected by the other devices doing their cycles.

The ACB cable at the back (the 40-way ribbon cable) connects REQUEST together for all ACB Controllers. Using the front panel LEMO sockets, the Highest Priority device then connects REQUEST to GRANT IN, then its GRANT OUT is connected to GRANT IN on the next lowest priority controller, then GRANT OUT on this to GRANT IN on the next, and so on. REQUEST is an open-collector output; GRANT IN is a pulled-up input; GRANT OUT is an open collector output, thus the wired-OR arbitration system is constructed.

10. Fast Access Modification

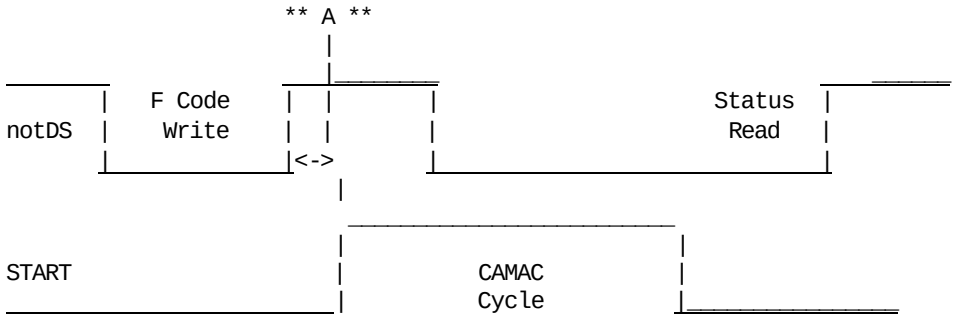
In Section 7.3, brave words were spoken about it being very unlikely that a processor would be able to access the 1330 again, having caused a CAMAC cycle to occur, before that cycle had completed. This was probably quite true when the 1330 was designed in 1985 but it appears to be very far from it now (Dec 1988) with the arrival of "Zero Wait State" 286 and 386 machines with clock speeds of 25 MHz and above. When "Machine Code" software such as the ESONE routine package is run, or code from an optimised Compiler, software running on these new machines is quite capable of "beating" the 1330, especially when it has to arbitrate with other ACB devices for Crate access.

For this reason, a modification has been included in the design as of December 1988 to cope with this potential problem. This modification involves sending the START signal, which denotes that the 1330 is either doing or is about to do a CAMAC cycle, down the Private Bus cable in an inverted form, so that the Personality card can delay the processor's next cycle using IOCHRDY - I/O Channel Ready - in the False state.

The circuitry on the personality card works as follows:

When the Address Comparator IC 5 sees an I/O Read or Write at its address, pin 6 will go high (A=B OUT). If START is true, then IOCHRDY will be pulled low immediately by IC 4 pin 6. The processor will insert wait states into the I/O cycle until IOCHRDY is released, at which point the data will be transferred and the read or write cycle will complete.

The Timing Diagram below shows how the modification ensures correct operation when an F Code Write is followed swiftly by a Status Register Read, for example: -



The Timing Diagram shows a gap between the trailing edge of the Function Code Write pulse and the START signal going TRUE. This delay is due to the F Code strobing monostables of IC49 and clearly if the processor were to start a second access at "A", i.e. before START goes TRUE, then an error would occur. To avoid this, changing IC49 from a 74LS123 to a 74123 has reduced the delay, and C6 has been removed. This reduces the delay from approx. 250 nSec to about 90 nSec.

11. Physical and Electrical

The 1330 is a two-width CAMAC controller. It consumes a total of approximately 2 Amps from the CAMAC +6 volt line; no other supplies are used. Due to the low power consumption of the unit, forced air-cooling is not essential.

The IBM personality card consumes approximately 200 milliamps of +5 volt power from the PC. No other power supplies are used.

12. Parts List and Assembly Details

12.1 Station 24 Front

12.1.1 Integrated Circuits

Type	Qty	Component Reference
74LS02	2	IC1, IC8
74LS04	1	IC10
74LS14	3	IC2, IC7, IC11
74LS74	1	IC9
74LS138	3	IC3, IC4, IC6
74LS245	1	IC5

12.1.2 Discrete Semiconductors

2N3704	1	TR1
1N4148	3	D1, D2, D3

12.1.3 Passive Components

1K x 13 Res.Pk	4	RN1, RN2, RN3, RN4 (on sockets)
220R 0.25W	2	R8, R9
470R	2	R5, R14
1K0	6	R1, R2, R3, R4, R6, R7
3K3	3	R10, R11, R12
100K	1	R13
22pF cer.	2	C1, C2
220pF cer.	1	C10
100nF cer.	6	C4, C5, C6, C7, C8, C9
1uF 35V tant.	1	C3

12.1.4 Miscellaneous

1 pole 8-way slide switch	1	SW1
34-way rt. angle header with latches	1	T&B 612 3454 ES

12.2 Station 24 Rear

12.2.1 Integrated Circuits

7404	1	IC1
7438	6	IC2, IC3, IC4, IC5, IC6, IC7
74LS273	3	IC8, IC9, IC10
74ALS534	3	IC11, IC12, IC13

Parts List & Assembly Details (cont'd)

12.2.2 Discrete Semiconductors

1N4005	1	D1

12.2.3 Passive Components

560R x 13 res. pk. (on sockets)	4	RN1, RN2, RN3, RN4
100nF cer.	5	C1, C2, C3, C4, C5

12.2.4 Miscellaneous

1 amp Littelfuse	1	FS1 (on inserts)

12.3 Station 25

12.3.1 Integrated Circuits

Type	Qty	Component Reference
74LS00	2	IC27, IC43
74LS02	5	IC25, IC28, IC29,IC42, IC45
7404	1	IC44
74LS08	4	IC25A, IC30, IC41, IC50
74LS14	1	IC35
7438	5	IC11, IC13, IC14, IC15, IC31
74LS74	6	IC36, IC37, IC38, IC39, IC47, IC48
74LS75	1	IC34
74123	1	IC49
74LS123	2	IC46
74S124	1	IC40
74LS157	2	IC16, IC17
74LS161	1	IC21
N82S23N	4	IC1 (NDA), IC2 (NDB), IC3 (NDC), IC26 (IBM V02)
74S201	1	IC19
74LS244	5	IC4, IC5, IC6, IC23, IC24
74LS273	1	IC22
74LS355	3	IC7, IC8, IC9
74LS374	1	IC20
74S374	1	IC32
74LS393	1	IC18
74LS620	1	IC10
75452	1	IC12
82S100	1	IC33 (1330)

12.3.2 Discrete Semiconductors

2N3704	1	TR1
1N5401	1	D1
BZY88C3V3	1	D2

Parts List & Assembly Details (Cont'd)

12.3.3 Passive Components

560R x 8 SIL	10	RP1 - RP10 inc. (RP1-9 on socket strips)
120R 0.25W	2	R19, R20 (on sockets)
220R	2	R6, R7
470R	1	R10
560R	2	R5, R8
1K0	6	R4, R9, R15, R21, R22, R23
4K7	3	R16, R17, R18
10K	5	R3, R11, R12, R13, R14
82K	1	R1
220K	1	R2
5K PRESET	1	RV1
10pF	1	C7
33pF cer.	2	C8, C9 note: C6 not fitted
100pF cer.	1	C5
100nF cer.	12	"C"
1uF 35V tant.	1	C4
2.2uF 35V tant.	1	C3
68uF 16V al.	2	C1, C2

Station 25 Cont.

12.3.4 Miscellaneous

PCB Mounted LEMO Socket	3	20-way straight header	1	
34-way straight header	1	4-way on/off DIL switch	1	SW1
40-way rt. angle header	1	2 amp Littelfuse	1	FS1

12.4 Module Assembly Parts

2-width CAMAC module kit; Front panel machined and engraved; Rear panel machined; TIL 209 LED (Qty 4), wired to PCBs 24 Front and 25; Min push button (PB), wired to Stn 25.

Note: Allow 10 inches of wire on connections of push button and Stn 25 LEDs to permit the module to be opened up for access.