IBM 1331/TURBO

IBM PC/XT/AT and Compatibles

CAMAC INTERFACE and CRATE CONTROLLER

TECHNICAL MANUAL

and CIRCUIT DESCRIPTION

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1. Introduction

The IBM 1331/TURBO PC Interface Set consists of a 1331 Personal Computer CAMAC Interface module, an IBM personality card and an interconnecting cable three metres long. The 1331 is a direct descendant of the 1330/IBM Interface/controller, with which it is designed to be 100% downwards compatible in software terms, i.e. any software written for the 1330 will run with the 1331. The basic features common to both are described in this manual, followed by a section on the extra advanced features of the 1331 (Section 8).

Normally, the 1331 interface and personality card will be supplied set up as the "first crate" i.e.

PC Address	-	Hex 280 I/O PAGE
Crate Select	-	Crate 0
ACB Arbitration	-	Request/Grant Mode
Master/Slave Sel.	-	Master Controller
Interrupt Request	-	Linked to IRQ5
DMA Level	-	No links selected

2. 1331 Setting Up

The unit consists of two printed circuit boards:

Station 24 (The Left Hand Board)
Station 25 (The Right Hand Board)

Since this controller is configurable as an Auxiliary Controller (ACB) it can be placed anywhere in the crate: even so, referring to these boards by their 'Master' station numbers is convenient and unambiguous. Note that if the 1331 is not fitted in Stations 24, 25 then those positions must be occupied by a suitable Master.

These boards are set up as follows:-

2.1 Station 24

2.1.1 Crate Select Switch. This is an 8-way DIP switch.

For single-crate applications, select Crate 0 by closing the front-most switch only, all others open. For crate 1, close the next one back and leave all the others open, and so on. Note that the standard configuration of the Personality Card Address Decode allows only FOUR Crates to be connected.
(Other arrangements to special order).

2.1.2 Private Bus Termination

Except where multiple 1331's are "daisy-chained" onto the same private bus cable, the 1331 will be the only device on this bus, so terminating packs RN1,2,3, and 4 should be fitted. In multi-crate situations only the last crate on the bus should have the resistor packs fitted. The maximum recommended length for the bus is 20 metres.

2.1.3 Dataway Pull-up Resistor Packs

These 6 packs of 8 x 560 ohm pull-up resistors per SIL pack, RN6 - RN11 should be fitted if the 1331 is in stations 24 and 25. If the 1331 is an Auxiliary Controller they must be removed.

2.1.4 Standard Configuration Station 24

Crate Select	Set for Crate 0
RN6-11	Fitted

2.2 Station 25 (see Section 3 for access)

2.2.1 Dataway Pull-Up Resistor Packs

If the 1331 is an Auxiliary Controller i.e. not in Stations 24 and 25, then SIL Resistor Packs RP1 to RP9 should be removed, along with discrete resistors R19, R20. The Resistor Packs are 8 x 560 ohm, and R19, R20 are 120 ohms.

2.2.2 Link 1 Request/Grant or ACL (Auxiliary Controller Lock-out)

For Normal operation, R/G Mode, leave this link OUT. For ACL Mode Insert Link 1. Note that only one device in the ACB Arbitration scheme is allowed to be in ACL Mode. (see Section 10)

2.2.3 Switch 1 A,B,C,D

SW1 A,B,C control the top 3 bits of the Encoded LAM Register. Switch OPEN=1, CLOSED=0.

SW1C controls bit 5
SW1B controls bit 6
SW1A controls bit 7

The purpose of these switches is to enable the Encoded LAM number to be used as a Vector for a Service Routine. Normally ALL CLOSED.

SW1D controls the Subaddress Auto Increment Feature in conjunction with SOFT LAM, (see Sect. 7.5) and appears as Bit 6 in the Status Register. Open = '1' = 'Enabled'.

2.2.4 Standard Configuration Station 25:

Link 1 OUT, Pull-ups IN, SW1 A-D all Closed.

3. 1331 Maintenance Access

For access to the component side of board 25, for example to remove the pull-up resistor packs, first remove both side covers from the module, then remove the securing screws from the top rail of the Station 25 board at front and rear. Loosen the screws securing the bottom rail of Station 25 front and rear and gently swing this board away from the rest of the unit. When you can get to it, reach in and pull the 34-way socket connector off its header, to allow the unit to open to its fullest extent, taking care that the wiring to the front panel hardware does not get stretched.

To reassemble, simply reverse the procedure.

Always store the resistor packs in a safe place if you do take them out, so that they can be replaced if necessary.

4. 1331 Front Panel

The 1331 Front Panel carries the 50-way Centronics type private bus connector, 3 holes for access to the PCB-mounted Request/Grant Connectors, sixteen LEDs and a reset button.

4.1 Private-bus Connector

Standard 50-way Centronics style socket connector. Pin 1 is top left.

4.2 Indicator LEDs

4.2.1 Request/Grant LED - When ON, shows that R/G mode is selected by link 1 being OUT on the Station 25 board. Will normally be on all the time.

4.2.2 Inhibit LED - shows the state of the internal inhibit flip-flop rather than the Dataway Inhibit line. Comes on after Power-Up or Reset.

4.2.3 Function Code LEDs - 8 LEDs to show the last Function Code written to the 1331.

4.2.4 Interrupt/ Addressed/ CAMAC LEDs:

Interrupt LED - comes on to show that an interrupt is being sent to the computer. This will happen if an Un-Masked LAM is detected while Interrupts are Enabled.

Addressed LED - flashes when the 1331 detects its own address. Stretched to 10 mSec.

CAMAC LED - flashes when the 1331 is performing a CAMAC cycle, stretched to 10 mSec.

4.2.5 FAIL/ NO X/ NO Q LEDs:

FAIL - Shows that the internal Q Repeat mode cycle generator has failed to get a Q response in 12 microseconds.

NO X - Shows that the last read of the Control and Status Register showed no X response. (Only updated during read CSR).

NO Q - As for NO X but referring to the Q response obtained.

4.3 Reset Button - This performs a "Power-on-Reset" on the whole module. In particular, it resets the following:

The Soft-LAM Flip-Flop
The Function-Code Register (Not the display)
The Q and X stores
The CAMAC-Cycle generator
The Interrupt-Enable Flag
The Inhibit (SET), C and Z Flip/Flops
The Repeat Cycle Sequencer

Whilst pressed, therefore, it stops the 1331 doing anything.

5. 1331 Rear Panel

5.1 ACB Connector

This is the standard 40-way ACB connection to other controllers in the crate. It is a 40-way plug.

6. IBM 1331 Personality Card - Setting Up **NEW ISSUE 4/5 PCB MAY 2000**

6.1 Base Address - selectable by two links to one of 4 addresses in the I/O page as follows:

JP12	JP13	ADDRESS (HEX)
IN	IN	200
OUT	IN	280 (Standard)
IN	OUT	300
OUT	OUT	380

NOTE: THERE IS A KNOWN ADDRESS CLASH BETWEEN A PERSONALITY CARD SET TO ADDRESS 300 HEX AND MANY TYPES OF ISA NETWORK CARDS AND SOUND CARDS. TO AVOID THIS, HYTEC RECOMMENDS THAT YOU ALWAYS SET THE PERSONALITY CARD TO ADDRESS 280 HEX UNLESS YOU HAVE A SPECIAL CARD AT THAT ADDRESS.

Normally, the address range decoded by the Personality Card is from Base Address to Base Address plus 3F HEX for up to 4 crates. This is because, in some computer installations, other peripheral devices reside at the top of some pages, which restricts the area available to CAMAC. To special order, however, we can provide an alternative decode PAL, giving 6 or even 8 crate access in one of the Address Pages. Contact HYTEC for details.

6.2 Interrupt Request Selection.

A group of links allows you to select any one of four IRQ lines on the System Board through which to interrupt the processor. IRQ 9 and IRQ 12 are only available on PC/AT and compatible machines, IRQ 3 and IRQ 5 are available on all machines. The choice of IRQ line is beyond the scope of this manual, except to say that the ESONE Subroutines use IRQ5 for interrupts.

LINK IN	IRQ line selected
JP8	IRQ 5
JP9	IRQ 3
JP11	IRQ 9
JP7	IRQ 12

Standard selection - IRQ 5.

6.3 DMA Request/Grant level

Six links, three each for Request and Grant level, determine which DMA channel is used on the System Board for the 1331 Advanced Feature - DMA Operation.

DMA Level	Links IN	Links OUT
5 (16-bit)	JP3,JP4	JP1,JP2,JP5,JP6
6 (16-bit)	JP5,JP6	JP3,JP4,JP1,JP2
7 (16-bit)	JP1,JP2	JP3,JP4,JP5,JP6

6.4 Target device select:

There is a new jumper on the personality card issue 4 & 5 which selects either 1331 CAMAC mode or 3331 VME mode. This is used to control the way the remote device is handled. JP10 IN = 3331 VME mode, OUT = 1331 CAMAC.

7. Installation, Operating and Programming

7.1 Introduction

The best way to understand how to use the 1331 is first to install and use it as if it were a 1330. Then, when you have done this, you can start to access some of the advanced features incorporated in the 1331.

7.2 IBM PC/AT and Compatibles

Remove the top cover of the computer and install the personality card in a free expansion slot. If the machine is an AT or AT compatible, then some of the slots will have two edge connector sockets rather than one. These are the A/B C/D slots which carry the full 16 bit data bus. This is not important to the operation of the personality card or the 1331 if you are not going to take advantage of its access to the 16-bit data bus since when operated as a 1330 it only uses an 8 bit port, but the A/B C/D slots also carry extra Interrupt lines which you may wish to use.

Having chosen the expansion slot in which to fit the Personality Card, set the Base Address Links as desired, select the Interrupt Request Link and DMA links as desired and install the card, securing it with the fixing screw.

If fitting seems awkward, loosen the bracket fixing screws where some latitude is available for accommodating slight mechanical differences, which do occur on some PC's.

Plug in the private bus cable. Before replacing the cover, check that the personality card is seated correctly.

Set the links and switches on the 1331 and install it in the crate. Fit the private bus cable and connect up the Request/Grant chain (see Sect. 10). Also fit the rear 40-way ACB cable between controllers, if there is more than one.

Switch ON the computer, monitor and CAMAC crate. Note that powering down the crate and 1331 will not affect the computer.

IF THE COMPUTER FAILS TO BOOT, CHECK THAT THE REQUEST/GRANT CHAIN IS INSTALLED CORRECTLY, SINCE THE 1331 MAY POWER UP WITH A CAMAC CYCLE PENDING AND IF THIS HAPPENS, THE I/O CHANNEL CHECK WILL FAIL SINCE "START" IS TRUE.

When the computer has booted up into DOS or Windows 95/98, run any version of BASIC or QUICK BASIC and type in this program:

```
10  FUN=&H28A       'Function code register at base + 10
20  OUT FUN,0       'Send Function code 0, do a CAMAC cycle
30  FOR I=1 TO 1000 'Delay loop
40  NEXT I
50  GOTO 20         'Do it again
```

Running this program should flash the Addressed and CAMAC LEDs, provided the base address is selected to be HEX 280 (otherwise change line 10) and the 1331 should now be doing CAMAC cycles. If you have a Dataway Test Module, you will be able to observe this happening.

If all is not well, check all your selections on the 1331 and on the personality card and try again. Also check the Request/Grant chain.

You are now ready to write your Application Program, possibly using the high-level-language-callable-subroutines or maybe using Compiled BASIC.

Remember that the registers in the 1331 are on WORD boundaries, so as to give correct operation on 16 bit machines, so their addresses are:

WRITE	Address	READ
	28E	[Diagnostic Readback]
[Repeat Register]	28C	[Repeat Register]
Function Code	28A	[A, N, F Readback]
Station Number	288	Encoded L
Subaddress	286	Status Register
Data High Byte	284	Data High Byte
Data Middle Byte	282	Data Middle Byte
Data Low Byte	280	Data Low Byte [281 New CSR]

Items in square brackets - [] are Advanced Feature extra registers of the 1331.

7.3 General Programming Considerations

It is important to appreciate that it is not always necessary to load all parameters for a command every time you wish to do a CAMAC cycle. For example, reading the same module at the same subaddress repetitively need only involve sending the F code and reading out the data. You may also, of course, read the Status Register to monitor X and Q etc.

Note also that when the Function Code is written, the 1331 will try to perform a CAMAC cycle immediately. It may well be prevented from doing so in multi-controller ACB systems by other units, through Request Inhibit or Auxiliary Controller Lock-out. It is, however, quite unlikely that even under these circumstances the 1331 will not have completed its CAMAC cycle by the time the software accesses the unit again. If the unit is accessed before it has completed its CAMAC cycle, the Personality Card will simply assert IO CHANNEL NOT READY on the System Board to cause the processor to insert WAIT States in the IO cycle until the 1331 is no longer busy, at which time the IO cycle can complete.

7.4 Interrupts

One very important aspect of the handling of all interrupts should be well understood before you write your software.

Imagine that you wish to perform a CAMAC command. You enter a sub-routine, which starts to load the registers of the 1331. Halfway through, you get an interrupt. The Interrupt Service Routine accesses the relevant module, clears the LAM etc. and exits. You will then return to your CAMAC command subroutine, but the Interrupt Service Routine has overwritten some or all of your registers. How do you recover this situation?

One way, of course would be to disable interrupts on entry to the CAMAC command subroutine, and re-enable on exit. This is indeed how the problem was handled in the 1330 software.

A much better way is to make all the Registers fully Read/Writeable, and this is what has been done in the 1331, as we shall see later (section 8).

Remember to Read the ENCL (Encoded LAM) Register before exiting the Interrupt Routine in order to clear out the stored LAM and FLAG and restart the LAM scan.

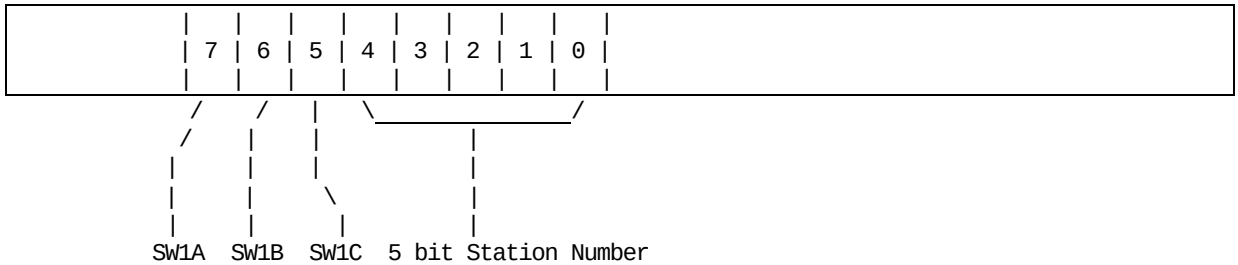
7.5 LAM Mask - Access to the LAM Mask is through Function Codes 64 and above:

F(64 + N) Set Mask bit to '1' (Enable) for Station N (0-23)
F(128 + N) Clear Mask bit to '0' (Disable) for Stn. N (0-23)
F(192 + N) Leave Mask bit unchanged for Station N (0 - 23),
allow examination of Mask bit and L line state through ENCL.

Note: Station number 0 refers to the Software LAM, set by F(49) and cleared by F(48). Setting the Software LAM while SW1D is open will invoke the Auto-subaddress Increment Feature. LAM 0 should be Masked OFF, of course, when using this feature.

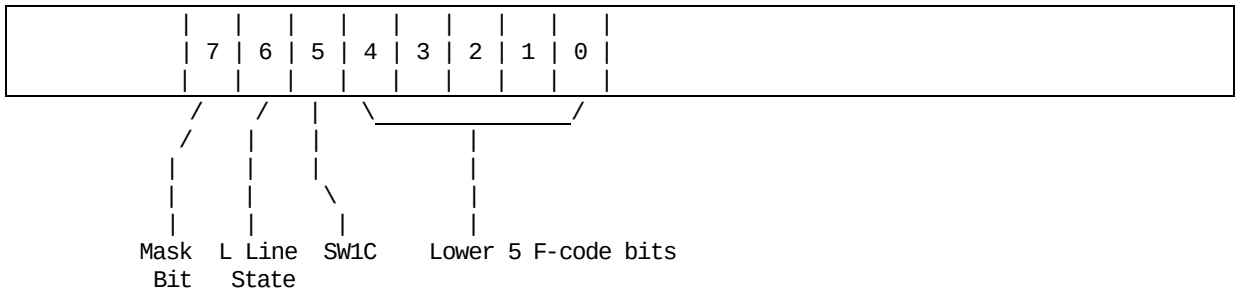
The presence of a Function Code of 64 or more stops the LAM scanner and switches the bottom 5 bits of the Encoded L Register to become the lower 5 Function Code bits as follows:

Encoded L Register - Normal Operation



Note that reading the Encoded L Register when no unmasked LAM is present will give a random number, so check the Status Register Interrupt Flag first.

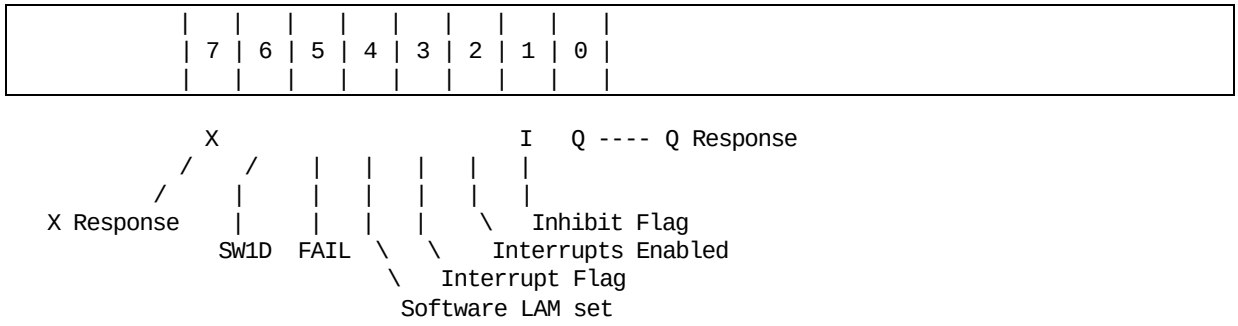
Encoded L Register - LAM Mask Access Operation



Note: The LAM Scanner is restarted once a Function Code of less than 64 has been written to the 1331.

7.6 Status Register

The Status Register format is as follows:



Note: FAIL means that the last attempted Q Repeat cycle (one of the 1331 advanced features) failed to get a valid Q response within 12 microseconds.

7.7 Special Function Codes

Code(s)	Purpose	Code(s)	Purpose
0-31	Normal CAMAC cycle	40	Disable Interrupts
32	Clear Inhibit	41	Enable Interrupts
33	Set Inhibit	48	Clear Soft LAM
34	Z cycle, clear I	49	Set Soft LAM
35	Z cycle, set I		
36	C cycle, clear I		
37	C cycle, set I		

8. 1331 Advanced Features

8.1 Register Readback

One of the biggest drawbacks of the 1330 Controller was the lack of fully read/writeable registers to permit full context restoration after interrupt servicing. To overcome this, the 1331 has been fitted with extra features to enable this to be done, namely:

a) The three byte-wide data registers have been made common to both read and write commands instead of being separate.

b) A readback system has been incorporated for Station Number, Subaddress and Function Code. This works as follows:

An internal "shadow" store stores the most recent loaded values. This can be accessed by sequentially reading the Function Code address (i.e. Base +10), which gives you in turn Subaddress, Station Number and finally Function Code. These can be stored away and then reloaded after the interrupt has been serviced.

8.2 Repeat Cycle Operation

When repetitively reading the same module and subaddress, it was always necessary in the 1330 to re-send the function code in order to reissue the command. This is no longer the case with the 1331, where you can read a location which implies "give me the data and then reissue the command". This can be done in either 8 or 16-bit mode, but for accesses at the same address (i.e. the repeat address) is restricted to 16-bit CAMAC operations. You can of course do 24-bit operations using the repeat feature by passing the top byte first, but this would be at a different address, so would not be compatible with DMA operation, as we will see in the next section.

8.3 DMA Channel Operation

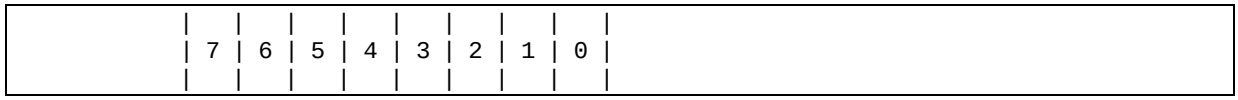
There are DMA Controllers on the PC System Board which have unused channels. In the PC and PC/XT there is just one 8-bit controller with up to two spare channels. In the PC/AT there is an 8-bit controller with up to two spare channels and also a 16-bit controller with three spare channels. The 16-bit channels can be used by the 1331 and its personality card and operation is as follows:

[Please note that hardware DMA is not supported by any of Hytec’s software driver packages, whereas software block modes are].

On the personality card there is a new Control and Status Register addressed at Base address plus 1 (an odd byte address), through which you can set DMA Request by setting bit 3. The System Board DMA Controller then responds with DMA Acknowledge, which then makes the personality card ready to accept DMA cycles. These are distinguished from normal I/O cycles by the fact that AEN (Address Enable) is high on the System Board. At this point, an LED comes on on the personality card to denote "DMA in Progress". You can still access the 1331 after this point with normal I/O cycles, of course, since the personality card can tell the difference (AEN low). When the personality card sees a DMA read or write, it switches over the Register Select lines from System Board address lines to a fixed code, namely the Repeat Address (as mentioned above) and also substitutes the Crate number with a value previously loaded into the new CSR (remember that the DMA controller gives out no address information with its IO Read command). The DMA Controller can then continually read or write CAMAC 8 or 16 bits at a time until its cycle count is exhausted, whereupon "Terminal Count" is pulsed on the System Board and the DMA control logic on the personality card is reset. The repeat cycle logic in the 1331 handles 8-bit cycles automatically, low byte first, then middle byte and re-trigger the CAMAC cycle. In 16- bit mode, which is selected by the presence of SBHE (system byte high enable) on the system board, the 1331 gives 16 bits of data then re-triggers the CAMAC command.

The formal sequences of operation for reads and writes in 8 and 16-bit mode are given in the circuit description section.

New Personality Card Control and Status Register Format



P x x Q A C4 C2 C1

P: DMA in Progress (read only)
Q: Q Mode: '1'= repeat until Q=1: '0'= Q ignore (write/read)
A: ARM DMA '1' = armed (write/read)
C4-C1: Crate Number in binary for DMA cycles (write/read)

Note: Q repeat is subject to a 12 microsecond timeout.

9. Circuit Description

This circuit description should be read in conjunction with the following Circuit Diagrams :

HL 1057 1331 Personality Card Circuit Diagram
HL 1058/9 1331 Station 24 Circuit Diagram - sheets 1 & 2
HL 1016 1330/1 Station 25 Circuit Diagram (common to both)

9.1 Personality Card

On the left of the diagram we see the System Board edge connectors A, B, C and D. The card is powered from the System Board +5V (VCC) and GND (ground) power rails. It consumes about 300 mA.

Top left we see the Address Comparator chip IC7, a 74F521, with the address selection links JP12 & JP13. For a valid NORMAL (as opposed to DMA) address decode, we must have SAEN low and SA9 high, then SA7 and SA8 must correspond to the selection from JP12 and JP13. These two jumpers links select the Base Address to be one of four values: HEX 200, 280, 300 or 380. The output of this comparator goes to the main control chip, IC3, a MACH131, and to some fast response logic producing /IOCHRDY and /IOCS16, which is conditioned by either IOR or IOW being present, that is the Processor is doing either an I/O Write or an I/O Read. The principal control outputs of the main decode device are /WR (Write – active low), /RD (Read) and /DS (Device Select). These go to the 1331 or 3331. The decode device also receives and produces virtually all the other control and timing signals required for the board. The only logic external to this device is the fast section mentioned above and the buffering out onto the 50-way cable to the remote controller(s).

9.2 Station 24

Starting at top left of sheet 1, we see first the Crate Address decoder with incoming terminated buffers, IC20, which is enabled by /BDS on pin 5. The two other enable inputs of this decoder, pins 4 and 6 are held in the true state. Addresses CS0, CS1 and CS2 are then decoded, and if the Crate Select switch is in the right position, then the common output line, pulled up by R5 will go LOW (/CSGO). This then enables the Register Read decoder, IC37, the Register Write decoder, IC36 and triggers the addressed LED flasher just below the read decoder, IC22.

The Read and Write decoders are enabled by /IRD and /IWR respectively. Register selection is decoded from lines RS0, RS1 and RS2 (register select 0, 1 and 2).

The signals R0 to R4 and W0 to W5, all active LOW, go off the board via the 34 way ribbon cable connector to Station 25, along with the Data Bus, DATA0 to DATA7. Notice that some internally generated read and write signals are combined into the R and W signals, and also that W6, R5, R6 and R7 are decoded for local use.

In this area we also see the active low INTR open-collector output, which is the AND of INTEN (Interrupt Enable) and LSUM (unMasked LAM Present), conditioned by NOINT, which has to do with masking interrupts while waiting for the computer to read the CSR, since this can not be saved and restored after interrupts. This "blanking" lasts for up to 30 microseconds.

Here also is the open collector driver for /BUSY which is a common output line used to signal the personality card that one or more of the 1331s on the bus is busy and to hold up the processor.

Below this we see the incoming connector (50-way) and the Data bus terminators and receivers, which are bidirectional latches. The control signals for these latch/drivers come from the "special decodes" PAL, top centre which controls the flow of data and also, in conjunction with the Repeat Cycle Sequencer, centre right, handles the input and output of 8 or 16-bit data to/from the internal 8-bit stores.

Just above the special decodes PAL is the function code store and display latch, which captures incoming F code writes, displays the data and also holds the code for use when the repeat cycle sequencer wishes to use it to trigger another cycle (since it has to do this by writing the F code again).

To the right of this is the Parameter Store, with its pointer system. It is based on a 16 x 8 File store, IC16 74ALS870, which is updated at the incoming register address each time the processor writes to the 1331. When R5 is accessed (Base+10 - read F code), the file store register address is derived from a counter, which until now had been held at the value 3. Thus the first read will be at location 3 (=Base+6) yielding the subaddress, following which the counter is incremented to give the station number on the next read, then the function code. As soon as the 1331 is addressed for a write, the counter is reloaded with 3 to be ready for the next readout sequence.

In the middle of the circuit, just above the string of decoupling capacitors, is the pair of stores to display Q and X, notice that the clock for this is R3 or read CSR so they will only get updated if the processor reads CSR or if the repeat cycle sequencer does this as we will see later. To the right of these is the Repeat Cycle Sequencer itself, set in motion by R6 and W6, either of which clock the Mode store, IC22, which stores the state of BCS16 (selecting 8 or 16-bit mode) at the start of each cycle. R6 and W6 are individually presented to the Sequencer, PLS105 IC 33, after latching, together with MODE (8/16-bit) and START (cycle in progress). On seeing R6 or W6 in either mode, the Sequencer will either fetch or store a byte or two of data through outputs R0INT, R1INT, W0INT, W1INT, where R means read, W means write, 0 means low byte, 1 means middle byte and INT means internal origin, and can also trigger a new CAMAC cycle through W5INT.

The detailed sequences are as follows:-

16-bit Read Cycle repeat.

a) The 1331 is pre-loaded with Station number and subaddress. The personality card CSR may also be set for Q repeat (see later).

b) The Function Code is loaded, causing the first Read to be performed.

c) The data from this read is read out normally through low and middle byte registers.

d) The processor issues a 16-bit read at the repeat address (Base+12)

e) The data from this read is discarded since the repeat sequencer has only just started, but following that read it will have triggered a new read and fetched low and middle bytes into the 16-bit data buffer.

f) The processor now reads the repeat address as many times as it likes, getting 16 bits of data each time, and triggering a new CAMAC cycle each time until all the data has been collected.

g) If the Q repeat bit is set, then if the repeat sequencer does not see Q=1 when it reads the 1331s CSR, then it will trigger the same cycle again until it does, or until the FAIL timer (just below the sequencer) tells it "Time up". The FAIL timer counts the internal 10 MHz clock while IBUSY (internal busy) is true, having been cleared by either R6 or W6 (=RGO). Q repeat refers only to READ cycles.

8-bit Read Cycle Repeat.

The sequence is exactly as that above except that from d) onwards, the reads are 8-bit, and the repeat sequencer waits for two reads, passing first the low byte, then the middle byte before re-triggering the CAMAC cycle.

16-bit Write Cycle repeat.

a) The Station Number and Subaddress are loaded as before.

b) The low and middle bytes for the first write are loaded into the normal 8-bit registers.

c) The Function Code is written causing the first write to take place.

d) 16-bit writes to the repeat address will now cause the data written to be placed into the internal low and middle 8-bit registers, and the cycle re-triggered.

e) Step d) is repeated until all data has been written.

8-bit Write Cycle Repeat.

Exactly as above, except that two 8-bit writes are required at the repeat address, low byte first, before the CAMAC cycle is repeated.

Station 24 Sheet 2

This sheet shows the CAMAC Dataway Read and Write line buffers, with pull-up resistor packs, fed to and from their own sets of byte-wide bidirectional buses (RW1-8, RW9-16, RW17-24). These buses are connected to a local latch (LS374) and by a bidirectional buffer to the 1331's internal 8-bit data bus DATA0-7. Control of the latches and buffers comes from the PAL, IC10, which decodes the internal read and write commands and also monitors dataway activity to decide when to output and store as appropriate.

9.3 Station 25

The Circuit Diagram for Station 25 splits neatly into sections:

Top left	LAM Scanning, LAM Mask
Top right	Function Code Decoding, C,Z,I control, Interrupt Enable, Status Register
Bottom left	Station Number decoding and buffering, Subaddress output
Bottom right	ACB Arbitration, CAMAC cycle generation

Top left we see the L lines from the Dataway, buffered by IC's 4, 5 and 6 and fed to the multiplexers, IC's 7, 8 and 9 and to the ACB AL lines. When the 1331 is NOT in Stations 24 and 25, the buffers are turned OFF, so as not to see the Data on the Read and Write lines, by signal MAS. This signal is High, i.e. the buffers are Enabled, when the resistor packs are IN. When they are removed for use of the 1331 as an Auxiliary, MAS goes LOW, switching OFF the buffers and also disabling the N line decoders.

The AL signals are scanned in turn by the LS355 multiplexers, along with the Software LAM, SLAM, fed in as LAM 0. The open-collector outputs of the multiplexers are "Wire-ORed" together (pins 19), and pulled up by R9. The scanning of the multiplexers is controlled by the scan oscillator, IC18 (LS393), which is clocked by the master 10MHz clock. Each L line is therefore selected in turn and its state presented to IC25 pin 8. The scan address is also fed to the Mask RAM, IC19 (74S201), whose active low output is presented to IC25 pin 9. If IC25 pins 8 and 9 are ever both low together, that is to say the LAM is present and the Mask output is True, then the LSUM Latch IC39 pin 9 will be set high. This has two effects; first it causes an Interrupt, if Interrupts are enabled, because LSUM goes to Station 24 board for output as INTR; second, it stops the scan oscillator through IC 27, pins 13, 12, 11. The LAM Scanner is now "frozen", with its scan address pointing to the unMasked LAM.

The computer can read this address by reading ENCODED L (R4). This enables the buffer IC23, which outputs 5 bits of LAM scanner address plus three bits of switch data from SW1 A to C. We have not yet touched on the address multiplexers, IC's 16 and 17, which are normally selecting their B inputs in the absence of signal MT. This signal will be active LOW whenever Function code bits F64 or F128 are present, which denotes "Mask Twiddling", hence the name MT. When this takes place, the scan address becomes equal to the bottom 5 bits of the function code. The corresponding bit in the Mask RAM can thus be written to '0' or '1' and the state of both Mask RAM output and L line observed through reading the encoded L.

Writing to the Mask RAM works as follows:

On power-up, the Function Code latch IC22, top right, is cleared to ensure that MT is not true.

A burst of scan oscillator pulses QB is fed to the write (W) pin on the Mask RAM while the data is zero. (IC28 pins 3,2,1 write pulses; IC17 pin 13 to pin 12 for zero data). This clears all elements in the Mask RAM.

When either F64 or F128 is present, but NOT both (IC30 pin 11 conditions IC28 9,8,10), the pulse which strobes the Function Code decoder PROM, generated from W5, puts a Write pulse on pin 12 of the Mask RAM, writing the state of F64 into it on DIN (F PROM pulse IC49 pin 13, F64 to IC17 pin 14 to pin 12 to DIN on RAM).

Notice that the scan oscillator is stopped when MT is true, so after altering the mask one must send a Function Code less than 64 to free it, and also that the scan oscillator resets itself on 24, through IC30 pins 4,5,6, so that it scans 0 to 23 and back to 0 again.

Notice that reading the Encoded L with R4 generates a short reset pulse for the LSUM latch, freeing the scan oscillator. The LAM scanner will then search for another unMasked LAM. It will thus either go right the way round to the original LAM, or may find another. Scan time is 400nSec per LAM, i.e. 10 microseconds per complete scan. The purpose of the LSUM latch and the "release-scan" system is twofold:

To detect and hold "fleeting" LAMs

To allow an Interrupt service routine to find out not only which station caused the Interrupt, but also if any other modules, possibly higher priority ones, have requested service since the original request was made.

Bottom Left we see the N Store and its decoders, IC's 20 (store) and IC's 1, 2 and 3. The N Store is clocked by W4 and its output is enabled by AFGO, a version of Dataway BUSY. The N value from the store is fed to the decoders and also OUT onto the ACB EN lines while it is doing a CAMAC cycle. At all other times it accepts EN data from the ACB and feeds it to its decoders. Thus, if it is Master (Stations 24 and 25) then the 1331 will decode any valid ACB EN given to it. When it is not Master, the decoders are disabled anyway.

Just to the right of the N Store we see the Subaddress Store/Counter. This is normally simply loaded with the desired subaddress value which is output onto the Dataway as usual. If, however, the Software LAM is set (remember that it should be Masked OFF to avoid an Interrupt), then the Count Enable pin of the chip, pin 7, will be high allowing the End Pulse from the CAMAC cycle generator to increment the subaddress, provided, of course, that Switch 1D is open to enable IC43 pins 4,5,6. This is intended for applications where a lot of subaddresses need to be scanned in turn, for example a 16 channel ADC, to save having to reload the subaddress each time.

Top Right we see the Function Code latch, IC22, and its decoding PROM, IC26 "IBM V2". After the new F Code has been latched in, a 100nS pulse delayed by 100nS strobes the PROM via pin 15. The outputs of the PROM function as follows:

Function Code	Action	Result
0-7	pulse pin 2	generate READS2
16-23	pulse pin 1	generate WRITE
40-41	pulse pin 6	set or clear INTEN
48-49	pulse pin 4	set or clear SLAM
32-37	pulse pin 7	set/clear I, generate C/Z
0-31, 34-37	pulse pin 5	set START FF = CAMAC cycle

Notice how the flip-flops for READS2, WRITE, C and Z, set by the various pulses from the PROM are all knocked down by End Pulse from the CAMAC cycle generator. Note also that if either the C or the Z flip-flop is set, then NOBUSY is generated, IC45 pins 13,12,11, to inhibit all the A,F and N outputs.

At the bottom of this section of the circuit, on the right, we see the Q and X latches, which sample these lines at S1 time. The outputs of these latches go to the SR buffer (Status Register), IC24, whose outputs are enabled onto the Data Bus by R3.

Bottom Right we see the CAMAC cycle generator, set in motion as described above by the START signal, and clocked by the 10MHz master oscillator, IC40, RV1. The operation of this state machine is beyond the scope of this manual, but suffice it to say that it conforms to all the specifications of EUR6500, including aborting on ACL etc. and can operate in either R/G or ACL modes.

The monostable IC46 and flip-flop IC47 act to ensure that End Pulse is only generated on the trailing edge of a complete BUSY pulse, and therefore that ACL aborted cycles are ignored from the point of view in particular of resetting the START latch.

Also in this corner of the circuit is the power-on-reset system which generates active low and active high reset pulses for all parts of the circuit for about 200mSec after power-on and also in response to the front panel reset button and the reset line from the computer.

The rather complicated system of zener and transistor etc. ensures that even a brief interruption of the supply will be recognised and mal-operation avoided.

10. ACB Configuration Information

On the front of the 1331, there are three LEMO sockets, labelled REQUEST, GRANT IN and GRANT OUT. When constructing a multi-controller ACB system, very careful thought must go into the way that each device is included in the arbitration scheme which these sockets construct.

Some devices are very fast indeed and, if placed at the top of the arbitration heirachy, would effectively "lock" everybody else out. These devices, although they must be reasonably high in priority so as to achieve optimum throughput, must not be allowed to prevent other more important devices from performing essential control actions. These "more important" devices will usually be computer interfaces, which, although their access rate may be relatively slow, will nevertheless require to "get in" whenever they need to, in order to service Interrupts, for example.

When connecting up the Request/Grant chain, therefore, always remember to put the main computer interface if not first, then certainly second in line. The faster devices, although they may experience interruptions in their streams of activity, will be only slightly affected by the other devices doing their cycles.

The ACB cable at the back (the 40-way ribbon cable) connects REQUEST together for all ACB Controllers. Using the front panel LEMO sockets, the Highest Priority device then connects REQUEST to GRANT IN, then its GRANT OUT is connected to GRANT IN on the next lowest priority controller, then GRANT OUT on this to GRANT IN on the next, and so on. REQUEST is an open-collector output; GRANT IN is a pulled-up input; GRANT OUT is an open collector output, thus the wired-OR arbitration system is constructed.

11. Parts List and Assembly Details

11.1 Station 24

11.1.1 Integrated Circuits

Type	Qty	Component Reference
74LS02	1	IC29
74LS04	2	IC30,IC39
74LS08	3	IC19,IC31,IC32
74LS14	1	IC21
74LS74	2	IC11,IC22
74LS75	1	IC24
74LS123	1	IC23
74LS138	3	IC20,IC36,IC37
74LS157	1	IC17
74LS161	1	IC18
74LS240	3	IC1,IC2,IC3
74LS244	1	IC35
74LS245	4	IC13,IC14,IC15,IC25
74LS374	3	IC4,IC5,IC6
74LS393	1	IC12
74LS642A-1	3	IC7,IC8,IC9
74LS652	3	IC26,IC27,IC38
74ALS870	1	IC16
PAL22V10	2	IC10 "1331P10V" IC28 "1331P28V"
PLS105	1	IC33 "1331 V5"
75452	1	IC34

11.1.2 Discrete Semiconductors

1N5401	1	D1
TIL 209	14	LD1 - LD14 inc.

11.1.3 Passive Components

470R x 13 Res.Pk	2	RN2,RN4 (on sockets)
560R x 13 Res.Pk	2	RN1,RN3 (on sockets)
470R x 8 Res. Pk	1	RN5
560R x 8 Res. Pk	6	RN6,RN7,RN8,RN9,RN10,RN11 (on skts.)
470R	6	R4,R10,R11,R12,R13,R14
1K0	2	R1,R5
1K5	1	R6
2K2	1	R2
10K	3	R3,R7,R8
100K	1	R9
10pF cer.	1	C4
1n0 cer.	1	C7
10n0 cer.	1	C5
100nF cer.	11	C6,C8 - C17 inc.
10uF 25V tant.	1	C3
47uF 16V tant.	2	C1,C2

Station 24 Cont.

11.1.4 Miscellaneous

1 pole 8-way DIL switch	1	SW1
34-way rt. angle header	1	

11.2 Station 25

11.2.1 Integrated Circuits

Type	Qty	Component Reference
74LS00	2	IC27,IC43
74LS02	5	IC25,IC28,IC29,IC42,IC45
7404	1	IC44
74LS08	4	IC25A,IC30,IC41,IC50
74LS14	1	IC35
7438	5	IC11,IC13,IC14,IC15,IC31
74LS74	6	IC36,IC37,IC38,IC39,IC47,IC48
74LS75	1	IC34
74123	1	IC49
74LS123	2	IC46
74S124	1	IC40
74LS157	2	IC16,IC17
74LS161	1	IC21
N82S23N	4	IC1 (1100 NDA) IC2 (1100 NDB) IC3 (1100 NDC) IC26 (IBM V02)
74S201	1	IC19
74LS244	5	IC4,IC5,IC6,IC23,IC24
74LS273	1	IC22
74LS355	3	IC7,IC8,IC9
74LS374	1	IC20
74S374	1	IC32
74LS393	1	IC18
74LS620	1	IC10
75452	1	IC12
82S100	1	IC33 (1330)

11.2.2 Discrete Semiconductors

2N3704	1	TR1
1N5401	1	D1
BZY88C3V3	1	D2

Station 25 Cont.

11.2.3 Passive Components

560R x 8 SIL	10	RP1 - RP10 inc. (RP1-9 on sockets)
120R 0.25W	2	R19,R20 (on sockets)
220R	2	R6,R7
470R	1	R10
560R	2	R5,R8
1K0	7	R3,R4,R9,R15,R21,R22,R23
4K7	3	R16,R17,R18
10K	4	R11,R12,R13,R14
82K	1	R1
220K	1	R2
5K PRESET	1	RV1

10pF cer.	1	C7
33pF cer.	4	C8, C9 note: C6 not fitted
100pF cer.	1	C5
100nF cer.	12	"C"
1uF 35V tant.	1	C4
10uF 35V tant	1	C3
68uF 16V al.	2	C1,C2

11.2.4 Miscellaneous

PCB Mounted LEMO Socket	3	
34-way straight header	1	
4-way on/off DIL switch	1	
40-way rt. angle header	1	
2 amp Littelfuse	1	FS1

11.3 Module Assembly Parts

2-width module kit.
Front panel machined and engraved.
Rear panel machined.
TIL 209 LED wired to PCB Station 25 Qty 2.
Min push button, wired to Stn 25.

Note: Allow 10 inches of wire on connections of push button and Stn 25 LEDs to permit the module to be opened up for access.