TECHNICAL MANUAL FOR THE

HYTEC VME BUS MONITOR

AND SWITCH REGISTER

VDS2081

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C O N T E N T S

1.0 **PRODUCT SUMMARY**

The product consists of a single 6V Euro Card with both connectors fitted and operates as a D32/A16, A24 or A32 device. It can operate in three main modes:

(a) Direct data mode.
This mode merely continuously monitors the 32 data, the 31 address lines, the 6 address modifier (AM) lines, the Long Word (LW) signal and the Read/Write line and displays them. Any command addressed to the module in this mode will be ignored.

(b) Auto reply mode.
In this mode the module monitors the front panel switches and uses them as an address. If detected with any AM combination it will raise "DTACK" without any transfer of data. This mode is useful for keeping the system running if a device fails to reply. The front panel LEDs display the address/data combinations present during the last transfer. Again any command addressed to the module's unique address will be ignored.

(c) Normal Mode.
In this mode the LEDs again display the address/data combinations present during the last transfer. In addition the module will respond to its own unique 32 bit address set on its internal switches with five register read combinations and one write.

(1) A 32 bit internal register which can be written and read
(2) A 32 bit front panel switch register which can act as a source
(3) A 32 bit read of the last address not to this module
(4) A 32 bit read of the last data not to this module
(5) A 8 bit read of the AM/LW/W combination of the last transfer not addressed to this module.

In all the modes the +5V, +12V and –12V lines are monitored and a green LED illuminated if all are within tolerance.

In addition the module can provide both system clock and/or power–on reset if desired.

A front panel switch can also provide a system reset if operated.

Bus Error and System Reset are also monitored and the duration extended for front panel display.

2.0 **TECHNICAL DESCRIPTION**

2.1 Address Selection and Decoding.

The address lines (A1 – A31) and address modifiers (AMO–5) are passed to a set of Tx/Rx chips (LS651) which are selectable as straight through or via staticisers.

The chips invert the signals and drive the display LEDs directly via limiting resistors.

Shortly after receipt of 'DSA', the relevant staticisers are loaded by 'CLKA' produced by the second stage decoder PAL IC21.

The staticised address is compared to the switch address signals (SWAD1–31), by means of three F521 comparitors and a PAL (IC2) which produces the coded signals ME16 and ME32. The 'SWAD' signals are selected by the "AUTO REPLY" switch on the front panel and are derived either from the internal Base Address switches (SWA) or from the 32 data switches on the front panel.

The derived ME16 and ME32 signals are passed to IC21 which uses them together with the address modifiers and the 16/24 or 32 bit address selection to determine whether any action is required of the units.

If agreement is found the signal 'GO' is produced and passed to the selector PAL (IC26).

Regardless of whether 'GO' is produced or not, IC26 also produce a signal 'CLKD' following a delayed 'DSA', if the command is a write or coincident with 'DTACK' if not, this copies the 32–bit data from the VME Bus into the data Tx/Rx chips staticisers.

2.2 Data Display and Selection

The data display, like the address is driven directly off the Tx/Rx chips staticisers loaded as indicated in 2.1. If the transfer is to or from this module or not, the data on the internal data bus is continuously displayed.

If 'GO' has been generated the data on the internal bus is supplied either from the VME Bus if a 'WRITE' or from one of five registers in the unit if a 'READ'.

These registers are:

(a) The front panel switches, these are selected if the signal 'RDSWS' is produced by IC26.

(b) The 'B' register which is located in the opposite direction of the Data Tx/Rx chips. This may be Read or Written by the selection of 'SEEB' or 'LDB' from IC26.

(c) The Last Address Register (IC18). This register is loaded at 'DTACK' time by 'COPY D/A' if the 'GO' signal has not been produced, indicating a transfer elsewhere.

(d) The Last Data Register (IC1). Loaded as (c).

(e) The Last AM Register (IC48). Loaded as (c).

2.3 Control

Control is achieved mainly by IC26 which takes the ’GO’ together with a delayed version and the lower address bits BA1–4, to produce gating signals RDSWS, RDDATA, RDAM, RDADD, SEEB and LDB.

Finally, after the delay, ’MYACK’ is produced which is maintained on the VME BUS as ’DTACK’ until DS0 and DS1 have both been removed by the controlling unit.

If ’AUTOREPLY’ is set only ’DTACK’ is produced with no gating signals and hence no data is transferred.

2.4 Voltage Monitoring

Voltage Monitoring is carried out by means of a TEXAS TL7770 chip which monitors the +5V and the two 12V lines. If within tolerance a green LED is illuminated.

2.5 System Clock

The unit may be selected to provide system clock by connecting a 16MHz oscillator chip via a link and buffer to the bus.

2.6 System Reset

At power–up the unit is held reset for approximately 500mS. This signal may be selected to give ’bus reset’ via a link and buffer. In addition operation of the front panel ’RST’ switch gives a 50mS signal pulse unconditionally to the Bus. The switch must be returned left to re–use. A monostable and LED gives a 100mS pulse if reset occurs on the bus from any source.

3.0 **OPERATING SETTINGS FOR VDS2081**

1. To select unit to provide system reset

   CONNECT: LK1: 1–2

2. To select unit to provide system clock

   CONNECT: LK2: 2–3

3. To select direct bus monitoring;

   MOVE SWITCH ”DD” TO RIGHT

   NB: This mode overrides all other functions.

4. To select normal display mode:

   MOVE SWITCH ”DD” TO LEFT

   NB: This mode displays address and data relative to the last bus transaction. Move Move switch ”AM” to right to display AM, LW and RD.

5. To select auto reply mode:

   MOVE SWITCH ”AR” TO RIGHT

   Set front panel switches 4–31 to the 16 byte group address which is required to reply.

   Unit will then produce ”DTACK” for any combinations of bits 0–3 using bit 4–31 as a base address.

   NB: This mode overrides register operation.

6. To select register operation:

   Set Unit to 16, 24 or 32 bit address as follows:

   16 bit LK3: 1–2, LK4: 2–3
   24 bit LK3: 2–3, LK4: 1–2
   32 bit LK3: 1–2, LK4: 1–2

   Set base address ”HEX” switches as full 32 bit address ignoring bits 0–3.

Unit will then respond as follows:

BASE ADDRESS	ADDRESS MODIFIER
16 BIT 24 BIT 32 BIT	29 OR 2D 39 OR 3D 09 OR 0D

OFF SET (BITS Ø–4)	READ	WRITE
Ø 2	32 BIT F.P. SWITCHES 32 BIT F.P. SWITCHES	D.TACK ONLY D.TACK ONLY
4 6	32 BIT ’B’ REGISTER 32 BIT ’B’ REGISTER	32 BIT ’B’ REGISTER 32 BIT ’B’ REGISTER
8 A	32 BIT LAST ADDRESS 32 BIT LAST ADDRESS	D.TACK ONLY D.TACK ONLY
C E	32 BIT LAST DATA 32 BIT LAST DATA	D.TACK ONLY D.TACK ONLY
10 12	8 BIT LAST AM 8 BIT LAST AM	D.TACK ONLY D.TACK ONLY
14 TO 1F	D.TACK ONLY	D.TACK ONLY

N.B. BITØ = ODD BYTE IS IGNORED
BIT 1 = 16 BIT IS IGNORED.