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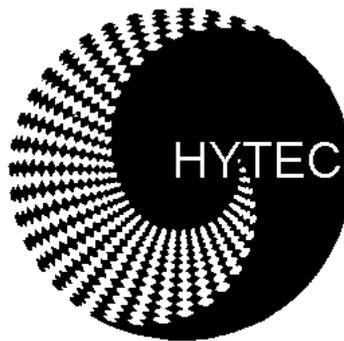
GPS2092 User Guide

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HYTEC VME GPS2092 PRECISION TIME-STAMP MODULE

1.   Introduction

The GPS2092 is a single-width VME module which uses signals received from an external antenna to produce accurate time and position information readable from VME. It uses a 68EC030 processor and 68882 co-processor to process 1PPS (one pulse-per-second) and event pulses to provide this information through a dual-ported RAM memory. This manual is for the first version of the unit, which uses a Motorola M12 Timing GPS engine.

The unit is normally supplied complete with a suitable active patch antenna (see later sections) and should be installed in a standard VME crate with forced air cooling.

2.   Preparation

Before installing the module in the VME crate, make sure the internal settings are as required. These are as follows:-

2.1   Baud Rate Setting

On the card, there is a four-pole DIL switch, SW2, which sets the baud rate for *both* serial ports, that is the front panel RS232 port and the serial data connection to the GPS engine. Since the baud rate to the GPS engine is fixed at 9600 baud, these switches must be left as delivered:

SW2-1 (front) = ON   SW2-2 = ON   SW2-3 = ON   SW2-4 (back) = OFF
(Front means nearest the front panel).

NOTE: in order to avoid confusion, later units of this type are delivered with the baud rate hard-wired to 9600 baud.

The front panel RS232 port must always, therefore, be connected at 9600 baud. The data format is 8 data bits, no parity, 1 stop bit. The pinout of the connector is as follows:-

Pin 1   GND   Pin 2   TX DATA   Pin 3   RX DATA   [Data IN to GPS module]

2.2   VME Base Address Setting

SW1 sets the card's base address in A16 Short Addressing space (address modifiers 29 and 2D HEX). It is a rotary HEX switch whose value is compared to address lines A15-A12 inclusive. When set to '7' for example, it therefore sets the base address to HEX 7000.

The card occupies 4 K bytes of A16 space starting at this address; the first 2K bytes (A11 = '0') are for on-board registers and the second 2K bytes (A11 = '1') are for the dual-ported memory.

2.3 VME IRQ Selection

Jumpers JP1 and JP2 are used to select the VME interrupt line that the card will use. You may select from IRQ4-IRQ7 inclusive. The selection is made as follows:

IRQ	JP1	JP2
4	IN	IN
5	IN	OUT
6	OUT	IN
7	OUT	OUT

2.4 Antenna Power Supply Voltage Selection

Jumpers JP3 and JP4 are used to select either 3.0 volts or 5.0 volts as the power supply for the GPS antenna. This is normally set at manufacture for the antenna supplied and should not be changed.

2.5 Clock Delay Setting

Jumpers JP5 – JP9 are used to select a delayed 50MHz clock signal for timing the hardware input pulses so that they latch the high-speed counter at the correct point. The default setting is JP6 IN, all others OUT, and this should not be changed.

2.6 Active Edge Selection

JP9 and JP10 select the active edge of the **EVENT** and **FAST CLEAR** inputs respectively. Each jumper consists of three pins, pin 1 identified by a square PCB pad, nearest the back of the module, pin 2 in the centre and pin 3 nearest the front panel of the module. Joining pins 1 and 2 of the relevant jumper selects the rising edge of the input, joining pins 2 and 3 selects the falling edge. The selected edge sets an interrupt flag for the processor and, in the case of the event input, stores the state of the internal counter for event timing purposes. 'Rising' and 'Falling' refer to the input in TTL level terms, where 'rising' means going from a TTL low to a TTL high.

It is possible to select NIM input signal levels by adjusting potentiometers (see below) but the direction of signal movement remains the same; so selecting the rising edge with a NIM input would mean looking for a transition **to** a less negative voltage, e.g. from -0.8 volts to 0 volts.

At manufacture, both JP9 and JP10 are fitted 1-2 rising edge.

2.7   Signal level selection.

R32 and R28 adjust the threshold for high-speed comparators that condition the FAST CLEAR and EVENT inputs respectively. The range of adjustment is from -1V to +1V. At manufacture, both are set to +1V, for TTL signals. Note that both inputs are fitted with 50-ohm termination resistors to ground.

To Adjust, proceed as follows:-

Event Input: monitor IC 37 pin 3 with a digital voltmeter and adjust with R28 to the desired value.
Fast Clear Input: monitor IC 41 pin 3 and adjust with R32 to the desired value.

2.8   RS232 Data Path Selection.

JP 11 and JP 12 are new jumpers fitted on issue 2.0 boards and are used to route the RS232 data communications from the GPS engine to the front-panel diagnostic port for use with an external PC running WINONCORE12, a package which allows fine tuning of the GPS installation not available through the firmware.

To use this feature, move JP11 and JP12 from their default position, which is '2-3', to position '1-2'. Remember to move these back once you have finished with this mode!

Note that when these jumpers are in the 'alternate' position, the on-board micro still receives GPS messages and will operate normally.

2.9   Using WINONCORE12

Having downloaded the file GPSOC.EXE (available from Hytec or a variety of free download sites on the Internet), run it to install the package on your PC. Then connect one of your PC's serial ports (COM1 is best) to the front panel diagnostic port on the GPS2092. Next, start WINONCORE12 and switch on the VME crate. If the small green LED along the bottom bar of the WINONCORE12 window starts flashing, the package has established communications and you can then select a variety of display windows to see progress on acquiring satellites and getting a position fix. The best windows are 'SIGNAL QUALITY' and 'NAVIGATION'.

The signal quality window shows you which satellites are in view and being tracked and the navigation window tells you if a good position fix has been obtained.

Also, along the top bar, is a button called 'SURVEY'. If you click this button after the engine has got a good fix – the NAVIGATION window will tell you if a 3D fix has been obtained.

Once the survey has been completed (about three hours) the engine will enter 'position hold mode' and give more precise timing information. It will also remember this selection through power cycles, since battery backup is provided by the 2092.

3.   Connecting Up.

The VME GPS2092 module can now be connected up to its antenna [MMCX subminiature connector] and any signal inputs. The antenna should be connected and, if necessary, disconnected with the power switched off to avoid any damage to the unit. The antenna supplied, will normally be an active 26dB patch antenna for surface mounting, together with the necessary cable. Excessive cable length should be avoided and the antenna position is quite important:

3.1   Antenna Position. The antenna should be mounted 'on its back', that is facing the sky [the surface opposite the mounting face is the active face] and with a clear view of the sky in all directions. Trees and buildings are barriers to the signal and should be avoided. A clear view right down to 40 degrees above the horizon in all directions is ideal.

4.   Setting to Work.

With the antenna in position and connected up, the power can be switched on.

When the unit is first switched on, it is advisable to have a diagnostic terminal connected to the front panel port so that operation of the unit can be observed.

Connect a terminal such as a VT100 or a PC running a terminal emulation program such as Hyperterminal to the diagnostic port on the front of the unit. Set the terminal to 9600 baud, 8 data bits, one stop bit, no parity. The connections for this terminal are:

Pin 1   ground
Pin 2   TX DATA   (from GPS92 to terminal)
Pin 3   RX DATA.

The front panel LEDs should show "TRACKING" ON and all the others OFF. The message "Looking for a satellite......." should be displayed on the terminal, followed at regular intervals by further messages saying that it is still looking.

The green **"1PPS" LED** will also be flashing to confirm the GPS engine is OK.

This goes on until the GPS engine has established where in the world it is, what the time is, and which satellites it can track. When the unit is first switched on, the unit will obviously need to do a full survey and this can take up to 30 minutes. Once the GPS engine has acquired a satellite, this is reported on the screen; further satellites will then be acquired.

Note that until the GPS engine has acquired three satellites, no position information can be output on the diagnostic terminal and no event pulses will be accepted.

At this point you can press <RETURN> on the terminal and the unit will respond with time information and details of satellites being tracked. In this initial version of the firmware, that is all you can do from the terminal, although other commands will be added later.

5.   Problems Getting Started

If the unit fails to see a satellite within 30 minutes or so, then there is probably a problem with the antenna. Check the cable connections and the antenna position, make sure there is no water in any of the connectors. Try also pressing the front panel RESET button to restart the processor.

6.   Using the Module

The primary purpose of this module is to provide accurate time stamp values for external events. The Event input on the front panel stores a 50MHz count value in an internal latch and interrupts the processor. From this value and the value of a similar latch, which stored the count on the last 1PPS (Pulse-Per-Second) pulse from the GPS engine, the processor works out the exact UTC (Universal Coordinated Time) time of the event. This is then stored in the Dual-Ported Memory, accessible via VME.

The Event Input - size 00 LEMO socket - is terminated in 50 ohms and, as we have seen above, can be a TTL signal or a negative signal such as NIM.

The other input on the front panel is Fast Clear, which is the same type as Event, i.e. TTL or NIM into 50 ohms- size 00 LEMO socket, which causes the processor to abort the last event calculation and prepare for the next.

There is one size 00 LEMO socket output on the front panel and this is called 1PPS. This is a high-powered TTL signal 2 microseconds wide whose leading edge is derived from the GPS engine 1PPS output, which is normally within 100 nanoseconds of UTC 1PPS. An LED next to this shows a stretched version of this pulse.

In a typical application, the event input will be connected to some external trigger signal, which will cause the time to be stored. The maximum rate at which this input can pulse has been found by experiment to be approximately 3KHz.

When an Event pulse has been received and the calculated time put in the Dual-Ported RAM, the processor will attempt to set the GPS module's Interrupt output. It will succeed if the Interrupt Enable bit has been set in the module's Control And Status Register.

REMEMBER that this module will evaluate the time of an event pulse at the front panel and put the data into the dual-ported memory, but the firmware is not designed to operate this unit as a "Real-Time Clock", that is it won't keep an updated time in the memory for you. If that is the intended application, you will need to put pulses into the event input in order to get it to update the time. You can use the 1PPS output for this if you wish, or supply an external 1-2KHz signal for the purpose. Don't forget that the input is 50 ohms to ground so you will need a line-driving type TTL signal.

7.   VME Addressing.

The module is equipped with a complete set of VME registers in A16 (short addressing) space, in line with Hytec's standard scheme which is modelled on the VXI Configuration Register set.

This register set comprises the following:-

a)   An ID register, indicating manufacturer and type.
b)   A vector register, for programming interrupt acknowledge data.
c)   A Model Code register, showing 2092 decimal, the unit's type no.
d)   A Control and Status Register through which the unit is controlled and monitored.

8.   VME Interface - Full Register Set Description

All registers in this module should be accessed in 16-bit mode; that is they are all D16 compatible.

Running through our 'Overview' list (sect. 7), the following is a full description of the format and function of each register.

Item   Name   Offset from Base Address (HEX)

a)/b)   ID/Vector   + 00h

The ID register and Vector register are at the same address. You read the ID and write the vector. The Vector can be read back for diagnostic purposes at offset 0Ch.

Reading the ID gives HEX FF7F, where 'F7F' on bits 0-11 is Hytec's unique VXI identifier, and 'F' on bits 12-15 means that this unit is A16 register based only.

Writing an 8-bit number to this location (D0-D7) stores a vector with which it will respond during interrupt acknowledge cycles.

c)   Model Code + 02h

This simply shows the unit's Hytec catalogue number, which is 2092 decimal.

d)   Control and Status Register + 04h

This is a 16-bit register (CSR for short) through which the card is controlled and its status observed.

It implements first a BUSY flagging system which can be used to implement a booking scheme. In addition to this, there are several 'fixed' bits, which derive from the VXI spec. and then the following:-

i) Interrupt Enable - one bit to enable IFLAG bit - set by the output of the event processing logic - as an interrupt source.

ii) Two bits, ISEL1 (JP2) and ISEL2 (JP1) which are read only and show the state of the IRQ line jumpers for selecting which IRQ line to drive and which level of interrupt acknowledge to respond to (see section 2.3). '1' = Jumper OUT.

Other bits are described in more detail below.

Control and Status Register Format

The format of this register is as follows:-

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	1	0	0	0	0	IFLAG	SP.	INTEN	ISEL2	ISEL1	READY	1	1	0	BUSY/RST

BUSY/RST: Writing a '1' to this bit resets the VME Register logic. When reading, on the first read after a power-up or a RESET, this bit will be seen as '0'. Subsequent reads will show this bit as '1', meaning BUSY. Bit 4, READY, is the inverse of the state of this bit and is read only.

ISEL2,1 (read only): These two bits show the state of the two interrupt select jumpers, JP1 and JP2, which select the IRQ level that the card will drive and respond to with its interrupt acknowledge vector.

INTEN (write/read): This bit enables the IRQ output of the board for the event completion logic. '1' = enabled.

IFLAG (read/clear): This shows the state of the internal logic flag which is set by the processor every time is completes the processing of an event pulse and has put new data in the dual-ported RAM. It is cleared by writing a '1' to this bit (RORA Protocol) – see note below.

SP (write/read) A spare writeable and readable CSR bit for future use.

Other bits: '1' means always read as '1', writing has no effect; '0' means always read as '0'.

Note: Remember that when you write to the CSR, for example to knock down the interrupt flag bit, that you must include the interrupt enable bit, if it was set. You must also beware of writing a '1' to bit 0, the reset bit, since if you read the CSR and then decide to use this data to 'include' other bits to restore them when clearing the IFLAG bit, you would naturally include the BUSY bit, bit 1 in this operation.

Dual-Ported RAM DATA FORMAT:-

Offset	NAME	BIT(s)	CONTENTS
0	Time_1	0-15	Low 16 bits of 10 nanosecond increments into second.
2	Time_2	0-10	High 11 bits of 10 nanosecond increments [27 bits total]
		11-15	Low 5 bits of seconds into day.
4	Time_3	0-11	High 12 bits of seconds into day [17 bits total]
		12-15	Low 4 bits of day into year.
6	Time_4	0-4	High 5 bits of day into year [9 bits total]
		5-9	5 bits of year starting from 1996 (0=1996)
		10	1 bit status = scheduled satellite visible?
		11-13	3 bits of number of satellites visible
		14-15	2 bits of navigation mode:-
			0=normal precision, 1=high precision,
			2=determining position, 3=no satellites visible.

NOTE: Pages at Offsets 8-E are not supported in the current firmware version.

Offset	NAME	BIT(s)	CONTENTS
8	Status_1	0-15	Low 16 bits of next satellite changeover time in seconds
A	Status_2	0	High bit of changeover time [17 bits total]
		1-5	5 bits of PRN (satellite number) of currently viewed satellite
		6-9	4 bits of current schedule entry number
		10	1 bit of "Position Known?" '1' = 'yes'.
C	PRN_1	0-4	PRN of first visible satellite,
		5-9	PRN of second visible satellite
		10-14	PRN of third visible satellite.
E	PRN_2	0-4	PRN of fourth visible satellite,
		5-9	PRN of fifth visible satellite
		10-14	PRN of sixth visible satellite.
10	Position_1	0-6	7 bits of Latitude degrees
		7-12	6 bits of Latitude minutes
		13-15	Low 3 bits of fraction of a minute of Latitude.
12	Position_2	0-6	High 7 bits of fraction of a minute of Latitude (thousandths).
		7	North/South flag bit – '1' = North.
		8-15	8 bits of Longitude in degrees.
14	Position_3	0-5	6 bits of Longitude minutes,
		6-15	10 bits of fraction of a minute of Longitude (thousandths).
16	Position_4	0	One bit East/West flag – '1' = East.
		1-12	12 bits of Altitude in metres,
		13	One bit flag for above/below sea level – '1' = above.

8.   Suggested Operating Sequence

For time information only this will be the data words at offsets 0 to 6 and the data within will then be extracted and formatted.