# HYTEC SP 232N

# RS 232C COMMUNICATIONS UNIT

# TECHNICAL MANUAL

&

# PROGRAMMING INSTRUCTIONS

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# 1. MODULE DESCRIPTION

The HYTEC SP 232N is a single width CAMAC module designed to interface external devices and systems using an RS232C interface in full duplex mode.

Features of the module are:-

1. Compatible with NE9047 and previous Hytec SP232 modules.
2. Two separate 256 byte buffers for transmitted and received data.
3. Full LAM structure for read, write and error handling.
4. Switched crystal-controlled baud rates from 300 to 38400 Baud.
5. Use of repeat-mode Q response for both read and write data.
6. Selection of word length and parity mode via a control register.
7. Selection of one or two stop bits via an on-board switch.
8. Additional control register for fully program-controlled operation.

# 2. SPECIFICATION

## 2.1 MECHANICAL SPECIFICATION

Single-width CAMAC module with a 25 way Cannon front panel socket.

## 2.2 TEMPERATURE RANGE

Operating temperature from 0 to +45 degrees C.

## 2.3 POWER REQUIREMENTS

+6V @ 1600 mA

## 2.4 FRONT PANEL CONNECTOR

Type:- Cannon DB25S
Mating Connector - Cannon DB25P

Pin Allocation:

| | | |
|---|---|---|
| Pin | 2 | RX DATA |
| | 3 | TX DATA |
| | 7 | GROUND |
| | 4 | REQUEST TO SEND OUTPUT – NOT NORMALLY USED |
| | 5 | CLEAR TO SEND INPUT – NOT NORMALLY USED |

## 2.5 FRONT PANEL INDICATORS

| | |
|---|---|
| TXGO | Green LED indicates TX path activity |
| RXGO | Green LED indicates RX path activity |
| EVEN | Red LED shows EVEN parity selected |
| P-EN | Red LED shows PARITY enabled |
| NB2 | )Red LED's show number of bits per character in conjunction with NB1 |
| NB1 | )see section 2.7 |
| SBITS | Red LED shows number of stop bits selected - ON= 2 stop bits; OFF=1 stop bit |
| SP3 | ) |
| SP2 | )Red LED's show speed selected – see table below |
| SP1 | ) |

## 2.6 USE OF THE CAMAC DATAWAY

Sub Address 0 or 15: A(0) + A(15) (Overall)

- F(1) Read Control Register 1
- F(8) Test LAM. Q response is generated if any LAM request is set.
- F(9) Reset: clear the FIFO stores and the receiver/transmitter circuits.
- F(17) Overwrite Control Register 1.

Sub Address 1: A(1) (Receiver)

- F(0) Command included for backward compatibility only – use F(2) instead.
- F(2) Read data and shift the next byte out. Clear LAM status bit 1 if set. This will be re-asserted if any more data is present in the RX FIFO. Q response is generated when data is present and valid.

Sub Address 2: A(2) (Transmitter)

- F(16) Overwrite data to be transmitted. Q response is generated if the data is accepted. Clear status bit 2 if set. This will be reasserted if the buffer FIFO is not full.

Sub Address 3: A(3) Control Register 2

- F(1) Read Control Register 2
- F(17) Overwrite Control Register 2

Sub Address 12: A(12) (LAM Status)

- F(1) Read LAM status
- F(11) Clear LAM status
- F(19) Selective set LAM status
- F(23) Selective clear LAM status

Sub Address 13: A(13) (LAM Mask)

- F(1) Read LAM mask
- F(11) Clear LAM mask
- F(19) Selective set LAM mask
- F(23) Selective clear LAM mask

Sub Address 14: A(14) (LAM REQUEST)

F(1) READ LAM Request Register

## 2.7 DATA AND REGISTER FORMATS

Transmitted Data

W8 W7 W6 W5 W4 W3 W2 W1 [A(2)F(16): Q='1' if not full]

MS LS

The number of bits active in the byte depends on the selected word length

Received Data

R8 R7 R6 R5 R4 R3 R2 R1 [A(1)F(2): Q='1' if data valid]

MS LS

The number of bits active in the byte depends on the selected word length.

Control Register 1 Data

| | |
|---|---|
| W6 W5 W4 W3 W2 W1 | A(0)F(17) |
| R6 R5 R4 R3 R2 R1 | A(0)F(1) |

Bit 1 - Not used

Bit 2 - Not used

Bit 3 - Parity - When '0' the parity bit is not generated and the most significant bit is determined by the data. When '1', parity is generated, sense selected by bit 4.

Bit 4 - Even Parity - Determines the parity sense generated and checked - '1' = even, '0' = odd.

| | | | |
|---|---|---|---|
| Bit 5 - Bit 6 | Number of bits per character - State | 00 - 8 bits | Display: NB2, NB1 =ON ON |
| | | 01 - 7 bits | Display: NB2, NB1 =ON OFF |
| | | 10 - 6 bits | Display: NB2, NB1 =OFF ON |
| | | 11 - 5 bits | Display: NB2, NB1 =OFF OFF |

Control Register 2 Data

| | |
|---|---|
| W8 W7 W6 W5 W4 W3 W2 W1 | A(3)F(17) |
| R8 R7 R6 R5 R4 R3 R2 R1 | A(3)F(1) |

Bit 8 '1' means dataway control of speed and number of stop bits: '0' means switch control.

Bit 7 '1' selects internal loopback of TX to RX data– test mode only.

Bit 6 '1' selects split data rate: TX controlled by dataway; RX controlled by switches.

Control Register 2 Data (continued)

Bit 5 Not used

Bit 4 Number of stop bits if bit 8 = '1':'1' means 2 stop bits; '0' means 1 stop bit.

Bits 3,2,1 Control TX/RX speed if bit 8 = '1' Function is the same as for the switches, i.e '111' is 38400 baud; '101' is 9600 baud etc.

Note: When bit 8 is '0', bits 1-4 of this register show the state of the switch selections.

LAM Mask

W3 W2 W1 [A(13)(F(19)+F(23))]
R3 R2 R1 [A(13) F(1)]

Bit 1 - RX FIFO LAM Mask

Bit 2 - TX FIFO LAM Mask

Bit 3 - Error LAM Mask

LAM Status

W5 W4 W3 W2 W1 [A(12)F(19) + F(23)]
R5 R4 R3 R2 R1 [A(12)F(1)]

Bit 1 - The RX FIFO is not empty

Bit 2 - The write buffer is not full. There are less than 256 characters in the Write FIFO store.

Bit 3 - Parity Error - A parity error has been detected in the last character received.

Bit 4 - Framing Error - the last character received had no valid stop bit.

Bit 5 - Overrun error.

LAM Request

R3 R2 R1 [A(14) F(1)]

Bit 1 - Read buffer not empty – RX Data to be read.

Bit 2 - Write buffer not full – i.e. space for TX data.

Bit 3 - Error condition received from the incoming data check circuit. This is an OR condition of status bits 3, 4 & 5

Use of Control Signals

'Z' Initialise: Clears the control register, the Read and Write FIFOs, together with LAM mask and status.

C & I Not used

Use of Status Signals

'L' (LAM) Generated for any LAM request. Inhibited by N.

'Q' Q response - Generated for A(1)F(2) when data is ready.
Generated for A(2) F(16) when data is accepted.
Generated for (A(0) + A(15)) F(8) when LAM is set.

'X' Command Accepted - Generated for all Dataway commands which can be executed by the module.

## 3 OPERATION

### 3.1 BAUD RATE SELECTION

The operating baud rate is selected by elements 1, 2 and 3 of dual-in-line switch SW1.

| SW1/1 | SW1/2 | SW1/3 | Baud Rate |
|---|---|---|---|
| ON | ON | ON | 38400 |
| ON | ON | OFF | 19200 |
| ON | OFF | ON | 9600 |
| ON | OFF | OFF | 4800 |
| OFF | ON | ON | 2400 |
| OFF | ON | OFF | 1200 |
| OFF | OFF | ON | 600 |
| OFF | OFF | OFF | 300 |

The state of these bits can be observed through bits 1-3 of Control Register 2 if dataway control is not selected (Control Register 2 bit 8='0'). Switch element ON=corresponding bit = '1'

### 3.2 STOP BIT SELECTION

SW1 element 4 controls the number of stop bits generated and expected by the module. ON=2 stop bits: OFF=1 stop bit. The state of this bit can be observed in bit 4 of Control Register 2 if dataway control is not selected (Control register 2 bit 8='0').

# 4. INSTALLATION

Set the internal switches as desired, unless dataway control is to be used, and plug the module into any normal station of the CAMAC crate. Switch on the power supplies when the module has been inserted.

## 4.1 INITIALISATION

The module is initialised by the use of a Z cycle or a clear command: F(9)A(0) or A(15). As soon as this command is sent the module will be ready to receive and send data. The FIFO's, UART, control registers, mask register and status register will all be cleared. At power-on or after one of these commands, the module defaults to "NE9047 Compatibility Mode" and will be software compatible with previous versions of these units supplied by Hytec Electronics Ltd.

# 5. PROGRAMMING

## 5.1 CONTROL REGISTER 1

Control Register 1, the 'original' control register, is initialised to the normally used state i.e. no parity and 8 bit characters. The number of stop bits in the transmitted or received character is determined by SW1 element 4 and not by a control bit. The control register may be overwritten by function code 17 on sub-address 0 or 15 with bits 3 to 6. The register is read using function code 1, again at either sub-address. The contents of the register are read via R1 to R6.

Other modes of operation may be programmed by use of Control Register 1 as described under Control Register 1 data.

## 5.2 WRITING DATA TO BE TRANSMITTED

Data to be transmitted is written via sub-address 2 using function code 16. Use of Q response can be made to test if the module has accepted the character or not. If Q is generated in response to A(2)F(16) then the module has accepted the Write data. The module can accept 256 characters before failing to send a Q response. These characters may be overwritten at the maximum dataway speed.

The module may be operated in this write-and-test-for-Q mode or in conjunction with the Write LAM status.

The character length is determined by bits 5 and 6 of the control register. If parity is enabled, the most significant bit of the character transmitted will be forced to the parity sense.

## 5.3 READING DATA RECEIVED

Data received is read via sub-address 1 using function code 2. Provided the Read FIFO is not empty a Q response will be generated when the data is read. Function code 2 reads the data and shifts the next character to the output of the FIFO. Thus Q-repeat mode may be used independent from or in conjunction with Read LAM status.

Character length and parity are again controlled using the same bits in the control register as used for transmitted data.

## 5.4 LAM HANDLING

Three LAM requests (Read, Write and Error) are enabled by the settings of three mask bits. The error status consists of three bits read via R3 to R5 and these indicate parity error, framing error and overrun error. The logical OR of these three status bits produces the 'error' bit which appears as bit 3 in the LAM Request Register if the error mask, bit 3, is set.

The mask bits may be selectively set using A(13)F(19) and selectively cleared using A(13)F(23) and Write data bits W1 to W3.

## 5.5 READ LAM

The Read LAM (Bit 1) will be set on receipt of a single character transferred to the RX FIFO.

## 5.6 WRITE LAM

The Write LAM or Transmit LAM will be set whenever there is space in the transmit FIFO.