LEEDS PATTERN TRIGGER MODULE,

HYTEC TYPE 238

USER GUIDE AND OPERATIONAL NOTES
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Introduction

The purpose of this module is to detect patterns of adjacent 'hit' pulses from a hexagonal array of detectors, essentially to eliminate the effect of random noise hits.

To achieve this, the module accepts 59 differential ECL inputs at the front panel, split internally into five overlapping 'patches' of 19 inputs each, and detects multiple adjacent pulsed logic states in each patch individually by a majority logic comparator and a memory look-up [the comparator says "more than ‘n’ bits present", the memory look-up says "interesting pattern", i.e. adjacent].

The inputs are connected by two front-panel 60-way IDC headers, 30 pairs on the upper connector and the remaining 29 on the lower. One extra input is present, and is available as an alternative source for the Fast Clear input, selected by wire link on the PCB.

Also on the front panel is a single-pole LEMO socket for a NIM level input to act as a Fast Clear signal.

On the rear panel is a position for a further IDC connector, providing scaling outputs for external logic and allowing forcing inputs to be accepted to override decisions made by the majority logic. Other signals on this connector provide a common VETO line, a Broadcast Clear/Enable line and an overall Trigger Output [for a readout controller].

The CAMAC port of this unit provides full access to all internal functions.

CAMAC Port

The function of the CAMAC port is as follows:-

Command	Purpose	Use of R/W lines	Q, X notes
F(0) A(0)	Read Patch memories at Pointer Address:- (Pointer incremented after operation)	R1-5 = Patch 1-5 'Q'	
F(1) A(1)	Read Memory Address Pointer	R1-19	
F(1) A(12)	Read Patch Flag Status	R1-5 = Patch 1-5 Flag	
F(2) A(0)	Read Detected Trigger Pattern	R1-19 = Patch Data R20-24 = Patch ID	Q=’1 = valid
F(16) A(0)	Write Patch Memories at Pointer Address:- (Pointer incremented after operation)	W1-5 = Patch 1-5 'Data'	

CAMAC Port, continued.

F(17) A(0)	Write Reference Setting	W1-5
F(17) A(1)	Write Memory Address Pointer	W1-19
F(24) A(0)	Disable Patch 1	None
F(24) A(1)	Disable Patch 2	None
F(24) A(2)	Disable Patch 3	None
F(24) A(3)	Disable Patch 4	None
F(24) A(4)	Disable Patch 5	None
F(25) A(15)	Reset; Clear all Patch Flags, Disable all patches, clear Memory Address Pointer.	
F(26) A(0)	Enable Patch 1	None
F(26) A(1)	Enable Patch 2	None
F(26) A(2)	Enable Patch 3	None
F(26) A(3)	Enable Patch 4	None
F(26) A(4)	Enable Patch 5	None
F(26) A(15)	Global Enable - Permit Patch Flags to generate LAMs, 'ARM'.	

Unaddressed Commands:- Z.S2 has the same effect as F(25) A(15).

Notes on CAMAC commands.

All commands produce the 'Command Accepted' response. X='1'.
F(2) A(0) produces a Q='1' response if the patch data being read is valid.

Comparator Reference operation:-

The comparator reference setting is applied to a 5-bit complementary binary DAC whose reference input is set at 1.2 volts. Thus each bit corresponds to 37.5 millivolts. Please note that the reference setting is no longer readable.

These values correspond to actual input majority as follows:-

Code Written	reference voltage (typical measured)
11111	0.015
11110	0.053
11101	0.091
11011	0.173
10111	0.325
01111	0.632
00000	1.190

Programming Procedure.

Command sequence:-

1) Give the module a RESET command F(25) A(15) to ensure it is inactive.

2) Now load up the patch memories by first writing the pointer to zero with F(17) A(1), then write consecutive data to each location specifying 0/1 for each patch. The pointer auto-increments; bit W1 corresponds to patch 1 and so on to W5; writing CAMAC '0' means ignore this patch pattern (address), '1' means store the data if this pattern appears.

3) Write the comparator reference value with F(17) A(0) to select the number of bits required to trigger.
4) Enable each of the patches (to allow its flag to be set) with F(26) A(0-4).

5) At this point, any input pulses will be captured if they satisfy the majority logic comparator and match a pre-loaded 'interesting' pattern.

6) However, the module will not produce LAM or respond correctly to readout commands until.....

7) You issue a Global Enable command: F(26) A(15). This clears any pre-existing patch flags and enables the LAM output.

8) You should now wait for module LAM or use the rear-panel wired-OR trigger signal to start the readout process.

9) When this appears, read out the patch words stored with F(2) A(0). The first word you read will be the first to be captured, identified by which of bits 20-24 are set [bit 20 corresponds to patch 1, bit 24 to patch 5]. The next patch read out will be the highest 'priority' (numerical- based on patch number) now remaining, and then the rest in descending sequence. When you get Q='0', that means you have had all the 'good' data.

10) To start capturing again, issue F(26) A(15).

Wiring Points:-

Issue 4 notes: The linking is now done on the PCB so no links need to be made. The delay lines are 5nS per tap

The output of the front-end comparator is used to clock the main latch and start the memory look-up process. Subsequent logic uses delayed versions of this clock to decide whether to store or discard the pattern. The standard delay line is 5nSec per tap and the outputs are brought to wiring pins as follows:-

Signal Function	Patch 1	Patch 2	Patch 3	Patch 4	Patch 5
Comparator Output (Main Latch Clock) delayed by:					
1 Steps	P40	P46	P19	P63	P57
2 Steps	P10	P14	P3	P30	P26
3 Steps	P42	P48	P21	P65	P59
4 Steps	P12	P16	P5	P32	P28
5 Steps	P44	P50	P24	P68	P61

These delayed clocks need to be wired to three places:-

Comparator freeze	P37	P36	P17	P51	P67
Clock Holding Latch	P33	P35	P34	P54	P22
Clock Flag flip-flop	P8	P38	P52	P53	P6

The suggested delays are:- [these are linked on the board]

Comparator freeze:-	10-15nS (2 step)
Holding Latch Clock:	12nS minimum (3 steps)
FLAG Latch Clock:	25nS minimum (5 steps).

Giving the following wire-wrap link chart:-

PATCH 1:	P37 – P10;	P33 - P42;	P8 - P44;
PATCH 2:	P36 - P14;	P35 - P48;	P38 – P50;
PATCH 3:	P17 – P3;	P34 – P21;	P52 - P24;
PATCH 4:	P51 – P30;	P54 - P65;	P53 - P68;
PATCH 5:	P67 - P26;	P22 - P59;	P6 - P61;

and Fast Clear: P7 - P55.

Other wiring pins:-

P7:	wire to P55 for Fast Clear from NIM input; wire to P69 to use 'input 60' from the IDC connector.
P1	Test point or free wiring point for common VETO line.

Connector Allocation.

60-way IDC:-(front view)

I/P 0 -ve	1	o o	2	I/P 0 +ve
I/P 1 -ve	3	o o	4	I/P 1 +ve
I/P 2 -ve	5	o o	6	I/P 2 +ve
I/P 3 -ve	7	o o	8	I/P 3 +ve
I/P 4 -ve	9	o o	10	I/P 4 +ve
I/P 5 -ve	11	o o	12	I/P 5 +ve
I/P 6 -ve	13	o o	14	I/P 6 +ve
I/P 7 -ve	15	o o	16	I/P 7 +ve
I/P 8 -ve	17	o o	18	I/P 8 +ve
I/P 9 -ve	19	o o	20	I/P 9 +ve
I/P 10 -ve	21	o o	22	I/P 10 +ve
I/P 11 -ve	23	o o	24	I/P 11 +ve
I/P 12 -ve	25	o o	26	I/P 12 +ve
I/P 13 -ve	27	o o	28	I/P 13 +ve
I/P 14 -ve	29	o o	30	I/P 14 +ve
I/P 15 -ve	31	o o	32	I/P 15 +ve
I/P 16 -ve	33	o o	34	I/P 16 +ve
I/P 17 -ve	35	o o	36	I/P 17 +ve
I/P 18 -ve	37	o o	38	I/P 18 +ve
I/P 19 -ve	39	o o	40	I/P 19 +ve
I/P 20 -ve	41	o o	42	I/P 20 +ve
I/P 21 -ve	43	o o	44	I/P 21 +ve
I/P 22 -ve	45	o o	46	I/P 22 +ve
I/P 23 -ve	47	o o	48	I/P 23 +ve
I/P 24 -ve	49	o o	50	I/P 24 +ve
I/P 25 -ve	51	o o	52	I/P 25 +ve
I/P 26 -ve	53	o o	54	I/P 26 +ve
I/P 27 -ve	55	o o	56	I/P 27 +ve
I/P 28 -ve	57	o o	58	I/P 28 +ve
I/P 29 -ve	59	o o	60	I/P 29 +ve

The second (lower) IDC connector starts with input 30 on pins 1 and 2 and ends with the spare input (59) on pins 59, 60. The orientation is the same.

Rear Panel 40-way Connector (rear view)

CK2 PATCH 1+	40	o o	39	CK2 PATCH 1 -
CK2 PATCH 2+	38	o o	37	CK2 PATCH 2 -
CK2 PATCH 3+	36	o o	35	CK2 PATCH 3-
CK2 PATCH 4+	34	o o	33	CK2 PATCH 4 -
CK2 PATCH 5+	32	o o	31	CK2 PATCH 5 -
CK3 PATCH 1+	30	o o	29	CK3 PATCH 1 -
CK3 PATCH 2+	28	o o	27	CK3 PATCH 2 -
CK3 PATCH 3+	26	o o	25	CK3 PATCH 3-
CK3 PATCH 4+	24	o o	23	CK3 PATCH 4 -
CK3 PATCH 5+	22	o o	21	CK3 PATCH 5 -
FORCE 1-	20	o o	19	FORCE 1+
FORCE 2-	18	o o	17	FORCE 2+
FORCE 3-	16	o o	15	FORCE 3+
FORCE 4-	14	o o	13	FORCE 4+
FORCE 5-	12	o o	11	FORCE 5+
Global Enable	10	o o	9	GROUND
TRIGGER	8	o o	7	GROUND
SPARE-ECL	6	o o	5	GROUND
VETO	4	o o	3	GROUND
FLAGOUT	2	o o	1	/FLAGOUT

Notes:-

CK2 is the main latch clock for each patch 'frozen' briefly by the comparator latch enable loop-back.

CK3 is the delayed main latch clock pulse ANDed with the memory output data.

PATCH 1+ refers to the positive sense ECL output for that patch related signal.

FLAGOUT is the propagation delay-corrected logical OR of all the patch flags, in ECL form.

VETO is a single-ended ECL wired-OR signal, which is pulled high by any trigger module seeing a patch flag true.

Suggested mating connector(s):-

Since the scaler outputs and forcing inputs, to say nothing of the overall Flag and VETO signals, need to go to different places, a normal 40-way IDC connector is not suitable.

In order to fit multiple connectors in this position, we need to select a crimp-contact box-section socket, such as the following example from the Farnell (Leeds) catalogue:-

Page 361: Berg 'Mini-Latch' crimp terminal housings and terminals available in two-row, 2+2, 5+5 and 10+10 configurations for picking up 2, 5 or 10 ECL pairs, for example.

P. Marshall, 1st October 1996.
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