# HYTEC VME - MADC 2508

## 32/64 CHANNEL 16-BIT ADC

## DATA ACQUISITION MODULE

## TECHNICAL MANUAL

## AND CIRCUIT DESCRIPTION

HYTEC ELECTRONICS LTD.,
5 CRADOCK ROAD
READING
RG2 0JT
U.K.

Doc: UM2508
Issue: 2.2
Date: 21/04/2005
Author: PJM

CONTENTS

## 1. Introduction

This single width 6U high VME module contains a 32-channel differential or 64-channel single-ended analogue input multiplexer, programmable-gain front end with optional filter (with settings programmed on a per-channel basis), internal reference signals and a 16-bit 8 microsecond sampling ADC providing binary two's complement data. The unit has a large conversion memory (128K words of 16 bits each) for applications requiring a block of samples.

### Analogue Specifications

| | |
|---|---|
| ADC Resolution: | 16 bits |
| ADC FS Input for unity gain: | +/-10V |
| Integral non-linearity: | 3 LSBs |
| Differential non-linearity: | 3 LSBs |
| No missing codes: | 16 bits |
| Zero drift: | 2ppm/deg C |
| Gain error drift: | 2ppm/deg C |
| ADC conversion time: | 8 us |
| Settling time / channel: | 2usmin/8us max (max throughput = 100kHz) |
| Spurious free dynamic range: | 96dB @ 45kHz |
| THD: | -96dB @ 45kHz |
| SNR: | 86dB @ 45kHz |
| Full power bandwidth: | 250kHz |
| Input over voltage protection: | +/-70V |
| Channel filter response: | -3dB @ 50kHz if low pass enabled |

### Operating Temperature Range
0 to +45 deg C ambient.

### Power Requirements
+5V @ 2.5A from the VME supply

## 2. ADC Module - Register Set Overview (AM29)

The module is equipped with a complete set of VME registers in A16 (short addressing) space, in line with Hytec's standard scheme which is modelled on the VXI Configuration Register set, see Figure 1.

This register set comprises the following:-

a) An ID register, indicating manufacturer and type.
b) A vector register, for programming interrupt acknowledge data.
c) A Model Code register, showing 2508 decimal, the unit's type no.
d) A Control and Status Register through which the unit is controlled and its status observed.
e) A Memory Attributes Register, which describes the capabilities of the extended addressing memory area.
f) A Memory Offset register, which positions the data memory in A32 space.
g) An 8-bit channels-per-scan register,
h) A 16-bit low Conversion Address Register, showing the lower 16 bits of the memory address last written to by the ADC system.
i) A 4-bit top Conversion Address Register showing the top bits of the conversion address.
j) A 16-bit Scans-per-Trigger register which controls the number of times the programmed number of channels will be scanned in a sequence.
k) A 4-bit Trigger Rate register, selecting no trigger, external trigger or one of 12 internal rates from 10Hz to 100KHz.
l) A 16 x 16-bit parameter store holding individual channel conversion control data.

## 3. Setting Up - Switches and Jumpers

Before installing the module, there are some jumpers to configure as follows:-

Jumpers J1, J2 and J3 are factory set and must not be moved.

Jumpers J4 to J11: These set the board's VME Base address in A16 (short addressing) space.

Jumpers J4 to J11 ‘OUT’ or ‘IN’ select '1' or '0' respectively for each of 8 address lines. J4 corresponds to address line A13, J11 to A06. The jumper ‘OUT’ means that the corresponding address line must be a '1', jumper ‘IN’ means the address line must be '0'. Address lines A15 and A14 must both be '1' to start at HEX C000 in line with Hytec's standard 'VXI' scheme.

For example: To select D700 as the start address:

| A15 | A14 | A13 | A12 | A11 | A10 | A09 | A08 | A07 | A06 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |

| | | J4 | J5 | J6 | J7 | J8 | J9 | J10 | J11 |
|---|---|---|---|---|---|---|---|---|---|
| fixed | fixed | IN | OUT | IN | OUT | OUT | OUT | IN | IN |

**ADC Data**

The ADC data is binary two’s complement D16 format .

| | |
|---|---|
| Full scale: | 7FFF |
| Mid scale: | 0000 |
| 1LSB below MS | FFFF |
| Full scale –ve | 8000 |

**Conversion Memory (AM09)**

Conversions are stored word ordered with ascending addresses from the memory base address pointed to by the offset register.

| **D15** **D0** | **128K conversions – 4K triggers** |
|---|---|
| 32 channels data | 4Kth scan |
| \| | \| |
| \| | \| |
| \| | \| |
| \| | \| |
| 32 channels data | Third scan |
| Ch 32 data | Second scan |
| \| | |
| Ch2 data | |
| Ch1 data | |
| Ch 32 data | First scan data |
| \| | |
| \| | |
| \| | |
| \| | |
| Ch3 data | |
| Ch2 data | |
| Ch1 data Memory offset base address | |

**3. Setting Up - Switches and Jumpers** (cont..)

There are 7 other jumpers on the unit; jumpers 12 to 18 select which VMEbus IRQ line the unit's Interrupt output signal will be connected to (see section 6 on Interrupts). J12 corresponds to IRQ1 and J18 to IRQ7.

**4. VME Interface - Full Register Set Description**

All registers in this module should be accessed in 16-bit mode, that is they are all D16 compatible. For some, the 'top half' has no meaning, but accesses to these will have no effect.

Running through our 'Overview' list (sect. 2), the following is a full description of the format and function of each register (see Fig. 1).

| Item | Name | Offset from Channel Base Address (HEX) |
|---|---|---|
| **a)/b)** | **ID/Vector** | **+ 00h** |

The ID register and Vector register are at the same address. You read the ID and write the vector. The Vector can be read back for diagnostic purposes at offset 0Ch.

Reading the ID gives HEX DF7F, where 'F7F' on bits 0-11 is Hytec's unique VXI identifier, and 'D' on bits 12-15 means that this unit is A16 register based with A32 memory.

Writing an 8 or 16-bit number to this location (D0-D7 or D15) stores a vector with which it will respond during interrupt acknowledge cycles.

**c) Model Code + 02h**

This simply shows the unit's Hytec catalogue number, which is 2508 decimal.

**d) Control and Status Register + 04h**

This is a 16-bit register (CSR for short) through which the ADC system is controlled and its status observed.

It implements first a BUSY flagging system which is used to show whether or not the ADC is acquiring data. In addition to this, there are several 'fixed' bits, which derive from the VXI spec. and then the following:-

i) Interrupt Enable - one bit to enable the output of the scanning logic as an interrupt source.

ii) Three bits, IPL0, IPL1 and IPL2 which must correspond to the IRQ line jumper for selecting which level of interrupt acknowledge to respond to (see section 6).

iii) An 'ARM' bit for allowing a trigger to start the ADC scanning.

iv) A Soft Trigger bit starting the scan from software.

Other bits are described in more detail in section 5.

**4. VME Interface - Full Register Set Description** (cont.)

**e) Offset register + 06h**

This is a 16-bit register where bits 15 down to 2 correspond to address lines A31 to A18 in A32 addressing to select the start address of the data memory.

**f) Memory Attributes Register + 08h**

This register specifies the capabilities of the A32 port and reads E9FF hex.

**g) Channels-per-Scan Register + 0Ah**

This 8-bit register controls the number of input channels to be scanned before reverting to channel 0. If you put 32 decimal in here, the unit will scan channels 0 to 31 and then loop round to channel 0 again.

**h) Conversion Address Registers + 0E and + 10h**

This 20-bit register is the actual conversion address counter for the ADC, and is formed as 16 bits at base + 0E and 4 bits at base +10. Only one of the top bits actually has any meaning, since the memory is 128K words by 16 bits, but four are provided.

You may read the counter at any time but you should only write to it when the ADC is stopped, for obvious reasons.

**j) Scans per Trigger Register +14h**

This 16-bit register controls how many times the selected number of channels will be scanned before the cycle will be complete. When it is complete, the ADC may either continue after another trigger or stop. On completion, the conversion address may be reset to zero, to loop round a lower segment of memory or continue to fill the memory as desired.

**k) Trigger Rate Register +16h**

This 4-bit register selects the trigger source. All triggers are edge-sensitive. The front panel trigger is active low on the high-to-low transition. The four bits select the source as follows:

| Bits | 3 2 1 0 | Source | 3 2 1 0 | Source |
|---|---|---|---|---|
| | 1 1 1 1 | Soft Trigger only | 1 1 1 0 | Soft Trigger only |
| | 1 1 0 1 | 100000Hz internal | 1 1 0 0 | 50000Hz internal |
| | 1 0 1 1 | 20000Hz internal | 1 0 1 0 | 10000Hz internal |
| | 1 0 0 1 | 5000Hz internal | 1 0 0 0 | 2000Hz internal |
| | 0 1 1 1 | 1000Hz internal | 0 1 1 0 | 500Hz internal |
| | 0 1 0 1 | 200Hz internal | 0 1 0 0 | 100Hz internal |
| | 0 0 1 1 | 50Hz internal | 0 0 1 0 | 20Hz internal |
| | 0 0 0 1 | 10Hz internal | 0 0 0 0 | Front panel trigger |

**4. VME Interface - Full Register Set Description** (cont.)

**l) Parameter Store + 20 to +3Eh**

This 16 x 16-bit register area holds 8 bits for each of the 32 channels. The low byte (data bits 0 to 7) of the first location controls the ADC channel for input 0 and the high byte operates for channel 1. This continues until we reach address +3Eh, where the low byte operates on channel 30 and the high byte on channel 31. In single-ended mode, where both input pins are used to supply analogue signal data referred to analogue ground, the sequence repeats itself, with channel 32 controlled by that for channel 0 and so on. The format of the parameter data is as follows:

| Bit: | 7 (15) | 6 (14) | 5 (13) | 4 (12) | 3 (11) | 2 (10) | 1 (9) | 0 (8) |
|---|---|---|---|---|---|---|---|---|
| | Sense | UNI. | Del-2 | Del-1 | FILT | G3 | G2 | G1 |

Sense: '0' = Normal = positive sense
'1' = Inverse = invert analogue signal

UNI. '0' = Bipolar (normal)
'1' = Unipolar: a 5 volt offset is introduced to create a +/- 5 volt signal from a 0-10 volt input (non-standard).

Delay 1-2 These two bits control an additional delay between the channel being selected and the conversion being started as follows:

| Del-2 | Del-1 | Additional Delay |
|---|---|---|
| 1 | 1 | 8 microseconds |
| 1 | 0 | 4 microseconds |
| 0 | 1 | 2 microseconds |
| 0 | 0 | 0 microseconds |

FILT '1' Low pass filter enabled
'0' Low pass filter disabled

G3, G2, G1 Control the gain of the front-end system for this channel:

| G3 | G2 | G1 | Gain |
|---|---|---|---|
| 1 | 1 | 1 | x64 |
| 1 | 1 | 0 | x32 |
| 1 | 0 | 1 | x16 |
| 1 | 0 | 0 | x8 |
| 0 | 1 | 1 | x8 |
| 0 | 1 | 0 | x4 |
| 0 | 0 | 1 | x2 |
| 0 | 0 | 0 | x1 |

## 5. Control and Status Register Format

The format of this register is as follows:-

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SD | x | 12Bit | LOOP | DIFF | CAL | TRIG | ARM | INTEN | MF | SING | IPL2 | IPL1 | IPL0 | 1 | BUSY |

BUSY: Writing a ‘1’ to this bit resets the control logic. When read, this bit shows whether the ADC is running.

IPL2,1,0: These select the IRQ level that the card will respond to with its interrupt acknowledge vector. The value must agree with the IRQ line selected on jumpers J12 to J18.

SING: This (when set to ‘1’) selects a single sequence of the number of scans of the number of channels selected for each trigger. When set to ‘0’, the scanning logic will repetitively scan after the first trigger until stopped.

MF: This status bit shows that the memory is full (that is the conversion address has overflowed). This stops the current scan and will generate an interrupt if enabled. This bit is cleared by writing a ‘0’ to it or issuing a reset.

INTEN: This bit enables the IRQ output of the board for either memory full or number of scans completed in SINGLE mode. ‘1’ = enabled.

ARM: When set to ‘1’, a trigger will start the scanning process. When set to ‘0’, no triggers are accepted.

TRIG: Writing a ‘1’ to this bit produces a ‘soft trigger’ to start a scan. This is independent of any other triggers. In order to repeat the process (i.e. to trigger again) you must write it as ‘0’, then write it as ‘1’, since the trigger is edge sensitive.

CAL: When set to ‘1’, calibration voltages are fed into the input stage instead of actual external signals. There are four sources, presented in a cycle as follows:

Code 00 – +5 volt reference, code 01 – ground, code 10 – –5 volt reference, code 11 – +2.5 volt reference. The code refers to the bottom two channel address bits, so channel 4 will see the same input as channel 0 and so on.

DIFF: When set to ‘1’, this selects 32 differential inputs. When set to ‘0’ it selects 64 single-ended inputs.

LOOP: When set to ‘1’, this causes the conversion address to be reset to zero when a sequence of scans completes. Selecting 1 scan of 32 channels with the ‘SING’ bit set to ‘’0’ and this bit set to ‘1’ produces a continuous scan of all 32 channels placed into the lowest 32 locations of memory.

12Bit: When set to ‘1’, this causes the output data of the ADC chip to be shifted down 4 bits and placed in the memory with the most significant bit sign-extended. ‘0’ means normal 16-bit data. The data format is always twos-complement binary. Full scale is 7FFF, negative full scale is 8000 Hex.

SD: Scan Done. When read as ‘1’, this means that the selected number of scans of the required number of channels have been completed in ’single’ mode. This bit is cleared by a ‘reset’.

Other bits: ‘1’ means always read as ‘1’, writing has no effect. ’x’ means reserved, can be written and read.

## 6. Interrupts

The interrupt output of the unit is the logical OR of the memory full and ‘scan done’ bits ANDed with the INTEN (interrupt enable) bit.

The ‘true’ output of this logic will cause the jumper selected VME IRQ line to be asserted. The unit implements a RORA (Release-on-Request-Acknowledge) protocol meaning that the service routine has to remove the source of the interrupt before exiting. This is normally done by resetting the module having first read the CSR and any other relevant registers.

## 7. Detailed Operating Sequence

Write the value 1 to the CSR to start, to issue a reset to the logic.

If you will be using interrupts, write the vector (8 or 16 bits) to offset 0h. You may read it back through offset Ch if desired.

Write the number of channels to be scanned into offset Ah (normally 32 decimal).

Write the number of scans per trigger into offset 14h (normally 1)

Write the memory offset into the register at offset 6h. Remember to shift the desired A32 address down 16 bits to produce this value.

Write zero to both sections of the conversion address, or a different value if you wish to start elsewhere in the memory, into locations 0Eh and 10h. Remember that the unit will normally expect to clear the scan address after a sequence, so this should be taken into account.

Prepare the block of 16 words of parameter data, selecting gain, filter and delay for each channel. Often this will be the same for all channels. Write this data into the parameter register set.

Select the trigger source and speed by writing a 4-bit value to offset 16h.

You are now ready to acquire data.

Prepare the CSR value you need to write to select the IRQ level (if used), single or continuous mode, differential option and the memory mode (loop or fill). Add the corresponding bit if you wish to enable the IRQ output (INTEN) and set the CAL bit if you wish to perform a calibration run. Now add the ARM bit, and the data is complete.

Write this prepared value into offset 4h.

On the next trigger edge, the unit will start acquiring data. If you are using soft trigger, add the relevant bit now and re-write the CSR to start the sequence.

If you now read the CSR and test the least significant bit, you will see the ‘BUSY’ status of the unit. If you have selected ‘continuous’, of course, this will remain set indefinitely. If you selected ‘single’, then once the number of scans of the number of channels has been performed the scan will stop, BUSY will be cleared and ‘Scan Done’ will be set. If the scan stopped because the memory overflowed, then that will show in the corresponding CSR bit. Likewise, if Scan Done stopped the scan, then that bit will be showing accordingly.

## 7. Detailed Operating Sequence (cont.)

Here is a complete list of all the forcing signals concerning the state of 'BUSY':

Can only be set by a trigger when ARMed provided that MF is false and Scan Done is false.

BUSY is immediately cleared by 'memory full' or 'Scan Done' and also by 'ARM' being cleared. This is therefore a way of 'soft-stopping' the scan.

## 8. Connections

### Analogue Inputs

Two 37-way D-type socket connectors are used to connect 32 differential or 64 single-ended voltage signals to the module. Pin 1 is bottom right, pin 20 is bottom left looking towards the face of the front panel.

**Connector 1-16 (Top)**

| Pin | Diff Signal | S.E. Signal | Pin | Diff Signal | S.E. Signal |
|---|---|---|---|---|---|
| 1 | Channel 1+ | Channel 1 | 20 | Channel 1- | Channel 33 |
| 2 | Channel 2+ | Channel 2 | 21 | Channel 2- | Channel 34 |
| 3 | Channel 3+ | Channel 3 | 22 | Channel 3- | Channel 35 |
| 4 | Channel 4+ | Channel 4 | 23 | Channel 4- | Channel 36 |
| 5 | Channel 5+ | Channel 5 | 24 | Channel 5- | Channel 37 |
| 6 | Channel 6+ | Channel 6 | 25 | Channel 6- | Channel 38 |
| 7 | Channel 7+ | Channel 7 | 26 | Channel 7- | Channel 39 |
| 8 | Channel 8+ | Channel 8 | 27 | Channel 8- | Channel 40 |
| 9 | Channel 9+ | Channel 9 | 28 | Channel 9- | Channel 41 |
| 10 | Channel 10+ | Channel 10 | 29 | Channel 10- | Channel 42 |
| 11 | Channel 11+ | Channel 11 | 30 | Channel 11- | Channel 43 |
| 12 | Channel 12+ | Channel 12 | 31 | Channel 12- | Channel 44 |
| 13 | Channel 13+ | Channel 13 | 32 | Channel 13- | Channel 45 |
| 14 | Channel 14+ | Channel 14 | 33 | Channel 14- | Channel 46 |
| 15 | Channel 15+ | Channel 15 | 34 | Channel 15- | Channel 47 |
| 16 | Channel 16+ | Channel 16 | 35 | Channel 16- | Channel 48 |
| 17 | +5V fused 1A | | 36 | +5V fused | |
| 18 | Analogue Ground | | 37 | Analogue Ground | |
| 19 | Analogue Ground | | | | |

**Connector 17-32 (Lower)**

| Pin | Diff Signal | S.E. Signal | Pin | Diff Signal | S.E. Signal |
|---|---|---|---|---|---|
| 1 | Channel 17+ | Channel 17 | 20 | Channel 17- | Channel 49 |
| 2 | Channel 18+ | Channel 18 | 21 | Channel 18- | Channel 50 |
| 3 | Channel 19+ | Channel 19 | 22 | Channel 19- | Channel 51 |
| 4 | Channel 20+ | Channel 20 | 23 | Channel 20- | Channel 52 |
| 5 | Channel 21+ | Channel 21 | 24 | Channel 21- | Channel 53 |
| 6 | Channel 22+ | Channel 22 | 25 | Channel 22- | Channel 54 |
| 7 | Channel 23+ | Channel 23 | 26 | Channel 23- | Channel 55 |
| 8 | Channel 24+ | Channel 24 | 27 | Channel 24- | Channel 56 |
| 9 | Channel 25+ | Channel 25 | 28 | Channel 25- | Channel 57 |
| 10 | Channel 26+ | Channel 26 | 29 | Channel 26- | Channel 58 |
| 11 | Channel 27+ | Channel 27 | 30 | Channel 27- | Channel 59 |
| 12 | Channel 28+ | Channel 28 | 31 | Channel 28- | Channel 60 |
| 13 | Channel 29+ | Channel 29 | 32 | Channel 29- | Channel 61 |
| 14 | Channel 30+ | Channel 30 | 33 | Channel 30- | Channel 62 |
| 15 | Channel 31+ | Channel 31 | 34 | Channel 31- | Channel 63 |
| 16 | Channel 32+ | Channel 32 | 35 | Channel 32- | Channel 64 |
| 17 | +5V fused 1A | | 36 | +5V fused | |
| 18 | Analogue Ground | | 37 | Analogue Ground | |
| 19 | Analogue Ground | | | | |

**Digital Signals**

A four pole Lemo connector RA0304 is used to trigger the module.

| Pin | Signal |
|---|---|
| 1 | Trigger input – TTL low-going |
| 2 | Ground |
| 3 | Busy output – TTL low-going |
| 4 | Ground |

**9.Adjustments and Test Points**

| **Adjustment** | **Signal** | **Test point** | **Signal** |
|---|---|---|---|
| VR1 | FILTER BUFF OFFS | TP1 | -15V |
| VR2 | AMP1 INV OFFS | TP2 | ANALOGUE - |
| VR3 | AMP1 OFFS 4 | TP3 | ANALOGUE BUF - |
| VR4 | AMP1 OFFS 2 | TP4 | ANALOGUE + |
| VR5 | AMP2 OFFS 1 | TP5 | ANALOGUE BUF + |
| VR6 | AMP2 BUFF OFFS | TP6 | AMP 1 |
| VR7 | ADC GAIN | TP7 | +15V |
| VR8 | ADC OFFS | TP8 | FILTER BUFF |
| VR9 | U/PLR BIAS OFFS | TP9 | MULTIPLEXED REF V |
| VR10 | +2.5V REF | TP10 | AGND |
| VR11 | -5V REF | TP11 | GND |
| VR12 | AMP1 OFFS 3 | TP12 | VCC |
| VR13 | AMP1 OFFS 1 | TP13 | AMP 2 |
| VR14 | AMP2 OFFS 4 | TP14 | FILTER O/P |
| VR15 | FILTER OFFSET | TP15 | AGND |
| VR16 | FILTER GAIN | TP16 | +5VIN |
| VR17 | +5V REF | TP17 | +5V REF |
| | | TP18 | -5V REF |