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VTR2535T-128K and VTR2535T-512K OCTAL 12bit 10MHZ TRANSIENT RECORDER

USERS MANUAL

For Issue 3 & 4 PCB with Xilinx Firmware Version MTBV1

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CONTENTS

1. INTRODUCTION

The VTR 2535-T Transient Recorder is a dual height single width VME module which digitises the voltage signals present on eight inputs with a resolution of 12 bits and records the data sequentially in its on-board SRAM. There are two basic variants: -

VTR 2535-T-128 stores up to 128K samples per channel,
VTR 2535-T-512 stores up to 512K samples per channel.

The memory is accessible from the VME bus when the module is not acquiring data. An interlock between its Busy and Memory Access control bits ensure that there is no conflict of access.
An interrupt is generated whenever the acquisition is stopped and interrupts enabled. A stop can be set either by a software stop command, a Triggered stop or when the memory is full.
The sample clock may be internally generated at programmed rates of 1, 2, 5 or 10 MHz. The module can also accept an external clock via a front panel two-pin connector.
The module also has an External Trigger input via a front panel connector. The trigger input signal can be programmed to act as a simple trigger (pulse input) or as a triggered Start and Stop signal (using signal levels).
Front panel LEDs indicate the status of Start, Stop, VME access and External Clock Enable conditions.
The module can be set to operated in a number of different modes by writing to on board control registers. The basic modes of operation are:-

- Software driven acquisition where acquisition is started and stopped by writing to a Control register on the unit.
- Pre-triggered sampling here the memory is divided into two, the first half is allocated to pre-trigger samples and the other to post-trigger samples. When the Pre-trigger mode is enabled, data is acquired into the pre-trigger circulating buffer. A change in state at the Trigger input causes the current conversion address of the pre-trigger buffer to be latched in the Trigger Address register so that data can be re-constructed up to the point of trigger. Conversions are then stored in the upper half of the memory until it is full.
- A Hardware Start and Stop mode. Here the trigger input starts the acquisitions on a rising edge, and stops the unit acquiring on a falling edge. This mode also offers the ability to stop acquisition and read the memory without stopping the conversion Address counter. The unit can then be restarted and the number of samples missed calculated.
- The module can also be set to log a pre-set number of samples, and Stop. This can be started by software or hardware triggering.
- Ring Buffer mode this is where the unit cycles round the memory until a stop command is issued either by software or by hardware. The ring buffer mode can be set in any of the above modes apart from the pre-trigger sampling mode.

2. PRODUCT SPECIFICATIONS

2.1 Power Requirements

+5V @ 600mA
+12V @ 350mA
-12V @ 450mA

2.2 Operating Temperature Range

0 to +45 deg Celsius ambient.

2.3 Mechanical

6U single width VME module with access to P1 and P2 connectors.

2.4 Front Panel Indicators

'VME'	LED (green) illuminates for a minimum of 100msecs whenever the module is accessed via the VME bus.
'Start'	LED (green) indicates that Start is set either by software command or by front panel trigger.
'Stop'	LED (red) indicates that acquisition has been stopped either by software command or when the memory is full or by front panel trigger.
'External'	LED (yellow) illuminated when the external clock is enabled.

2.5 Signal Specifications

2.5.1 External Clock

Connector type: 0302
Signal: Differential ECL or single TTL.
Clocks ADC conversions on the rising edge and latches the data on the trailing edge. 10MHz max rate. Max. period without data degradation 1mS.

2.5.2 Trigger

Connector type: 00250
Signal: Single TTL or ECL. Rise time < 20nS
Triggers post sampling in PT mode.
Starts and Stops acquisition in non-PT mode.

2.5.3 Analogue Inputs 0-7

Connector type: 0302 Pin 1+, Pin 2-, Screen common.
Signal: Differential +/- with screen (capasititivly AC coupled to chassis ground)
Span: 0 to 2V unipolar +/-2V, bipolar as determined by PCB jumpers.
0 to 5V unipolar +/-5V, bipolar as determined by PCB jumpers.
0 to 2.5V unipolar +/-2.5V, bipolar as determined by PCB jumpers external reference only.
CMRR: 50dB
CMV: +/-9V

Input impedance	1K/100R jumper selectable.
ADC resolution:	12 bits.
Diff. non-linearity:	+/-0.35 LSB at 12 bits typical.
Int. non-linearity:	+/-0.7 LSB at 12 bits typical.
Offset error:	1 LSB at 12 bits.
Bandwidth (ADC):	20MHz
Transient response:	30nS typical to full scale step(0.01%)
SNR:	67.5dB at 5MHz typical.
SINAD:	65dB at 5MHz typical.
ADC aperture delay:	2nS typical.
ADC aperture jitter:	8pS typical.

Signal Gain and offset can be adjusted using trim pots 'VR1 OF' (offset) and 'VR2 GN' (gain setting). These have been factory pre-set for 0 to 2V unipolar inputs and may need adjustment when other settings.

3. Internal and external Sample Clocks

The unit can be set to use either an internal or external sample clock, via jumper switches. To select the internal sample clock jumpers J42 and J44 need to be made and for external clocking J41 and J43 should be made (see **appendix A**).
The selection of the external or internal clocking and the internal clock rates (of 1, 2, 5 or 10 MHz) are set by writing to the Control register of the unit.

	Control register bit setting		
Clock Setting	T2 (bit D14)	T1 (bit D13)	T0 (bit D12)
External Clock	0	0	0
1MHz	0	0	1
2MHz	0	1	0
5MHz	0	1	1
10MHz	1	0	0

The external clock can have a maxim frequency of 10MHz and a maximum period 1mS without data degradation. The external clock signal can be differential ECL or single TTL. To select ECL jumpers J39 and J40 must be made and J41, J42, J43and J44 removed. To select TTL jumpers J37 and J38 should be made along with J41 and J43.

4. Interrupt Settings

The interrupt generated by the unit is set using on board jumpers J51 to J57 see **appendix A** for settings.
The interrupt priority is set using jumpers J48 to J50 see appendix A for settings.

5. Trigger Input

The trigger input can be used to trigger post sampling in pre-trigger mode or it can be used to start and stop acquisitions. These modes are selected by writing to the control register of the unit.
The trigger input circuitry can be set to operate with various inputs using jumpers JJ1 to JJ9 see **appendix A** for settings.

6. Use of the VME data bus and Memory Access

6.1 Base Address

The module uses A16/D16/D8 (EO) (Even and Odd byte) for accesses to the configuration registers. The base address of the configuration registers is determined by PCB jumper settings (J33=A6 to J26=A12).

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	J26	J27	J28	J29	J30	J31	J32	J33	X	X	CA	CA	CA	0

Addresses are in the range C000 - FFFE
A06 - A13 is the module address determined by the setting of the relevant PCB jumpers (J33=A6 to J26=A12).
A00 - A03 is the particular configuration register address (e.g. C000 is ID).

6.2 Memory Access

The units base address is stored as an offset in the Memory Offset register. For the 128k the address lines A21 to A31 can be used as a memory offset. The 512k module uses address lines A23 to A31.
The unit also supports 32 bit VME block transfer mode BLT for memory access.
Memory data may be accessed as bytes, words or longwords using A32/D32/D16/D8 (EO).
Words and bytes are accessed via D15-D00. A1 addresses the low order word of a longword, A0 the high order word (big endian), thus A0 accesses the first conversion, A1 the second, and so on.
Conversions for each ADC are word ordered from 0 to 128K (512K) as shown: -
Memory top = Base + 1M (4M) words

D31			D16	D15			D00
ADC8	1st to (128K-1)th conversions	64Kx16		ADC8	2nd to 128Kth conversions	64Kx16	
ADC7	1st to (128K-1)th conversions	64Kx16		ADC7	2nd to 128Kth conversions	64Kx16	
ADC6	1st to (128K-1)th conversions	64Kx16		ADC6	2nd to 128Kth conversions	64Kx16	
ADC5	1st to (128K-1)th conversions	64Kx16		ADC5	2nd to 128Kth conversions	64Kx16	
ADC4	1st to (128K-1)th conversions	64Kx16		ADC4	2nd to 128Kth conversions	64Kx16	
ADC3	1st to (128K-1)th conversions	64Kx16		ADC3	2nd to 128Kth conversions	64Kx16	
ADC2	1st to (128K-1)th conversions	64Kx16		ADC2	2nd to 128Kth conversions	64Kx16	
ADC1	1st to (128K-1)th conversions	64Kx16		ADC1	2nd to 128Kth conversions	64Kx16	

Memory base = Value in Memory Offset Register.

6.3 Memory Data

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	
0	0	0	O/R	AD 11	AD 10	AD 09	AD 08	AD 07	AD 06	AD 05	AD 04	AD 03	AD 02	AD 01	AD 00	Sample 1

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	
0	0	0	O/R	AD 11	AD 10	AD 09	AD 08	AD 07	AD 06	AD 05	AD 04	AD 03	AD 02	AD 01	AD 00	Sample 2

ADxx denotes ADC conversion data bit
O/R denotes out of range bit

6.4 Address Modifiers

Configuration Registers: AM29 or 2D (short non-privileged or supervisory)
Memory: AM09 or 0D (extended non-priv. or supervisory)
BTL: AM0B or 0F (extended non-priv. or supervisory)

7. Firmware Registers

7.1 ID (Read)

Address: Base + 00

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1

7.2 Device Type (Read)

Address: Base + 02

128K with trigger = 12535

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	1	1	0	0	0	0	1	1	1	1	0	1	1	1

512K with trigger = 12535

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	1	0	1	1	0	0	0	0	0	0	0	0	1	1	1

7.3 Control & Status Register (CSR)

Control (Write)

Address: Base + 04

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A32	T2	T1	T0	ARM	RP10	RP9	RP8	I.E.	F	RB	C	SP	ST	PT	Rst

Status (Read)

Address: Base + 04

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A32	T2	T1	T0	ARM	RP10	RP9	RP8	I.E.	F	RB	C	SP	ST	PT	Bsy

A32 Enables memory access from VME when set to a 1.
Disables ADC data acquisition.

T2 Set sample clock bit 2 000 - external 001 - 1 MHz 010 - 2MHz

T1 Set sample clock bit 1 011 - 5MHz 100 - 10MHz

T0 Set sample clock bit 0

ARM Enable hardware triggered START and STOP and clears the conversion address to zero.

RP10 – RP8 Select/set reset interval for latency compensation

RP10	RP9	RP8	Reset interval latency compensation
0	0	0	Disable ADC latency compensation
0	0	1	800ns → 850ns
0	1	0	1.60µs → 1.65µs
0	1	1	3.2µs → 3.25µs
1	0	0	12.8µs → 12.85µs
1	0	1	51.2µs → 51.25µs
1	1	0	409.6µs → 409.65µs
1	1	1	1.23ms → 1.23005ms

Table 1 External clock low periods to reset latency compensation.

IE Interrupt Enable - An IRQ is generated if Stop is set.
The IRQ number is determined by PCB jumper settings.
F Full flag - Set when the memory has been completely filled.
RB Ring Buffer Mode - Stop is not set when Full is set when RB=1
Acquisition continues with the conversion address wrapping around.
C Continue acquisition from the point where it was last stopped.
SP Stops acquisition (drives front panel STOP led).
SP is set by: memory full (RB is not set), triggered stop, or pre-set count Stop.
ST Starts acquisition (drives front panel START led) and clears the conversion address to zero.
If PT is set acquisition is confined to the lower 64K of memory until Trigger if PT is not set ST may be set by command or by Trigger whereupon conversions will fill the memory.
PT Enables Pre-trigger acquisition.
Busy Set when acquisition is started or continued.
Inhibits A32 from being set (i.e. disables VME memory accesses).
Rst Clears status register to zero.

7.3.1 Start/Stop/Continue Bits of Control Register

To start acquiring data write a '1' to D02 (START bit) of the Control Register, this also zeros the conversion address register.
A START can also be generated by the trigger input going high and with ARM and PT set.
For any Start the A32 flag must be zero otherwise start will be inhibited.
A stop can be generated in one of 4 ways:

i. A Software Stop by writing a one to D03 of the Control register.
ii. A stop is generated when the memory Full flag is set and ring mode is disabled.
iii. A stop is generated when the number of samples to be read has been reached.
iv. A Hardware stop generated by taking the Trigger input low when ARM and PT are set.

When a STOP is generated the Start bit (D02), Continue bit (D04) and Busy bit (D00) of the CSR are cleared.
Writing a one to the Continue bit (D04) of the Control register allows the acquisition to be restarted after it has been stopped. Alternatively a rising edge on the trigger input will also START acquisition.

7.3.2 Ring buffer mode (RB bit D05)

In Ring Buffer mode RB=1 (bit D05) a Stop and interrupt will not be generated when memory Full flag is set and acquisition continues with the conversion address wrapping around.

7.3.3 Memory full Flag (F bit D06)

The Full flag will be set when the memory has been completely filled and will generate a Stop if the ring buffer mode is disabled RB=0.

7.3.4 Interrupt Enable (IE bit D07)

With the Interrupt Enable bit set a VME IRQ will be generated when ever the Stop bit is asserted.
The VME IRQ generated is determined by PCB jumper settings J51=INT1 to J57=INT7.
The interrupt is cleared by writing a zero to the Stop bit.

7.3.5 ARM and PT

The ARM and PT bits set how the trigger input is used. The valid state are as follows
PT=0 and ARM=0 Trigger input disabled
PT=0 and ARM=1 Null
PT=1 and ARM=0 the unit operates in pre trigger mode.
PT=1 and ARM =1 Start trigger goes high Stop on trigger goes low.
When the ARM bit is set it zeros the conversion address register.

7.3.6 Latency Compensation (RP8-RP10 bits D08 – D10)

The need for latency compensation is due to pipeline delays in the ADC9220 and the delays caused by data manipulation in the VTR2535.
In all modes latency compensation can be enabled/disabled. If latency compensation disabled (RP0=0 RP=0 RP2=0 of the CSR) then the first four data readings on all channels after a Start will be invalid data. If ON then the first data reading (address zero) on all channels after a Start at will be invalid.
Latency compensation is achieved by delaying the incrementing of the address counter at the start or continuation of sampling by a set number conversion clock cycles.
When the external clock is used to control the starting, stopping and continuation of data acquisition a method is available to reset the latency compensation by holding the sample clock low for a defined period (if enabled). The period required is programmable using bits D8 to D10 (RP8-RP10) of the CSR (see **Table 1** for settings).
All address written to the Start Address register and the Trigger/Stop Address register are automatically have latency compensation applied regardless of whether latency compensation is disabled.

7.4 Memory Offset (Read/Write)

Address: Base + 06

VTR 2535-128K

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	x	x	x	x	x

VTR 2535-512K

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A31	A30	A29	A28	A27	A26	A25	A24	A23	x	x	x	x	x	x	x

7.5 Conversion Address or Sample Counter (LS) (Read)

Address: Base + 08

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M15	M14	M13	M12	M11	M10	M09	M08	M07	M06	M05	M04	M03	M02	M01	M00

Conversion Address or Sample Counter (MS) (Read)

Address: Base + 0A

NB M17 and M18 are 0 for the VTR 2535-128

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	0	0	0	0	0	M18	M17	M16

The conversion address registers gives the acquisition address in a 16bit format, which is also the number of logged samples.

7.6 Vector (Read/Write)

Address: Read = Base + 0C, Write = Base + 00

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V09	V08	V07	V06	V05	V04	V03	V02	V01	V00

7.7 Trigger Address/Triggered STOP Address (LS) (Read/Write)

Address: Base + 0E

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
T15	T14	T13	T12	T11	T10	T09	T08	T07	T06	T05	T04	T03	T02	T01	T00

Trigger Address/Triggered STOP Address (MS) (Read/Write)

Address: Base + 10

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
T31	T30	T29	T28	T27	T26	T25	T24	T23	T22	T21	T20	T19	T18	T17	T16

The data held in these registers is the triggered address or the triggered stop address in a 32 bit format.

7.8 Pre-set Count Register (LS) (Read/Write)

Address: Base + 12

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00

Pre-set Count Register (MS) (Read/Write)

Address: Base + 14

NB M17 and M18 are 0 for the VTR 2536-128

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	0	0	0	0	0	P18	P17	P16

The value written to this register will give the number of samples that will be taken before the Stop bit of the CSR is set to one.

7.9 Triggered Start Address (LS) (Read/Write)

Address: Base + 16

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
TS15	TS14	TS13	TS12	TS11	TS10	TS09	TS08	TS07	TS06	TS05	TS04	TS03	TS02	TS01	TS00

Triggered Start Address (MS) (Read/Write)

Address: Base + 18

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
TS15	TS14	TS13	TS12	TS11	TS10	TS09	TS08	TS07	TS06	TS05	TS04	TS03	TS02	TS01	TS00

The data held in these registers is the triggered start address in a 32 bit format.

7.9 Range Setting of Channels Registers (Not facilitated on Issue 3 PCB)

Eight pairs of pcb jumper settings indicate the conversion range of each channel.

Range Setting Channels 1 and 2 (Read only)

Address: Base + 1A

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
x	x	x	x	x	x	x	x	x	x	x	x	RS03	RS02	RS01	RS00

RS01 RS00 00 : 2V span, 01 : Not used, 10 : +/-4V, 11 : +/-5V on channel 0
RS03 RS02 00 : 4V span, 01 : Not used, 10 : +/-2V, 11 : +/-5V on channel 1

Range Setting Channels 3 and 4 (Read only)

Address: Base + 1C

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
x	x	x	x	x	x	x	x	x	x	x	x	RS07	RS06	RS05	RS04

RS05 RS04 00 : 4V span, 01 : Not used, 10 : +/-2V, 11 : +/-5V on channel 2
RS07 RS06 00 : 4V span, 01 : Not used, 10 : +/-2V, 11 : +/-5V on channel 3

Range Setting Channels 5 and 6 (Read only)

Address: Base + 1E

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
x	x	x	x	x	x	x	x	x	x	x	x	RS11	RS10	RS09	RS08

RS09 RS08 00 : 4V span, 01 : Not used, 10 : +/-2V, 11 : +/-5V on channel 4
RS11 RS10 00 : 4V span, 01 : Not used, 10 : +/-2V, 11 : +/-5V on channel 5

Range Setting Channels 7 and 8 (Read only)

Address: Base + 20

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
x	x	x	x	x	x	x	x	x	x	x	x	RS15	RS14	RS13	RS12

RS13 RS12 00 : 4V span, 01 : Not used, 10 : +/-2V, 11 : +/-5V on channel 6
RS15 RS14 00 : 4V span, 01 : Not used, 10 : +/-2V, 11 : +/-5V on channel 7

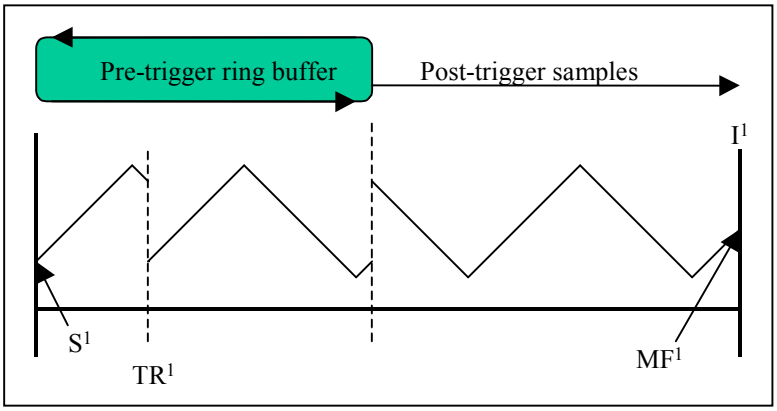
7.10 VME System Reset

A VME system reset will clear the following registers:

- Control Register
- Status Register
- Memory Offset Register
- Vector Register

8. MODES OF OPERATION

8.1 Pre Trigger Mode



S^x=Software Start (ST)
TR=Trigger
MF^X=Memory full Stop
I^x=Interrupt generated
(if Ints enabled)

CSR has the following bits set PT=1 ARM=0 RM=0
Number of Samples to be Logged is set to zero by writing PCR=0
To start digitising set ST=1 in the CSR

In Pre-triggered sampling mode the memory is divided into two, the first half is allocated to pre-trigger samples and the other to post-trigger samples. Data is acquired into the pre-trigger circulating buffer by writing '1' to bit 3 (ST) of the CSR ,. A change in state at the Trigger input causes the last 32bit acquisition address prior to the trigger to be latched into the Trigger Address Register base + 0Ehex` and base + 10hex. This address has latency compensation applied atomically as has the data. The Data acquisition continues from the base of the post-trigger buffer (10000h for the 128k and 40000h for the 512k) until the buffer has been filled whereupon the Stop bit of the CSR is set.

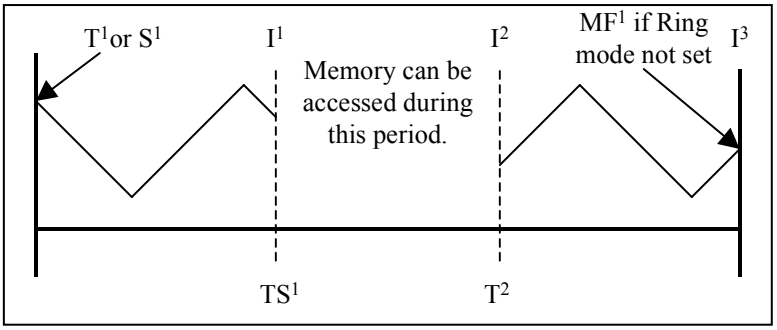
Pre-trigger data can be re-constructed using the Trigger Address as the top address of the pre-trigger buffer. The data from this register needs to be shifted up one and masked with 1FFFFh for 128K version and 7FFFF for the 512K version.
e.g. 128k version
TpAddrRegLS= (Read Trigger address register LS)
Triggered_Addr=(TpAddrRegLS<<1)&0x1FFFF;

e.g. 512k version
TpAddrRegLS= (Read Trigger address register LS)
TpAddrRegMS= (Read Trigger address register MS)
Triggered_Addr=(((TpAddrRegMS<<16)+TpAddrRegLS)<<1)&0x7FFFF;

In the 512K version the memory is divided into 256K blocks otherwise the operation is the same as the 128K module.

Note: A reset must be issued at the beginning of a new operation by writing a '1' to bit 1 of the CSR.

8.2 Triggered START STOP



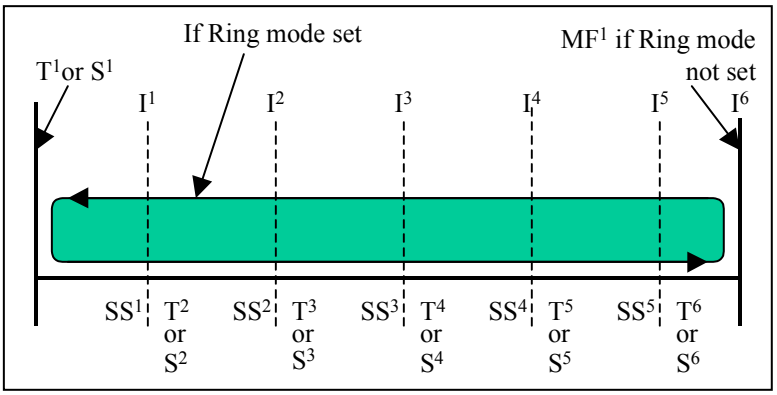
Tx=Triggered Start
TSx=Triggered Stop
Sx=Software Start
SSx=Software Stop
MFX=Memory full Stop
Ix=Interrupt generated
(if Ints enabled)

PT=1 ARM=1 RM=X PCR=0

This can be used with or without ring buffer mode set.
When a '1' is written to ARM the address/sample counter is zeroed.
Trigger going high start acquisition, and writes the start address to the Start Address register. Taking the trigger low stops the unit acquiring and latches the conversion address in to the Triggered Stop register. The writing of the both these registers has latency compensation built in. The address from both these registers is in 32bit format and needs to be shifted up by one and masked with 1FFFFh for 128K version and 7FFFF for the 512K version to give 16bit address.

In the Stopped condition the conversion counter (32 bit) continues to increment, and the memory can be read (once A32 of CSR is set to 1). The acquisitions can then be restarted by taking the Trigger high , which causes the start address (the current value of the conversion counter) to be loaded into the Triggered Start Address register. By reading both the Start Address register and the Stop address register allow the number of samples that have been missed to be calculated.
The above sequence can be repeated indefinitely if the ring buffer mode is set. If ring buffer mode is not set then the unit will Stop when the memory is full.

8.3 Acquire a Set Number of Samples

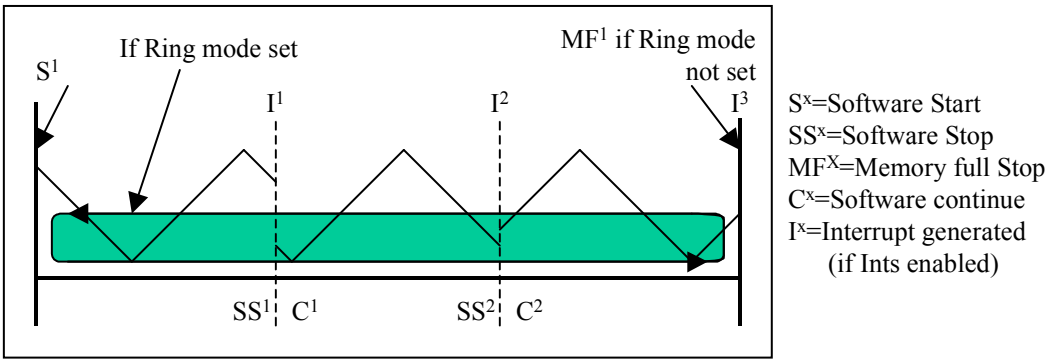


Tx=Triggered Start
TSx=Triggered Stop
Sx=Software Start
SSx=Software Stop
MFX=Memory full Stop
Ix=Interrupt generated
(if Ints enabled)

In this mode the acquisition can be started by software or by a hardware trigger:
Triggered Start PT=1 ARM=1 RM=X PCR>0
Software Start PT=0 ARM=0 RM=X PCR>0

This allows the user to set the number of samples acquired before a STOP is generated. Number of Samples to be Logged is written to the Pre-set Count Register (PCR) the range is from 1 to 1FFFFh for the 128k or 1 to 7FFFFh for the 512k.
Due to the unit writing acquired data in pairs in to the memory the number put in to the pre-set count register should be even. If an odd number of counts is entered it will be rounded up to the nearest even value.

8.4 Software START, STOP and Continue



PT=0 ARM=0 RM=X PCR=0

To start an acquisition using software, a one is written to D02 of the Control register. The A32 flag of the CSR must be cleared otherwise START will be inhibited. Writing a one to the START bit also clears the acquisition address and sets the BUSY bit of the CSR..
If ring buffer mode is **not** set the unit will acquire until the memory is full where it will set the Stop flag and cause an interrupt if interrupt enable bit of the CSR set.
If Ring buffer mode is enabled then a software stop can be issued to stop acquisition by writing a one to D03 of the Control register again an interrupt will be generated if interrupt enable bit set on the Control register.
When a stop is generated the START bit (D02), CONTINUE bit (D04) and BUSY bit (D01) of the CSR are cleared.
Acquisition can be continued by first clearing the Stop bit and then writing a one to the continue bit (D04) of the Control register. The unit will then carry on acquiring from the address it was stopped at. If a Start is used to continue, the address will be cleared.
If a START-STOP-CONTINUE sequence is initiated with Latency Compensation enabled, the first address after the stop address will hold good data. If latency compensation OFF then the first four data readings on all channels will be invalid data.

APPENDIX A

PCB JUMPERS

Clock

J37 & J38	TTL	Make for external TTL clock input
J39 & J40	ECL	Make for external ECL clock input
J41 & J43	Ext	Make for external TTL clock input
J42 & J44	Int	Make for internal TTL clock
J45	INH	Make to inhibit internal TTL clock

CLOCK TYPE	J37	J38	J39	J40	J41	J42	J43	J44
Ext CLK TTL	X	X			X		X	
Ext CLK ECL			X	X				
Int CLK						X		X

X = JUMPER IN

Base Address

J26-J33	BA	Make according to required A13-A06.
J25	Spare	Allocated for memory expansion option

Interrupts

J48-J50 Priority Make according to required interrupt priority.

	J50	J49	J48
1	Made	Made	Open
2	Made	Open	Made
3	Made	Open	Open
4	Open	Made	Made
5	Open	Made	Open
6	Open	Open	Made
7	Open	Open	Open

J51	IRQ1	Make to generate IRQ1*
J52	IRQ2	Make to generate IRQ2*
J53	IRQ3	Make to generate IRQ3*
J54	IRQ4	Make to generate IRQ4*
J55	IRQ5	Make to generate IRQ5*
J56	IRQ6	Make to generate IRQ6*
J57	IRQ7	Make to generate IRQ7*

FPGA Boot

J34-J36	Master	Made when Master FPGA (IC4) SPROM installed.
J8	Slave 1	Made when Slave 1 FPGA (IC5) SPROM installed.
J11	Slave 2	Made when Slave 2 FPGA (IC6) SPROM installed.
J14	Slave 3	Made when Slave 3 FPGA (IC7) SPROM installed.
J17	Slave 4	Made when Slave 4 FPGA (IC8) SPROM installed.
J19-J24	Boot	Left open. Option to boot all slaves from one SPROM.

Input Terminations

J1 (I/Ps 1-8)	Term	When made 100R is connected across the respective input.

Grounds

LK2	AGND	When made connects Analogue Ground to Chassis Ground.
LK3	GND	When made connects Digital Ground to Chassis Ground.
LK4	AGND	When made connects Analogue Ground to Digital Ground.

Ranges

J2	2V	Make for 2V full scale input voltage
J3	5V	Make for 5V full scale input voltage
J4	SEN	Make 1:2 for normal operation.
J5	U/B	Make 1:2 for unipolar input voltage. Make 2:3 for bipolar input voltage.
J6	Xref	Make if single reference is to be used for all channels. (Normally open)
J47	XR/2	IN 2.5V full scale input voltage using external Reference
		OUT 5V full scale input voltage using external Reference

	Jumper Settings								
Range	J2 (2V)	J3 (5V)	J4 (SEN)			J5 U/B			J47 (XR/2)
			1	2	3	1	2	3	
2V Int Ref	X		X	X		X	X		
5V Int Ref		X	X	X		X	X		
±2V Int Ref	X		X	X			X	X	
±5V Int Ref		X	X	X			X	X	
2.5V Ext Ref				X	X	X	X		X
±2.5V Ext Ref				X	X		X	X	X
5V Ext Ref				X	X	X	X		
±5V Ext Ref				X	X		X	X	

X = JUMPER IN

WARNING J2 and J3 must not be IN at the same time.

Not Facilitated on Issue 3 PCB

RS01(J61) RS00(J60) 00 : 2V span, 01 : 5V, 10 : +/-2V, 11 : +/-5V on channel 1
RS03(J63) RS02(J62) 00 : 2V span, 01 : 5V, 10 : +/-2V, 11 : +/-5V on channel 2
RS05(J65) RS04(J64) 00 : 2V span, 01 : 5V, 10 : +/-2V, 11 : +/-5V on channel 3
RS07(J67) RS06(J66) 00 : 2V span, 01 : 5V, 10 : +/-2V, 11 : +/-5V on channel 4
RS09(J69) RS08(J68) 00 : 2V span, 01 : 5V, 10 : +/-2V, 11 : +/-5V on channel 5
RS11(J71) RS10(J70) 00 : 2V span, 01 : 5V, 10 : +/-2V, 11 : +/-5V on channel 6
RS13(J73) RS12(J72) 00 : 2V span, 01 : 5V, 10 : +/-2V, 11 : +/-5V on channel 7
RS15(J75) RS14(J74) 00 : 2V span, 01 : 5V, 10 : +/-2V, 11 : +/-5V on channel 8

Suggested jumper settings.
0 = jumper IN. 1 = Jumper OUT.
e.g. J62 and J63 both IN = 2V span on channel 1.

Trigger Operation

	JJ1	JJ2	JJ3	JJ4	JJ5	JJ6	JJ7	JJ8	JJ9
ECL – SINGLE ENDED			X		X		X		X
TTL – PULL DOWN TERMINATED		X			X	X			X
TTL – PULL UP TERMINATED	X				X	X			X
TTL – PULL DOWN/UP	X	X			X	X			X
ECL – DIFFERENTIAL				X					X
AS ABOVE BUT NEGATIVE I/P								X	

X = JUMPER IN

Denotes Factory Settings