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VTR2537
1M SAMPLES PER CHANNEL OCTAL 12bit 50MHZ TRANSIENT RECORDER

USERS MANUAL

For Issue 4 PCB with FPGA Firmware Version 2537mV401 & 2537sV401

Document Nos.: VTR2537/UTM/G/x/2.0
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CONTENTS

1. INTRODUCTION

The VTR 2537 Transient Recorder is a dual height single width VME64 module which digitises the voltage signals present on eight inputs with a resolution of 12 bits and records all 8 channels simultaneously in its on-board SRAM which accepts up to 1M samples per channel.
The memory is accessible from the VME bus when the module is not acquiring data. An interlock between its Busy and Memory Access control bits ensure that there is no conflict of access.
An interrupt is generated whenever the acquisition is stopped and interrupts enabled. Acquisition can be halted either by:

- Software Stop command
- Hardware Stop
- Memory full.

The sample clock may be internally generated at programmed rates of 0.5, 1, 2, 5, 10, 25 or 50 MHz. The module can also accept an external clock upto 25MHz max via a front panel two-pin connector.
The module accepts an External Trigger via a front panel Lemo connector.
Front panel LEDs indicate the status of Start/Arm, Stop/Busy, VME access and External Clock Enable conditions.
The module can be operated in a number of different modes by writing to on-board control registers. The basic modes of operation are:-

- Pre-triggered (PT) sampling where the memory is divided into two areas, the first is allocated to pre-trigger samples and the other to post-trigger samples. When the Pre-trigger mode is enabled, data is acquired into the pre-trigger circulating buffer. A change in state of the Trigger (either software or hardware generated) causes the current conversion address of the pre-trigger buffer to be latched in the Trigger Address register so that data can be re-constructed up to the point of trigger. Conversions are then stored in the upper half of the memory until it is full. **MS=0 PT=1 RM=0**

- Multiple segment mode (MS). Here the memory is divided into a number of pre/post trigger buffers with the following selectable buffer sizes of 512k, 256k, 128k, 64k, 32k, 16k, 8k, 4k and 2k. When the module is Armed conversions occur in the first pre-trigger circulating buffer. When triggered conversions are stored in the first post-trigger buffer until it is full. Data is then acquired into the next pre-trigger circulating buffer until triggered again whereupon conversions are then stored in the next post-trigger buffer. This continues until all segments are full or acquisition is stopped. At each trigger the trigger address is stored in a section of memory reserved for these addresses. Up to 256 trigger addresses may be recorded. **MS=1 PT=1 RM=0**

- Software driven Start/Stop mode. A software driven mode wherein acquisition is started and stopped by writing to a control register on the unit. If Ring Mode (RM) is not set then the unit will acquire until the memory is full. If Ring Mode (RM) is set acquisition will occur until the unit is stopped by a software stop command. **MS=0 PT=0 RM=X**

- Hardware Gate mode. Here the trigger input signal enables the acquisition when true and stops it when false. If Ring Mode (RM) is not set then the unit will acquirer until the memory is full. If Ring Mode (RM) is set acquisition will occur until the unit the trigger taken low. **MS=0 PT=0 RM=X**

- Ring buffer mode (RM). Here the acquisition cycles round the memory until a stop command is issued by software or via the trigger.

2. PRODUCT SPECIFICATIONS

2.1 Power Requirements

+5V @ 3.5A

2.2 Operating Temperature Range

0 to +45 deg Celsius ambient.

2.3 Mechanical

6U single width VME module with access to P1 and P2 connectors and VME64X capability.

2.4 Front Panel Indicators

'VME'	LED illuminates for a minimum of 100msecs whenever the module is accessed via the VME bus.
'START/ARM'	LED indicates that the module has Started in Stop/Start mode or is Armed and is acquiring data Pre-triggered or Multiple segment mode.
'STOP/BUSY'	LED indicates that the module Stopped in Stop/Start mode or that it has been triggered and is actively acquiring data in to post-trigger memory in Pre-triggered or Multiple segment mode.
'External'	LED illuminated when the external clock is enabled.

2.5 Signal Specifications

2.5.1 External Clock

Connector type:	EPL 0S 302 LEMO Pin 1+, Pin 2-, Screen common.
Signal:	Differential PECL with jumper selectable termination of 50 ohms. Clocks ADC conversions on the rising edge and latches the data on the trailing edge. 25MHz max rate.

2.5.2 Trigger

Connector type:	RP-00-250 Single pole Lemo socket
Signal:	Hardware Trigger positive or negative going TTL 50ohm terminated.

2.5.3 Analogue Inputs 1- 8

Connector type:	EPL 0S 302 LEMO Pin 1+, Pin 2-, Screen common.
Signal:	Differential +/- with screen (capacitively AC coupled to chassis ground)
Span:	+/-2V, bipolar as determined by PCB jumpers. +/-1V, bipolar as determined by PCB jumpers.
Max Input Volts	+/-30V for 100ms
CMRR:	43db @ +/-1V CM
CMV:	+/-3V
Input impedance	100K/100R jumper selectable.

ADC resolution:	12 bits (ADC 14 bits read as 12)
Diff. non-linearity:	+/-0.5 LSB at 12 bits typical. 12 bits no missing codes.
Int. non-linearity:	+/-1 LSB at 12 bits typical.
Offset error:	+/-1.0 LSB at 12 bits (10MHz sample speed).
Gain Error:	+/-0.1%FS at 25 deg C (10MHz sample speed).
Gain Drift:	+/-3ppm per deg C typical.
Offset Drift:	+/-2ppm per deg C typical.
Bandwidth (ADC):	750MHz
Bandwidth (Front end)	50MHz 3dB typical
Transient response:	15ns to 0.1% typical for 2V step
SNR:	70dB at 30MHz typical (ADC).
SINAD:	70dB at 30MHz typical (ADC).
ADC aperture delay:	1.5ns typical.
ADC aperture jitter:	0.3ps rms typical.

3. Signal Gain and Offset

Signal Gain and offset can be adjusted using trim pots 'OFST' (offset) and 'GAIN' (gain setting). These have been factory pre-set for the +/-2V bipolar input range running at 10MHz and may need adjustment when other settings are used.

4. Internal and External Sample Clocks

The unit can be programmed to use either an internal or external sample clock. The selection of the external or internal clocking and the internal clock rates are set by writing to the Control register of the unit.
The external clock signal is PECL (will tolerate LVTTL) and can have a maximum frequency of up to 25MHz .

5. Interrupt Settings

The interrupt generated by the unit is set using on board jumpers J12 to J18 see **appendix A** for settings.
The interrupt priority is set using jumpers J9 to J11 see appendix A for settings.

6. Trigger Input

The trigger input is used to trigger sampling in all modes. The trigger input circuitry can be set to operate with a negative going TTL or positive going TTL Trigger input using jumper JJ3 see **appendix A** for settings.

The trigger must be asserted for a minimum of one a clock cycle of the sample clock when in PT mode. This ensures the trigger is latched on the rising edge of the sample clock.

7. VME Addressing

7.1 A16 A24 Base Address

Address	Offset	Range	Assignment	Size
I/O Base+	0x0000	0x0000 0x0001	Manufacturer's ID	2 Bytes
I/O Base+	0x0002	0x0002 0x0003	Device Type	2 Bytes
I/O Base+	0x0004	0x0004 0x001F	Module specific configuration registers	28 Bytes
I/O Base+	0x0020	0x0020 0x002E	ADC Data	16 Bytes
I/O Base+	0x0030	0x0030 0x0041	Not Mapped Reserved for future use	X Bytes

VTR2537 A16 and A24 address Map

7.1.1 Short Addressing (A16 AM29h and AM2Dh)

The module uses A16/D16/D8 (EO) (Even and Odd byte) for accesses to the configuration registers (CR). The base address of the configuration registers is determined by rotary selector switch SW1 and J36 settings.

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
J36	SW1	SW1	SW1	SW1	0	0	CR	CR	CR	CR	CR	CR	CR	CR	0

Addresses are in the range 0000 – F9FE
The module address is determined by the setting of the rotary selector switch SW1 and Jumper J36 A11 - A15.
The address lines A00 - A05 allow addressing of a particular configuration register.
Configuration Registers Address modifiers:
AM29 Short (A16) non-privilege
AM2D Short (A16) supervisory

7.1.2 Standard Addressing (A24 AM39h and AM3Dh)

The module uses A24/D16/D8 (EO) (Even and Odd byte) for accesses to the configuration registers (CR). The base address of the configuration registers is determined by rotary selector switch SW1 and J36 settings.

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08
J36	SW1	SW1	SW1	SW1	0	0	CR	CR	CR	CR	CR	CR	CR	CR	CR

A07	A06	A05	A04	A03	A02	A01	A00
CR	CR	CR	CR	CR	CR	CR	0

Configuration Registers Address modifiers:
AM39 Standard (A24) non-privilege
AM3D Standard (A24) supervisory

7.2 Memory Access

The units Extended Memory base address is stored as an offset in the Memory Offset register and for the 1M sample per channel unit the address lines A24 to A31 can be used as a memory offset. The unit also supports 32 bit VME block transfer mode BLT for memory access.
Memory data may be accessed as bytes, words or longwords using A32/D32/D16/D8 (EO).
Words and bytes are accessed via D15-D00. A1 addresses the low order word of a longword, A0 the high order word (big endian), thus A0 accesses the first conversion, A1 the second, and so on.
Conversions for each ADC are word ordered from 0 to 1M as shown: -
Memory top = Base + 8M words

D31			D16	D15			D00
ADC8	1st to (1M -1)th conversions	512Kx16		ADC8	2nd to 1M th conversions	512Kx16	
ADC7	1st to (1M -1)th conversions	512Kx16		ADC7	2nd to 1M th conversions	512Kx16	
ADC6	1st to (1M -1)th conversions	512Kx16		ADC6	2nd to 1M th conversions	512Kx16	
ADC5	1st to (1M -1)th conversions	512Kx16		ADC5	2nd to 1M th conversions	512Kx16	
ADC4	1st to (1M -1)th conversions	512Kx16		ADC4	2nd to 1M th conversions	512Kx16	
ADC3	1st to (1M -1)th conversions	512Kx16		ADC3	2nd to 1M th conversions	512Kx16	
ADC2	1st to (1M -1)th conversions	512Kx16		ADC2	2nd to 1M th conversions	512Kx16	
ADC1	1st to (1M-1)th conversions	512Kx16		ADC1	2nd to 1Mth conversions	512Kx16	

Memory base = Value in Memory Offset Register.

7.3 Memory Data

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0	0	0	OTR	AD 11	AD 10	AD 09	AD 08	AD 07	AD 06	AD 05	AD 04	AD 03	AD 02	AD 01	AD 00

2^{nd} conversion

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	OTR	AD 11	AD10	AD 09	AD 08	AD 07	AD 06	AD 05	AD 04	AD 03	AD 02	AD 01	AD 00

1^{st} conversion

ADxx denotes ADC conversion data bit.
OTR denotes out of range bit.

When the ADC input drops below the lower threshold the OTR bit is set giving a digital output of 1000hex. When the ADC exceeds the upper threshold value the OTR bit is set giving a digital output of 1FFFFhex.

Extended Memory Address modifiers:
Memory: AM09 or 0D (extended non-priv. or supervisory)
BTL: AM0B or 0F (extended non-priv. or supervisory)

8. Firmware Registers

8.1 Manufacture ID (Read Only)

Address: Base + 00
Value = 8063 (0x1F7F)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1

8.2 Device Type (Read Only)

Address: Base + 02
Value = 2537 (0x09E9)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	1	0	0	1	1	1	1	0	1	0	0	1

8.3 Control & Status Register (CSR)

Control (Write)
Address: Base + 04

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A32	T5	T4	T3	T2	T1	T0	ARM	I.E.	F	MS	RM	SP	ST	PT	Rst

Status (Read)
Address: Base + 04

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A32	T5	T4	T3	T2	T1	T0	ARM	I.E.	F	MS	RM	SP	LK	PT	SP/Bsy

A32 Enables acquisition memory access from VME when set to a 1 and disables ADC data acquisition. When set to zero can read trigger address memory. A32 can not be written to when unit is sampling.

T5-T3 Set the sampling clock rate.

	Control register bit setting for sample clock rate		
Clock Setting	T5 (bit D14)	T4 (bit D13)	T3 (bit D12)
External Clock	0	0	0
0.5MHz	0	0	1
1MHz	0	1	0
2MHz	0	1	1
5MHz	1	0	0
10MHz	1	0	1
25MHz	1	1	0
50MHz	1	1	1

Max 25MHz

When using the internal clock the user should set jumpers for external clock for single ended to reduce a possible noise source.

T2-T0 Not Used

ARM Start acquisition in the pre-trigger mode (A32 set to '0'). In Start/stop mode this arms the module and allows the trigger to start (A32 set to '0') and stop the module.

IE Interrupt Enable - An IRQ is generated if Stop is set. The IRQ number is determined by PCB jumper settings J12 to J18 see appendix A.

F Full flag - Set when the memory has been completely filled. Reset by writing zero to this bit.

MS Multi-segment Mode. Multiple pre/post triggered acquisitions can be performed according to the segment size as set in the segment size register at Base + 16h.

RB When Ring Buffer mode is set to '1', STOP will not set when memory is full (FULL flag set). The acquisition will continue with the address counter wrapping around.

SP Stops acquisition. SP is set by: memory full, triggered stop, or pre-set count Stop.

ST Writing a '1' Start data acquisition , writing a '0'stops data acquisition.

LK Shows if the clock is locked (if clock is not locked the data may be inaccurate).

PT **1 =** Enables Pre/post-trigger acquisition.
0 = Enables Hardware/Software Triggered Start/Stop mode.

SP/Bsy In Pre/post-trigger mode (PT=1) set when the module has been triggered (drives front panel BUSY LED).
In Start/stop trigger mode (PT=0) set whenever the module is Stopped (drives front panel STOP LED).

Rst Clears status register to zero write only.

8.4 Memory Offset (Read/Write)

Address: Base + 06

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A31	A30	A29	A28	A27	A26	A25	A24	X	X	X	X	X	X	X	X

8.5 Conversion Address or Sample Counter (LS) (Read Only)

Address: Base + 08

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M15	M14	M13	M12	M11	M10	M09	M08	M07	M06	M05	M04	M03	M02	M01	M00

Conversion Address or Sample Counter (MS) (Read Only)

Address: Base + 0

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	0	0	0	0	0	M18	M17	M16

The conversion address registers gives the acquisition address in a 19bit format, which is also the number of logged samples. This is cleared when the unit is ARMed.

8.6 Interrupt Vector (Read/Write)

Address: Base + 0C

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V09	V08	V07	V06	V05	V04	V03	V02	V01	V00

8.7 **Segment size** (Read/Write)

Address: Base + 16

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
x	x	x	X	x	x	x	512K	256K	128K	64K	32K	16K	8K	4K	2K

Defines the pre-trigger buffer size in Pre/post-trigger mode and the pre/post-trigger buffer size in Multi-segment mode. Restricted to binary multiples, e.g. 4 (D02=1) sets pre-trigger and post-trigger buffer sizes to 8K.

8.8 **Number of Trigger Address** (Read Only)

Address: Base + 18

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
x	x	x	x	x	x	x	x	TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0

This gives the number of times the unit has been triggered and has logged the triggered address. Only the first 8 bits used as the trigger address memory is only 256 words in size.
This register is cleared when the unit is Armed.

8.9 **ADC Data Registers** (Read Only)

Address: Base + 20 to 2E

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	OTR	AD11	AD10	AD09	AD08	AD07	AD06	AD05	AD04	AD03	AD02	AD01	AD00

The eight ADC registers store the last sample conversions and may be read at any time.
Data format for +/-2V range is 0000h = –2V, 0800h = 0V and 0FFFh = +2V.
Data format for +/-1V range is 0000h = –1V, 0800h = 0V and 0FFFh = +1V.
If Out-of-Range (OTR) set indicates that the input signal is beyond the input range.

8.10 VME System Reset

A VME system reset will clear the following registers:

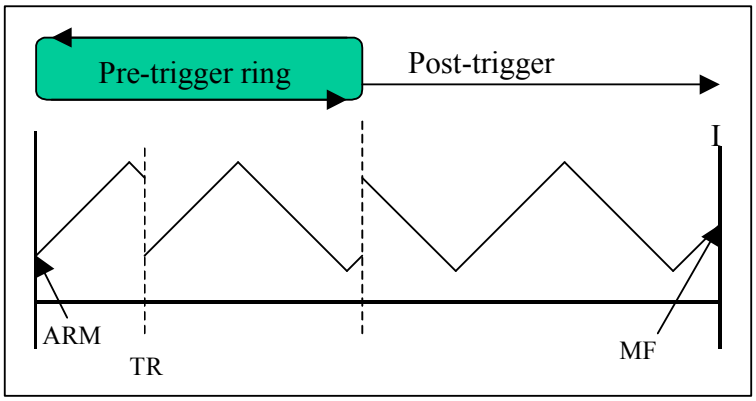
- Control Register
- Status Register
- Memory Offset Register
- Vector Register
- Segment Size Register

9. **Trigger Address Memory** (Read)

The data held in this part of the memory is the triggered address and is held in a 32 bit format.
Note: In Multi-segment mode the Trigger Addresses are stored sequentially from address 0 to 255 memory locations.
To access this part of the extended memory the A32 bit of the CSR needs to set to 0 then do an extended memory read (AM09 or 0D).
The address is zeroed when unit is ARMed.

10. MODES OF OPERATION

10.1 Pre Trigger Mode



TR=Trigger point

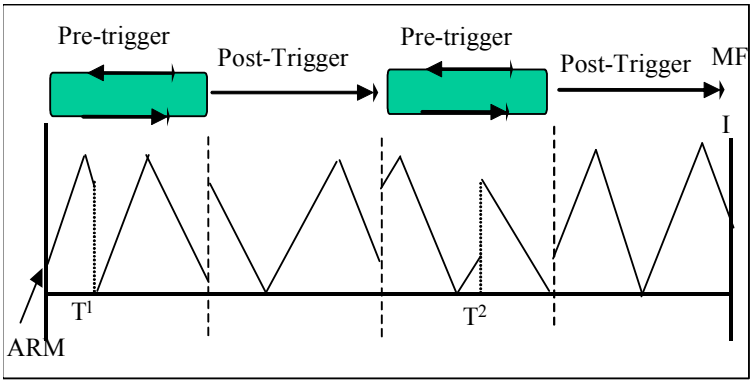
MF=Memory full

I=Interrupt

CSR has the following bits set PT=1 MS=0 RM=0
To start set ARM=1 in CSR

Pre/post-triggered sampling where the memory is divided between that allocated to pre-trigger samples set by the Segment Size register and the remainder to post-trigger samples.
When the Pre/post-trigger mode is enabled, data is acquired into the pre-trigger circulating buffer. A Trigger input (front panel or software) causes the BUSY led to be illuminated and the current conversion address of the pre-trigger buffer to be latched in the Trigger Address register so that data can be re-constructed up to the point of trigger. Conversions are then stored in the post-trigger memory until it is full.

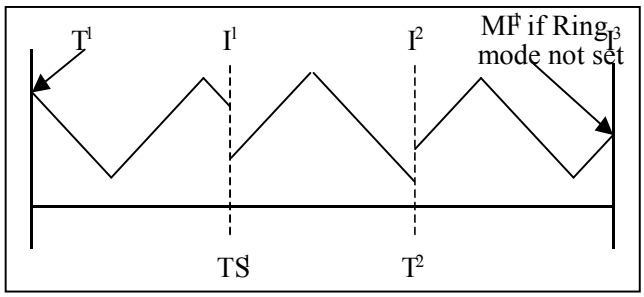
10.2 Multiple Segmented Mode



CSR has the following bits set PT=1 MS=1 RM=0
To start set ARM=1 in CSR

Here the memory is divided into a number of pre/post trigger buffers with a minimum size of 2K per buffer. When the module is Armed conversions occur in the first pre-trigger circulating buffer. When triggered (front panel or software) the BUSY led is illuminated and conversions are stored in the first post-trigger buffer until it is full.
Data is then acquired into the next pre-trigger circulating buffer until triggered again whereupon conversions are then stored in the next post-trigger buffer. This continues until all segments are full or acquisition is stopped. At each trigger the trigger address is stored in a section of memory reserved for these addresses. Up to 256 trigger addresses per channel may be recorded.

10.3 Hardware Triggered START STOP



T^x = Triggered Start

TS^3 =Triggered Stop

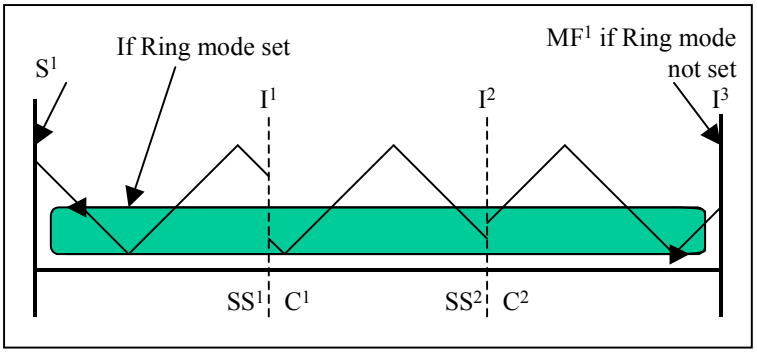
MF^x = Memory full Stop set if RM not set

I^x = Interrupt generated if RM not set (if Ints enabled)

PT=0 ARM=1 MS=0 RM=X

This can be used with or without Ring Buffer mode set.
When a '1' is written to ARM the address/sample counter is zeroed and the STOP led is illuminated.
The front panel trigger input going high starts acquisition and illuminates the START Led on front panel, taking the trigger low stops the unit acquiring (STOP led illuminated).
In the Stopped condition the memory can be read (once A32 of CSR is set to 1). The acquisitions can then be restarted when A32 is set low and by taking the Trigger high.
The above sequence can be repeated indefinitely if the ring buffer mode is set. If ring buffer mode is not set, the unit will stop when the memory is full.

10.4 Software START, STOP



PT=0 MS=0 ARM=1 RM=X

This can be used with or without Ring Buffer mode set.
When a '1' is written to ARM the address/sample counter is zeroed and the STOP led is illuminated.
Writing a one to D02 (ST) of the Control register starts data acquisition and illuminates the START Led on front panel, writing a zero to D02 (ST) of the Control stops the unit acquiring and illuminates the STOP led.
and latches the conversion address in to the Triggered address space. This is the first location in triggered memory space.
In the Stopped condition the memory can be read (once A32 of CSR is set to 1). The acquisitions can then be restarted by writing a one to D02 (ST) of the Control register with A32 is set low.
The above sequence can be repeated indefinitely if the ring buffer mode is set. If ring buffer mode is not set, the unit will stop when the memory is full.

11. Relation to Input Voltage and Output Data

The reference voltage is set at 2.048V when the SPAN VREF Jumper is set to 1:2. This gives a voltage span of +/-2.048 and the volts/bit is approx 1mV as calculated below.

Volts/bit=(2.048/((2**11)-1)) = 0.001000489V/bit

ADCV=V/bit*(ADCval-2048);

With Data Select Format Jumper Set to 2:3 for straight binary representation as shown below.

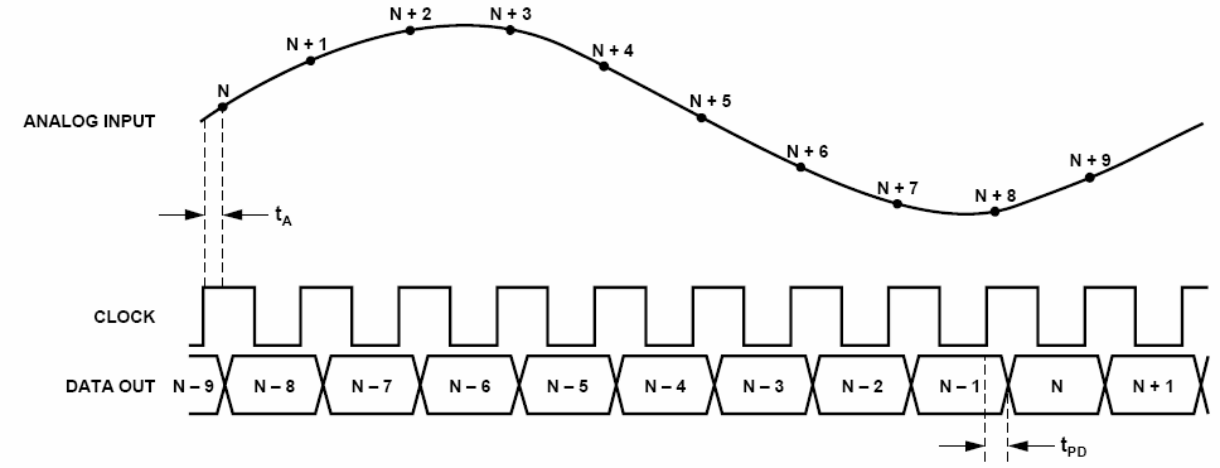
BINARY CODE	INPUT VOLTAGE (V)
1111 1111 1111	+2.048
↑	↑
1000 0000 0001	0.001
1000 0000 0000	0V
0111 1111 1111	-0.001
↑	↑
0000 0000 0000	-2.048

ADC output

12. ADC AD9244 Operation

12.1 Latency Compensation

The ADCs used in the unit have a pipeline architecture which leads to latency. While the converter captures a new input sample every clock cycle, it takes eight clocks cycles for the conversion to be fully processed and appear at the output, as illustrated below.



When the unit starts to sample the firmware of the VTR2537 compensates for this latency by waiting until the data present at the outputs of the ADC is the first full processed value before acquiring in to memory. Also when the unit stops acquiring the firmware carries on acquiring data for a set number of clocks to ensure all good data has been logged in to memory.

12.2 Out of Range (OTR)

An out-of-range condition exits when the analog input voltage is beyond the input range of the ADC. The OTR has the same pipeline latency as the digital data.

OTR	MSB	Analog Input
0	0	Within range
0	1	Within range
1	0	Under range
1	1	Over range

12.3 Clock Stabiliser (DCS)

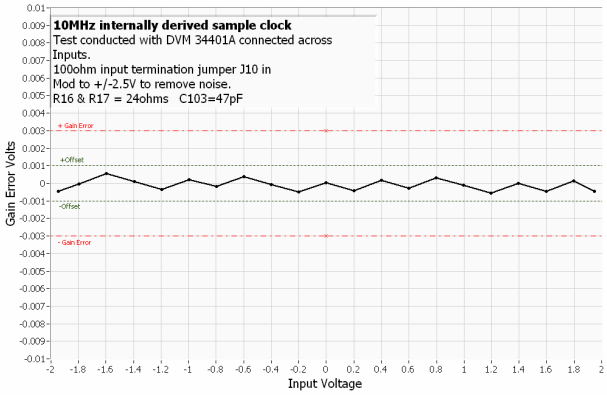
The clock stabiliser in the AD9244 de-sensitises the ADC from clock duty cycle variations. This helps to reduce noise and give a more stable output from the ADC.

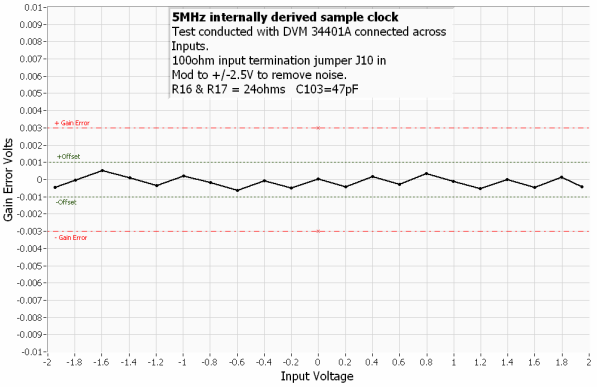
IMPORTANT NOTE

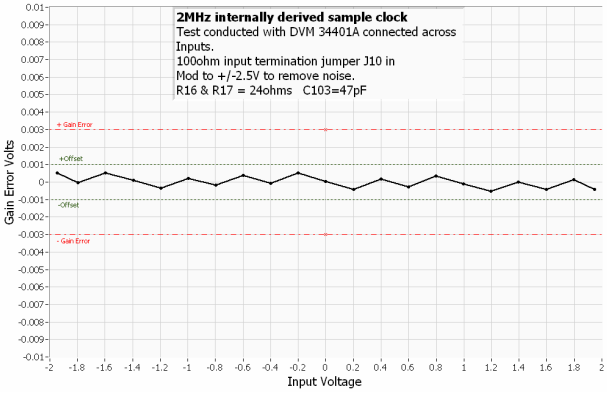
Once the clock frequency is changed, more than 100 clock cycles may be required for the clock stabiliser to settle to the new speed. (Internal clock runs continuously when selected).

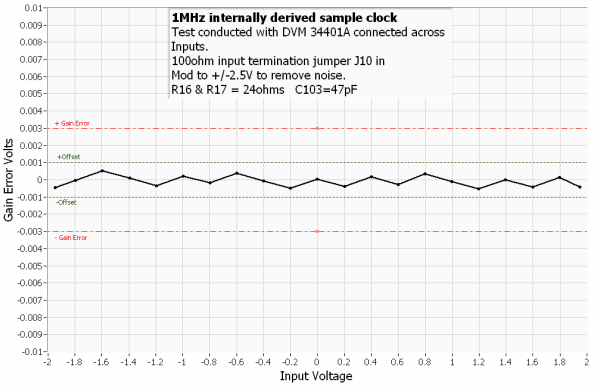
13. Gain Error and Offset Vs Sample Frequency

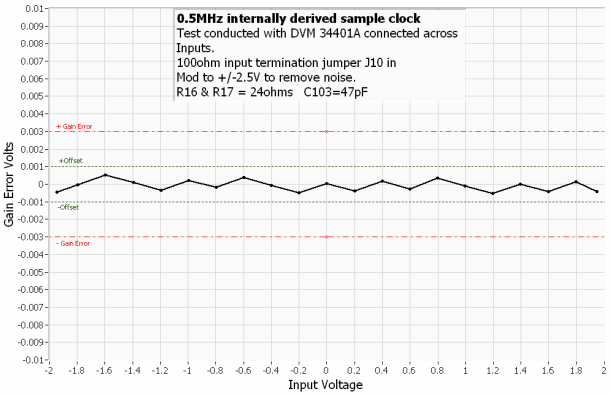
Span +/-2Volts

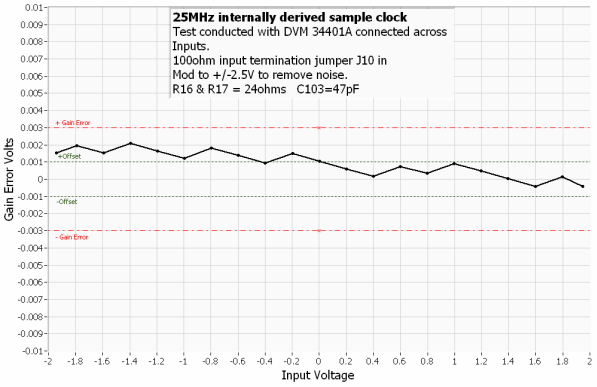


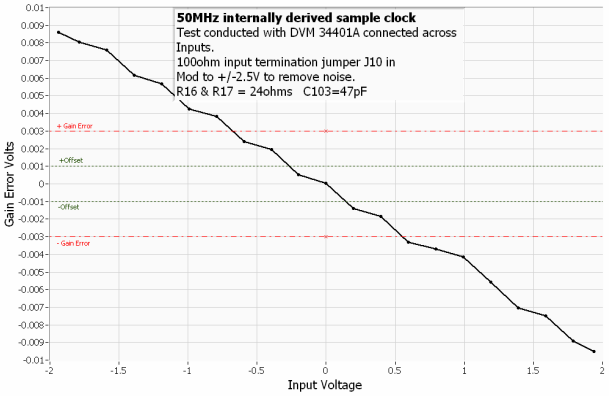


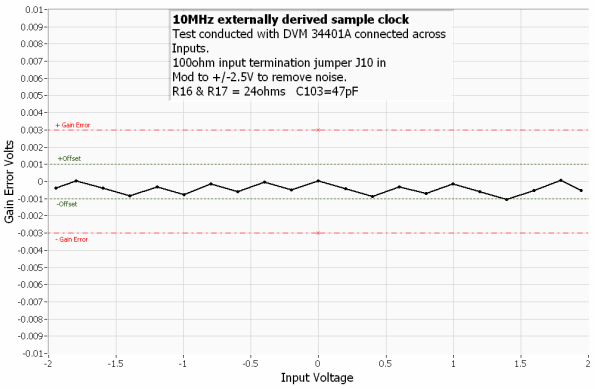


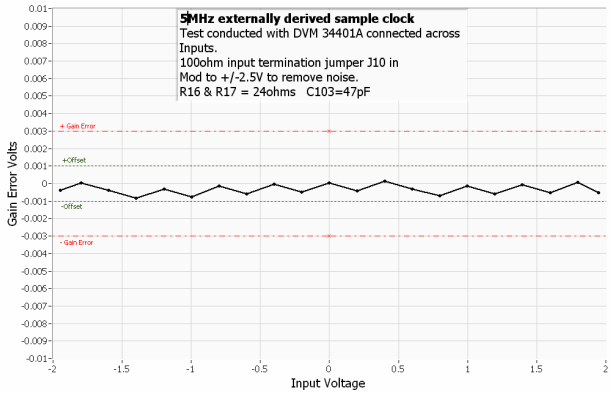


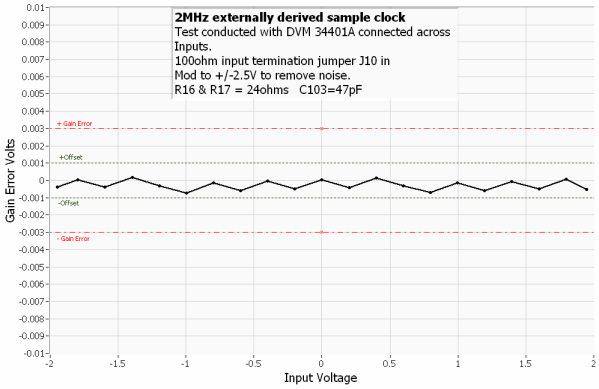


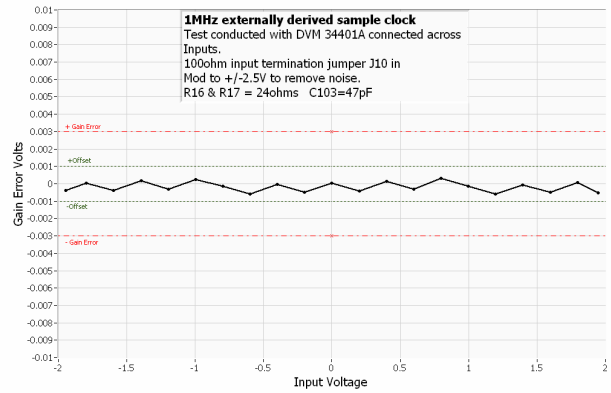


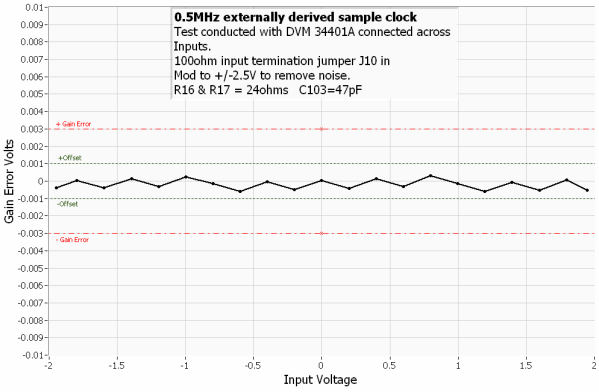

50MHz internally derived sample clock
Test conducted with DVM 34401A connected across Inputs.
100ohm input termination jumper J10 in Mod to +/-2.5V to remove noise.
R16 & R17 = 24ohms C103=47pF
+ Gain Error
+Offset
-Offset
- Gain Error
Gain Error Volts
Input Voltage

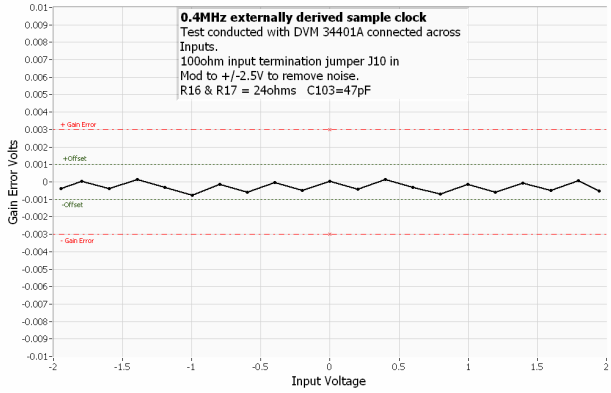

10MHz externally derived sample clock
Test conducted with DVM 34401A connected across Inputs.
100ohm input termination jumper J10 in Mod to +/-2.5V to remove noise.
R16 & R17 = 24ohms C103=47pF
+ Gain Error
+Offset
-Offset
- Gain Error
Gain Error Volts
Input Voltage

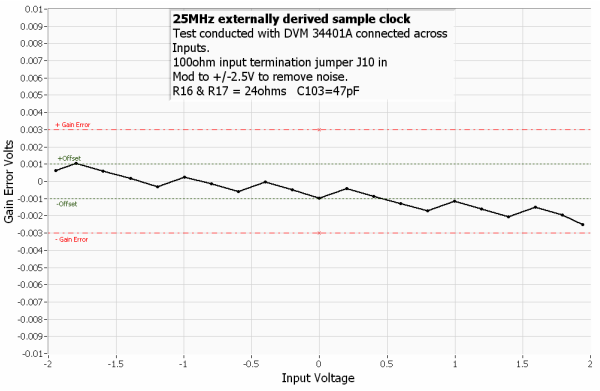

5MHz externally derived sample clock
Test conducted with DVM 34401A connected across Inputs.
100ohm input termination jumper J10 in Mod to +/-2.5V to remove noise.
R16 & R17 = 24ohms C103=47pF
+ Gain Error
+Offset
-Offset
- Gain Error
Gain Error Volts
Input Voltage


2MHz externally derived sample clock
Test conducted with DVM 34401A connected across Inputs.
100ohm input termination jumper J10 in Mod to +/-2.5V to remove noise.
R16 & R17 = 24ohms C103=47pF
+ Gain Error
+Offset
-Offset
- Gain Error
Gain Error Volts
Input Voltage


1MHz externally derived sample clock
Test conducted with DVM 34401A connected across Inputs.
100ohm input termination jumper J10 in Mod to +/-2.5V to remove noise.
R16 & R17 = 24ohms C103=47pF
+ Gain Error
+Offset
-Offset
- Gain Error
Gain Error Volts
Input Voltage


0.5MHz externally derived sample clock
Test conducted with DVM 34401A connected across Inputs.
100ohm input termination jumper J10 in Mod to +/-2.5V to remove noise.
R16 & R17 = 24ohms C103=47pF
+ Gain Error
+Offset
-Offset
- Gain Error
Gain Error Volts
Input Voltage


0.4MHz externally derived sample clock
Test conducted with DVM 34401A connected across Inputs.
100ohm input termination jumper J10 in Mod to +/-2.5V to remove noise.
R16 & R17 = 24ohms C103=47pF
+ Gain Error
+Offset
-Offset
- Gain Error
Gain Error Volts
Input Voltage


25MHz externally derived sample clock
Test conducted with DVM 34401A connected across Inputs.
100ohm input termination jumper J10 in Mod to +/-2.5V to remove noise.
R16 & R17 = 24ohms C103=47pF
+ Gain Error
+Offset
-Offset
- Gain Error
Gain Error Volts
Input Voltage

APPENDIX A

PCB JUMPER and SWITCH SETTINGS

Clock

POS ECL
Single ended J5 Make 1:2 J6 Make 2:3
Differential J5 Make 2:3 J6 Make 1:2

J7 Made puts 50ohm termination on clock input.
When using internal clock should set jumpers for external clock for single ended to reduce a possible noise source.

VME Register Base Address

The base address of the configuration registers is determined by rotary selector switch SW1 and J36 settings.

Base Addrs (Hex)		J36 A15	SW1 A14-A11
A16	A24		
0000	000000	OUT	0
0800	080000	OUT	1
1000	100000	OUT	2
1800	180000	OUT	3
: :	: :	: :	: :
8000	800000	IN	0
8800	880000	IN	1
9000	900000	IN	2
9800	980000	IN	3
: :	: :	: :	: :
E000	E00000	IN	C
E800	E80000	IN	D
F000	F00000	IN	E
F800	F80000	IN	F

Trigger Operation

JJ1: This should be made.
JJ2: This should be left open.
JJ3:
Set Jumper 1:2 for negative going TTL Trigger input.
Set Jumper 2:3 for positive going TTL Trigger input.
NOTE
The front panel trigger input should not be left open when set for positive going TTL as this will cause the trigger to the unit to be HIGH.

Interrupts

J9-J11 Priority Make according to required interrupt priority.

Int Priority Level	J9	J10	J11
1	Made	Made	Open
2	Made	Open	Made
3	Made	Open	Open
4	Open	Made	Made
5	Open	Made	Open
6	Open	Open	Made
7	Open	Open	Open
None	Made	Made	Made

J12 to J18 sets interrupt level.

J12	IRQ1	Make to generate IRQ1*
J13	IRQ2	Make to generate IRQ2*
J14	IRQ3	Make to generate IRQ3*
J15	IRQ4	Make to generate IRQ4*
J16	IRQ5	Make to generate IRQ5*
J17	IRQ6	Make to generate IRQ6*
J18	IRQ7	Make to generate IRQ7*

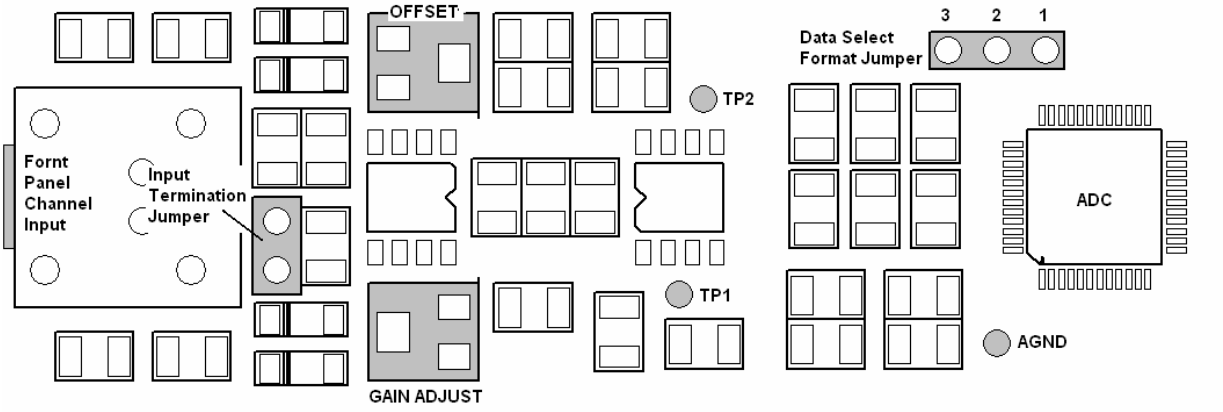
FPGA Boot

J8	Master	Made when Master FPGA (IC50) SPROM installed.
J35	Slave	Made when Slave FPGA (IC51) SPROM installed.

Data Select Format

Set Jumper 1:2 for twos complement data

Set Jumper 2:3 for straight binary



PCB Layout of a single channel

Input Terminations

When the Input Termination Jumper is made 100R is connected across the respective input.

Ranges

Jumper SPAN VREF (I/P chan1 to chan8):
Make 1:2 for +/-2V input voltage (Standard).
Make 2:3 for +/-1V input voltage (may need recalibrating if selected).

Grounds

LK1	GND to AGND	When made connects Analogue Ground to Digital Ground do not remove this link as component damage may result .
LK2	AGND to CGND	When made connects Analogue Ground to Chassis Ground.
LK3	GND to CGND	When made connects Digital Ground to Chassis Ground.

NB LK2 and LK3 both made connects AGND to GND

J19 to J34 are not used.

Denotes Factory Settings