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VTR2537M
128M SAMPLES PER CHANNEL OCTAL 12bit 50MHZ TRANSIENT RECORDER

USERS MANUAL

PCB Issue 2

Xilinx Version
Master 2537mmV6
Slave 2537msV4

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1. Features

The VTR 2537M Transient Recorder is a dual height double width VME module which simultaneously digitises the voltage signals present on eight Lemo inputs with a resolution of 12 bits and records the data in parallel in its on-board RAM which accepts up to 128M samples per channel.

The memory is accessible from the VME bus when the module is not acquiring data. An interlock between its Busy and Memory Access control bits ensure that there is no conflict of access.

An interrupt is generated whenever the acquisition is stopped and interrupts enabled. Acquisition can be halted either by a software/hardware Stop command or when the memory is full.

The sample clock may be internally generated at programmed rates of 5, 10, 25 or 50 MHz. The module can also accept an external clock (50MHz max) via a front panel Lemo connector. Different clock rates may be selected for pre or post-trigger.

The module accepts an External Trigger via a front panel Lemo connector.

Front panel LEDs indicate the status of Arm, Busy/Stop, VME access and External Clock Enable conditions.

The module can be operated in a number of different modes by writing to on-board control registers. The basic modes of operation are:-

- Start/Stop mode. A software driven mode wherein acquisition is started and stopped by writing to bits in a control register on the unit.
- Hardware Gate mode. Here the trigger input signal enables the acquisition when true and stops it when false.

2. PRODUCT SPECIFICATIONS

2.1 Power Requirements

+5V @ 5A

2.2 Operating Temperature Range

0 to +45 deg Celsius ambient.

2.3 Mechanical

6U double width VME module with access to P1 and P2 connectors and VME capability.

2.4 Front Panel Indicators

'VME'	LED illuminates for a minimum of 100msecs whenever the module is accessed via the VME bus.
'Start/ARM'	LED indicates that the module is Armed and is acquiring data.
'Stop/BUSY'	LED indicates that the module has been triggered and that the module is actively acquiring in post-trigger mode.
'Ext Clock'	LED indicates when the external clock is enabled.

2.5 Signal Specifications

2.5.1 External Clock

Connector type:	00250 Single pole Lemo socket.
Signal:	PECL with jumper selectable termination of 50 ohms. Clocks ADC conversions on the rising edge and latches the data on the trailing edge. 50MHz max rate.

2.5.2 Trigger

Connector type:	00250 Single pole Lemo socket
Signal:	Jumper selectable TTL or ECL.. Controls start/stop in 'Gate' mode.

2.5.3 Analogue Inputs 1 - 8

Connector type:	00250 Single pole Lemo socket
Signal:	Single-ended +/- with screen optionally jumper connected to ground.
Span:	+/-2.5V, bipolar as determined by PCB jumpers. +/-5V, bipolar as determined by PCB jumpers.
CMRR:	70db @ +/-1V CM
CMV:	+/-5V
Input impedance	250R/50R jumper selectable.
ADC resolution:	12 bits.
Diff. non-linearity:	+/-0.35 LSB at 12 bits typical. 12 bits no missing codes.
Int. non-linearity:	+/-1.5 LSB at 12 bits typical.

Offset error:	+/-0.3 LSB at 12 bits.
Gain Error:	+/-0.3%FS at 25 deg C
Gain Drift:	+/-26ppm per deg C
Offset Drift:	+/-2ppm per deg C
Bandwidth (ADC):	120MHz
Transient response:	15nS to 0.1% typical for 2V step
SNR:	65dB at 10MHz typical.
SINAD:	65dB at 10MHz typical.
ADC aperture delay:	2nS typical.
ADC aperture jitter:	8pS typical.

3. Signal Gain and Offset

Signal gain and offset can be adjusted using trim pots 'VR1 OF' (offset) and 'VR2 GN' (gain setting). These are factory pre-set for the +/-5V bipolar input range running at 50MHz and may need adjustment when other settings are used.

4. Internal and External Sample Clocks

The unit can be set to use either an internal or external sample clock. External or internal clocking modes and the internal clock rates are set by writing to the Control register of the unit.
The external clock signal is PECL and can have a frequency of 25MHz up to a maximum of 50 MHz . This frequency can be divided by the sample rate register value to provide the data sample rate**.**

5. Interrupt Settings

The interrupt generated by the unit is set using on board jumpers see Appendix A.
The interrupt priority is set using jumpers see Appendix A.

6. Trigger Input

The trigger input is used to trigger post sampling in all modes. The trigger input circuitry can be set to operate with various input levels using jumpers see Appendix A Trigger Operation.

7. Use of the VME data bus and Memory Access

7.1 Short Base Address

The module uses A16/D16/D8 (EO) (Even and Odd byte) for accesses to the configuration registers. The base address of the configuration registers is determined by rotary selector switches SW1 and SW2 settings.

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	SW2	SW2	SW2	SW2	SW1	SW1	SW1	SW1	CA	CA	CA	CA	CA	0

Addresses are in the range C000 - FFDE
A06 - A13 is the module address determined by the setting of the rotary selector switches SW1 and SW2.
A00 - A04 is the particular configuration register address (e.g. C000 is ID).

7.2 Memory Access

Memory access is enabled from VME by setting A32 bit in CSR register to a '1'.
The unit also supports 32 bit VME block transfer mode BLT for memory access.
Memory data may be accessed as longwords using A32/D32.
Conversions for each ADC are word ordered from 0 to 128M as shown: -
Memory top = Base + 1G words

D31 D16	D15 D00	
ADC8 (128Mx16) 1st to 128M th conversions	ADC7 (128Mx16) 1st to 128M th conversions	7FFFFFFFh 60000000h
ADC6 (128Mx16) 1st to 128M th conversions	ADC5 (128Mx16) 1st to 128M th conversions	5FFFFFFFh 40000000h
ADC4 (128Mx16) 1st to 128M th conversions	ADC3 (128Mx16) 1st to 128M th conversions	3FFFFFFFh 20000000h
ADC2 (128Mx16) 1st to 128M th conversions	ADC1 (128Mx16) 1st to 128M th conversions	1FFFFFFF 00000000h

Memory base = Value in Memory Offset Register.

7.3 Memory Data

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0	0	0	O/R	AD 11	AD 10	AD 09	AD 08	AD 07	AD 06	AD 05	AD 04	AD 03	AD 02	AD 01	AD 00

2nd conversion

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	O/R	AD 11	AD 10	AD 09	AD 08	AD 07	AD 06	AD 05	AD 04	AD 03	AD 02	AD 01	AD 00

1st conversion

ADxx denotes ADC conversion data bit
O/R denotes out of range bit

When the ADC input drop below the lower threshold the O/R bit is set giving a digital output of 1000hex.
When the ADC exceeds the upper threshold value the O/R bit is set giving a digital output of 1FFFFhex.

7.4 Address Modifiers

Configuration Registers: AM29 or 2D (short non-privileged or supervisory)
Memory: AM09 or 0D (extended non-priv. or supervisory)
BTL: AM0B or 0F (extended non-priv. or supervisory)

8. Firmware Registers

8.1 Manufacture ID (Read)

Address: Base + 00
Value = 8063 (0x1F7F)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1

8.2 Device Type (Read)

Address: Base + 02

Value = (**2**)2537M (0x5809) (The '**2**' stands for large memory Mver)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	1	0	1	1	0	0	0	0	0	0	0	1	0	0	1

8.3 Control & Status Register (CSR)

Control (Write)
Address: Base + 04

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A32	T2	T1	T0	NU	NU	SDRST	ARM	I.E.	F	NU	NU	SP	ST	NU	Rst

Status (Read)
Address: Base + 04

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A32	T5	T4	T3	NU	NU	NU	ARM	I.E.	F	NU	NU	SP	ST	NU	B/S

A32 Enables memory access from VME when set to a 1 and disables ADC data acquisition.

T2-T0 Sets the acquisition master clock frequency.

	Control register bit setting for High clock rate		
Clock Setting	T2 (bit D14)	T1 (bit D13)	T0 (bit D12)
50MHz	0	0	0
Not used	0	0	1
Not used	0	1	0
Not used	0	1	1
Not used	1	0	0
Not used	1	0	1
Not used	1	1	0
External Clock	1	1	1

Note: The external clock should be a stable fixed clock frequency in the range 25MHz-50MHz

SDRST This will reset the SDRAM control logic, this should not be used. If used need to wait 5ms before SDRAM can be used.

ARM Start acquisition in the pre-trigger mode. (This inhibits A32 from being set, i.e. it disables VME memory accesses).

IE Interrupt Enable - An IRQ is generated if Stop is set. The IRQ number is determined by PCB jumper settings.
F Full flag - Set when the memory has been completely filled.
SP Stops acquisition. SP is set by: memory full, triggered stop, or pre-set count Stop.
ST Write Software trigger.
B/S Stopped in Start/Stop mode. Drives F.P. Busy/StopLED (Read only).
Rst Clears status register to zero (Write only).

8.4 Memory Offset (Read/Write)

Address: Base + 06

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A31	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Two offsets may be used.
The A32 bit must be set in the CSR to enable VME memory access. This allows no more than two modules to co-exist in the crate.

8.5 Interrupt Vector (Read/Write)

Address: Read = Base + 0C, Write = Base + 00

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V09	V08	V07	V06	V05	V04	V03	V02	V01	V00

8.6 Sample Rate (Read/Write)

Address: Base + 1A

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0

This is a 16 bit register that sets the VTR2537M sample rate. The sample rate is determined by the equation:
Sample rate = Master clock / (register value +1)
E.g. a master clock of 50MHz and a sample rate value of 1 yields a sample rate value of 25MHz.

8.7 Test control (Read/Write)

Address: Read = Base + 1C, Write = Base + 1C

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	x	x	x	x	x	x	x	x	x	x	C2	C1	x

This register controls various test elements with the code.
Its default value is zero.
It is a 16 bit register with bit settings as follows:
Bit 1: 0 Store data from ADC
1 Store data from internally generated test ramp.

Note that the test ramp on the second channel is the inverse of that on the first channel.
Bit 2: 0 Internally generated test ramp is full amplitude (i.e. 12 bits)
1 Internally generated test ramp is divided by 16 (i.e.8 bits)

Bits 13-15: Act as a 3 bit control selecting one of eight signals to be routed to test pin 101

Writing to the test control register initiates both sample rate and test control.
It is advisable to wait 50us before memory accesses are made after writing the test control value.

VME System Reset

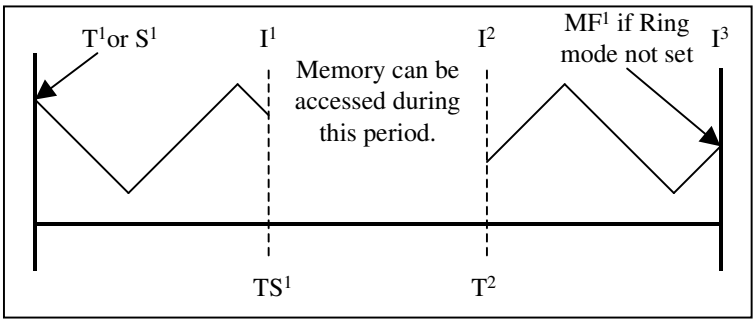
A VME system reset will clear the following registers:

- Control Register
- Status Register
- Memory Offset Register

Vector Register

9. MODES OF OPERATION

9.1 Triggered START STOP

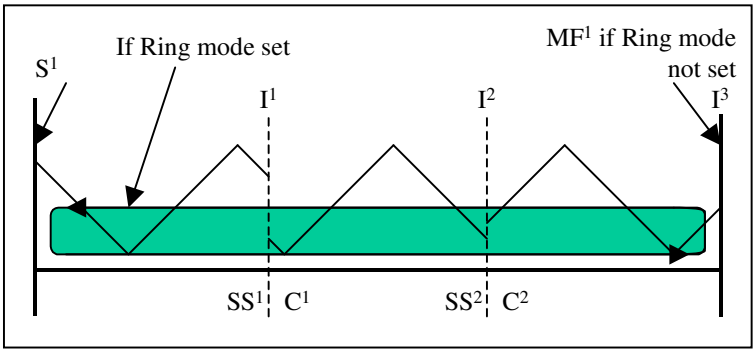


Tx=Triggered Start
TSx=Triggered Stop
Sx=Software Start
SSx=Software Stop
MFX=Memory full Stop
Ix=Interrupt generated
(if Ints enabled)

PT=0 ARM=1 MS=0 C=0

When a '1' is written to ARM bit of the CSR the address/sample counter is zeroed and the STOP led is illuminated.
Trigger going high start acquisition and illuminates the START Led on the front panel, taking the trigger low stops the unit acquiring and illuminates the STOP led.
In the Stopped condition the memory can be read (once A32 of CSR is set to 1).
If trigger is left high the unit will stop when the memory is full.

9.2 Software START, STOP



Sx=Software Start
SSx=Software Stop
MFX=Memory full Stop
Cx=Software continue
Ix=Interrupt generated
(if Ints enabled)

PT=0 ARM=1 MS=0 C=0

When a '1' is written to ARM of the CSR the address/sample counter is zeroed and the STOP led is illuminated.
Writing a one to D02 (ST) of the Control register starts data acquisition and illuminates the START Led on front panel, writing a zero to D02 (ST) of the Control stops the unit acquiring and illuminates the STOP led.
In the Stopped condition the memory can be read (once A32 of CSR is set to 1).
If D02 (ST) is left high the unit will stop when the memory is full.

APPENDIX A

PCB JUMPER and SWITCH SETTINGS

Clock

POS ECL
Single ended J5 Make 2:3 J6 Make 2:3

J7 Made puts 50ohm termination on clock input.

VME Short IO Base Address

SW1 and SW2 sets VME SHORT IO base address
SW1 sets address Lines A9 to A6
SW2 sets address Lines A13 to A10

SW1 = 0x0 and SW2 = 0x0 gives a Base address of 0xC000
to
SW1 = 0xF and SW2 = 0xF gives a Base address of 0xFFC0

Interrupts

J9-J11 Priority Make according to required interrupt priority.

Int Priority Level	J9	J10	J11
1	Made	Made	Open
2	Made	Open	Made
3	Made	Open	Open
4	Open	Made	Made
5	Open	Made	Open
6	Open	Open	Made
7	Open	Open	Open

J12 to J18 sets interrupt level.

J12	IRQ1	Make to generate IRQ1*
J13	IRQ2	Make to generate IRQ2*
J14	IRQ3	Make to generate IRQ3*
J15	IRQ4	Make to generate IRQ4*
J16	IRQ5	Make to generate IRQ5*
J17	IRQ6	Make to generate IRQ6*
J18	IRQ7	Make to generate IRQ7*

FPGA Boot

J8	Master	Made when Master FPGA (IC14) SPROM installed.
J20	Slave	Made when Slave FPGA (IC15) SPROM installed.

Input Terminations

J2 (I/Ps1-8) Term When made 50R is connected across the respective input.

Input Ranges

J3 Make 1-2 to select +/-2.5V span. Make 2-3 to select +/-5V span.

Input Grounding

J1 connects the screen of the Lemo input connector to Agnd.

Grounds

LK1 – LK5 GND to AGND When made connects Analogue Ground to Digital Ground do not remove these link as component damage may result .

Trigger Operation

	JJ1	JJ2	JJ3	JJ4	JJ5	JJ6	JJ7	JJ8	JJ9
ECL-SINGLE ENDED			X		X		X		X
TTL – PULL DOWN TERMINATED		X			X	X			X
TTL – PULL UP TERMINATED	X				X	X			X
TTL – PULL DOWN/UP	X	X			X	X		X	
ECL - DIFFERENTIAL				X					X
AS ABOVE BUT NEGATIVE I/P								X	

Denotes Factory Settings