ADC 520/521

FAST 1 TO 4 CHANNEL

12 BIT ADC CAMAC MODULE

WITH OPTIONAL COMPARATOR

AND SWITCHED GAIN (ADC 521)

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1. INTRODUCTION

This unit is a high speed Analogue to Digital converter module with up to four inputs, each with its own 12 Bit ADC chip and all capable of performing concurrent conversions in as little as 10 microseconds. Each input is fitted with a sample-and-hold amplifier with a settling time of one microsecond, whose gain can be switched under Dataway control (to special order - see ADC521 below) to cater for input ranges down to 500mV without significant drift errors. A comparator can also be fitted as an optional extra, which when loaded with a 12 bit binary value from the dataway performs a comparison with the output of channel 1 (Subaddress 0) every time a conversion is completed, whereupon it can stop, or carry on performing conversions depending on the state of "Greater than" or "Less than" flags, allowing experiments like stress/strain plotting to be achieved very easily. The "Fast" version of this unit, the ADC520F has a conversion time of 15 microseconds, a slightly slower standard version is available, with a maximum conversion time of 25uS, as well as an even faster version ("EF" type) with a conversion time of 10uS.

The ADC 521 is a variant of the ADC 520 which has analogue switches for each channel to permit the gain of the Sample-and-Hold amplifier to be changed in a "times 1" "times N" fashion, the value of N being chosen by the customer up to a value of 50. See also section 6.

A Differential Input variant is also offered, where the input sample-and-hold amplifiers are modified to take the difference between the two input lines from two-pole front panel LEMO sockets. This type is selected by a suffix 'M'.

2. COMMAND SET

Note. - Because the unit has 1 - 4 channels and an optional comparator, links are used to define the configuration, which also govern the Q and X responses.

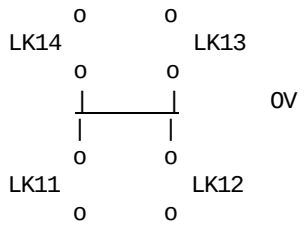
Command	Meaning	Response
F(0) A(0)	Read ch 1 data	X=1, Q=1 if Data Ready
F(0) A(1)	Read ch 2 data	X=1, Q=1 if Data Ready (only if fitted)
F(0) A(2)	Read ch 3 data	X=1, Q=1 if Data Ready (only if fitted)
F(0) A(3)	Read ch 4 data	X=1, Q=1 if Data Ready (only if fitted)
F(1) A(0)	Read Control Register	X=1, Q=1
F(8) A(15)	Test LAM	X=1, Q=LAM
F(16) A(0)	Write Comparator	X=1, Q=Accepted-Data Ready (only if fitted)

This command (F(16) A(0)) also loads the gain control bits for the alternative use of the comparator register in the ADC 521. Bit W1 corresponds to Channel 1, W2 = Channel 2 etc.

F(16) A(15)	Write Test Mode Data into all Data Registers, disable ADC's, enter Test Mode	X=1, Q=1
F(17) A(0)	Write Control Register	X=1, Q=1
F(24) A(0)	Disable LAM	X=1, Q=0
F(26) A(0)	Enable LAM	X=1, Q=0
F(27) A(0)	Test LAM Enabled	X=1, Q=Enabled
F(25) A(15)	Reset, Exit Test Mode	X=1 Q=0

3. CONFIGURATION LINKS

These are located at the top of the PCB at the back:-



NO LINKS - All 4 channels and comparator fitted

LK 14 in - Comparator not fitted

LK 13 in - Channel 4 not fitted

LK 12 in - Channel 3 not fitted

LK 11 in - Channel 2 not fitted

Other Links

LK 1 to 4 Select UNIPOLAR or BIPOLAR for corresponding channel. (LK1 = CH 1)

A - B = BIPOLAR

A - C = UNIPOLAR

LK 5 to 8 Select input span for each channel (LK5=CH1)

A - B = 20V SPAN (Note: Not in Unipolar Mode)

A - C = 10V SPAN

LK 9 Select Test Retrigger Mode

Hytec use only - do not fit.

LK 10 Select Int/Ext Trigger input

A - B = Internal Retrigger (another conversion as soon as data taken)

A - C = External Retrigger

4. OPERATING MODES

This unit operates in three principal modes:-

4.1 Continuous Mode

4.1.1 Internal Triggering (Link 10 in position A - B)

The unit performs conversions on all channels fitted and when all have finished, sets the "Data Ready" Flag - this will also cause a LAM if enabled - it then does another conversion. When this is finished, if the Flag is still set, it waits until it is reset, and when it is, stores the data from this last conversion and starts another. The "Data Ready" Flag is then, of course, immediately set again. The resetting of the "Data Ready" Flag is accomplished by selecting (through the Control Register) which dataway command shall signify that all the data has been read out, i.e. this is the last read command before a new conversion should start. Thus, for a 2 channel ADC, one would chose F(0) A(1) as the Restart Command, then after both subaddresses A(0) and A(1) have been read, a new conversion would start.

4.1.2 External Triggering (Link 10 in position A - C)

In this mode, the Trigger Input will start a new conversion following its LOW to HIGH transition. The Trigger Input is TTL compatible, pulled up to +5V by a 1K resistor. After this conversion, the results are stored in the Data Registers and the "Data Ready" Flag is set. The Data is then read out, finishing with the chosen Restart Command, which resets the "Data Ready" Flag. The unit will now accept a new Trigger Input pulse. The input Sample and Hold circuits go into SAMPLE mode as soon as the conversion is completed, and enter HOLD mode 50nS after the active (Low to High) transition of the Trigger Input. 200nS later, to allow for settling of the Sample and Hold amplifiers, a new conversion is started.

One Trigger Out pulse is produced every time the "Data Ready" Flag is set. It is a 1uSec wide Low going TTL pulse.

4.2 Non-Continuous or Comparator Mode

Every time a conversion is completed, the state of the comparator output flags are examined, using the "Greater than"/"Less than" selection from the Control Register to generate a single "True/False" signal. If it is False, the data is discarded and a new conversion starts; if it is True then the data is stored and the "Data Ready" Flag is set, causing a LAM if enabled. The Flag is reset and a new series of conversions is started by the selected Restart Command, which in this case should be F(16) A(0) to signify that data has been read out and a new value loaded into the comparator.

4.3 Test Mode

For testing purposes, all data registers can be written at the same time with F(16) A(15). They can all then be read back individually by F(0) A(0-3) to check all the data paths.

Entering Test Mode by issuing the command F(16) A(15) disables normal ADC operation. F(25) A(15) is used to exit Test Mode and return to normal operation.

5. CONTROL REGISTER

All the features described under "Operating Modes" on page 5 are selected through the Control Register, which has 4 writeable bits and 6 readable bits:-

6	5	4	3	2	1
STOP	F	R1	R0	CONT	G/L

R0 and R1 select the Restart Command as follows:-

R1	R0	Restart Command
0	0	F(16) A(0)
0	1	F(0) A(0)
1	0	F(0) A(1)
1	1	F(0) A(3)

Note that F(0) A(2) is not available as a restart command since a 3 channel ADC is not offered.

CONT selects Continuous or Comparator Mode.

CONT = '1' - CONTINUOUS

CONT = '0' - COMPARATOR

G/L Selects whether the comparator is looking for an output from Channel 1 ADC Greater Than or Less Than the value written into the Comparator Register:-

G/L = '1' - Greater Than

G/L = '0' - Less Than

The above bits are all writeable and readable, together with two extra read-only bits:-

F (FLAG) - The "Data Ready" Flag - '1' = Data Ready

STOP - The output of the comparator logic - '1' = 'True'

6. DATA FORMAT

The ADC and the Comparator both use straight Binary or Offset Binary, depending whether the unit is in Unipolar or Bipolar Mode.

Note - 0-20V Unipolar is NOT available.

Standard input ranges are +/-5V, 0-10V, +/-10V.

Special Input Ranges can be supplied to reduce the input range down as low as 500mV, for example, by adding extra components around the input Sample-and-Hold amplifier, contact HYTEC for details.

These ranges can be switched from the dataway, in a "Times 1, Times N" fashion on a per-channel basis. In this case, the control of the switches is achieved through the bottom four bits of the Comparator Register, where bit 1 corresponds to the switch, which will control the gain of Channel 1.

This module is known as the ADC 521.

Data Written = '1' - Gain is "Times N"

Data Written = '0' - Gain is "Times 1"

7. GETTING STARTED

With a fast ADC unit like this, with its Special Control Register functions, actually getting it to start doing what you want can be quite tricky. Follow these rules:

Decide the Operating Mode, Restart Command etc. and load the Control Register with F(17) A(0). This command is accepted at any time. If you choose Comparator Mode, start by selecting Greater Than, whereupon the Flag will immediately be set because the Comparator Register is reset by Power-On or F(25) A(15). (Any ADC data will be greater than zero at this point so the Data Ready Flag will be set).

Having got the Flag set, you may now access the Comparator Register and the Control Register to set up your starting conditions. (Note: the unit will not let you write to the Comparator or Read the Data unless the Flag is set).

If you want Continuous Mode, just write this to the Control Register with the Restart Command Selection and the unit will immediately tell you it has "Data Ready". Take the data, ending with the Restart Command and away you go!

If you get "stuck" try F(25) A(15) to kick the unit into life!

8. POWER REQUIREMENTS

+ 6V 1A
+ 24V 100mA
- 24V 100mA

9. PARTS LIST

Integrated Circuits

Type	Qty	Location(s)
74LS00	2	IC23, IC31
74LS02	5	IC6, IC18, IC29, IC32, IC33
74LS04	1	IC30
74LS08	3	IC8, IC25, IC28
74LS14	1	IC14
74LS74	3	IC15, IC26, IC27
74LS85	3	IC20, IC21, IC22 (Comparator only)
74LS123	3	IC24, IC34, IC35
74LS139	1	IC17
74LS153	1	IC13
74LS174	2	IC11, IC12 (Comparator or ADC 521)
74LS175	1	IC10
74LS365	1	IC19
74LS366	2	IC4, IC5
74LS652 **	8	IC36 - IC43 inc. (4 channel unit)
7401	3	IC1, IC2, IC3
7405	1	IC7
7437	1	IC16
PLS100	1	IC9 (Version 4, on socket)
HA5320-5 **	4	IC48, IC49, IC50, IC51
ADC674K **	4	IC44, IC45, IC46, IC47

(See Note 1 on page 9 about ADC chip types for each module type)

** Note: On 1 or 2 channel units, unused channels will not be equipped with S/H (HA5320-5), ADC or data register (LS652) chips.

7815	1	VREG (+12 V Reg)
7915	1	VREG (-12 V Reg) Front panel.

Discrete Semiconductors

1N5401	1	D1
1N4148	9	D2 - D10 inc.

Passive Components

10R 0.25W	8	R21 - R28 inc.
100R	4	R13 - R16 inc.
220R	2	R43, R44
270R	4	R33 - R36 inc.
330R	1	R53
1K0	7	R41,R42,R45,R52,R54,R55,R56
6K8	2	R59, R60
10K	12	R46 - R50 inc., R62 - R68 inc.
22K	8	R5 - R12 inc.
33K	1	R51
39K	2	R58, R61
100K	4	R29 - R32 inc.
1M0	4	R1 - R4 inc.

PARTS LIST (cont.)

200R Preset	8	RV5 - RV12 inc.
10K Preset	4	RV1 - RV4 inc.
20K Preset	4	RV13 - RV16 inc.
SOT (Special)	8	R17 - R20 inc., R37 - R40 inc.
47pF cer.	4	C31 - C34 inc.
82pF cer.	4	C15 - C18 inc.
220pF cer.	1	C29
1n0 cer.	1	C30
100nF cer.	20	C19 - C22 inc., C23 - C26 inc. and all decouplers "C".
1uF 35V tant.	4	C3 - C6 inc.
15uF 16V tant.	2	C27, C28
100uF 6V tant.	2	C1, C2
SOT ***	8	C7 - C14 inc.
Fuse 1A	2	FS2, FS3
Fuse 2A	1	FS1

Note 1: The type of ADC chip fitted depends on the type/grade of module ordered as follows:-

Standard units : 25 uSec. conversion - ADC chip is ADC574K
Fast units (F) : 15 uSec. conversion - ADC chip is ADC674K
Extra Fast (EF): 10 uSec. conversion - ADC chip is ADC774K

*** Extra "Select-on-Test" components which may be added to special order.