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VICB8003 VME 64x INDUSTRY PACK CARRIER BOARD WITH SHARC DSP PROCESSOR.

USERS MANUAL

PCB Issue 3
Xilinx Version 8003V603

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1. PRODUCT DESCRIPTION

The VICB 8003 is a 6U (double height) VME board constructed to the VME64x standard, with EMC front panel, injector/ejector handles, guide pin and slot keying, static discharge protection, hot swap capability, blue power up LED, geographical addressing or jumpers, 5-row P1 and P2 connectors and 5-row P0 connector. An Analog Devices ADSP21061 or 21062 SHARC (Super Harvard Architecture) DSP processor is also fitted for front-end processing.

The module features hot-swap capability with auto power up and host interaction. An on-board FPGA allows full mapping of the IP board memory, I/O and ID spaces.

The VME interface supports short I/O access A16:D32:D16:D08 (EO), standard I/O access A24:D32:D16:D08 (EO) and extended memory access A32:D32:D16:D08 (EO).

Four Industry Pack sites are available and can accept 4 single-size Industry Packs.

The carrier board supports the 8MHz IP interface.

One of VMEbus interrupt lines IRQ1 to IRQ7 can be selected and enabled by writing to an on-board register. The Industry Pack interrupt lines INT0 and INT1 from each of the four sites can be enabled on an individual basis and mapped to the selected VME IRQ line.

The base address of extended memory can be set by register (offset addressing) or by geographical addressing lines. The size of the IP memory allocated to each site can be set to 1MB, 2MB, 4MB or 8MB per site through a control register.

Four front panel mounted LED’s flash to visually confirm completed IP access cycles to individual slots.

There is a TTL input on the front panel that allows connection to any or all of the IP card Strobe lines through jumpers. The signal is routed through a reserved pin on the IP logic connector to allow overall control to be applied to IP boards in data acquisition systems.

The carrier board has some thickened I/O tracks to allow the IP boards to be powered externally to give full isolation.

All I/O is via the VME backplane P0 and P2 connectors as specified in the VME64 extensions specification. The signals connect to the industry pack sites according to the VME64x Greenspring pinout for IP module carriers.

Hytec has a number of rear-mounted transition cards with high-density 50-way [SCSI2] connectors, which can cater for all 200 IP I/O signals and provide any necessary signal conditioning.

1.1 Key Features

- VME64 extensions / Industry Pack Carrier Board
- VME64x rear panel I/O
- ADPS21061 or 21062 SHARC DSP microprocessor with Flash boot EPROM and optional RAM memory and front panel serial or LVDS link ports.
- Full EMC shielding and insertion/extraction handles
- Fully Hot-Swap capable with auto power-up and host interaction
- 6U (double height) VME base card
- User selectable VME interrupt level
- Geographical addressing
- Front panel TTL input to IP cards via Strobe lines
- Thickened I/O lines to allow external power supplies to IPs
- VME 64x Configuration ROM
- On-board clock generation
- VME64x guide pin and slot keying
- 3.3V supply to P2 connector
- 5V supply to P2 connector

2. USE OF THE VME DATA BUS AND MEMORY ACCESS

2.1 VME Addressing

The module uses A16/D32/D16/D08 (EO) (Even and Odd byte) or A24/D32/D16/D08 (EO) for accesses to the IP I/O, IP ID and Carrier board Configuration Registers.
The base address of these areas is determined either by PCB jumper settings (J6 to J10) or by VME64x geographical addressing lines GA0 to GA4.
The PCB jumpers on issue 2 boards should be used only where geographical addressing is not available and ***will*** override the GA lines so they should not be fitted in a GA crate. Later issue 3 PCBs have a different jumper arrangement where either jumpers or GA lines set the base address. (see appendix A)

Address	Offset	Range	Assignment	Size
I/O Base+	0x0000	0x0000 0x007E	IP A I/O Space	128 Bytes
I/O Base+	0x0080	0x0080 0x00FE	IP A ID Space	128 Bytes
I/O Base+	0x0100	0x0100 0x017E	IP B I/O Space	128 Bytes
I/O Base+	0x0180	0x0180 0x01FE	IP B ID Space	128 Bytes
I/O Base+	0x0200	0x0200 0x027E	IP C I/O Space	128 Bytes
I/O Base+	0x0280	0x0280 0x02FE	IP C ID Space	128 Bytes
I/O Base+	0x0300	0x0300 0x037E	IP D I/O Space	128 Bytes
I/O Base+	0x0380	0x0380 0x03FE	IP D ID Space	128 Bytes
I/O Base+	0x0400	0x0400 0x041E	Carrier on board registers	32 Bytes
I/O Base +	0x0420	0x0420 0x043E	SHARC Control Registers	32 Bytes
I/O Base +	0x0440	0x0440 0x047E	Dual-Ported SRAM accessible from VME and SHARC	64 Bytes
I/O Base+	0x0480	0x0480 0x04FF	Green Springs Type ID	128 Bytes
I/O Base+	0x0600	0x0600 0x07FF	VME64x configuration ROM (See **appendix B)**	512 Bytes

8003 A16 and A24 address Map

2.1.1 Short Addressing (A16 AM29h and 2Dh)

In Short address mode the geographical addressing lines equate to the address lines GA0 =A11 to GA4=A15 and the jumper address setting J6=A11 to J10=A15.
A11 - A15 is the module address determined by the setting of the relevant PCB jumpers or geographical address lines

Address modifiers

IP I/O, IP ID and Carrier board Configuration Registers:
AM29 Short (A16) non-privileged.
AM2D Short (A16) supervisory.

2.1.2 Standard Addressing (A24 AM39h and 3Dh)

The A24 base address is determined either by PCB jumper settings J6=A19 to J10=A23 or by geographical addressing lines GA0 =A19 to GA4=A23.

IP I/O, IP ID and Carrier board Configuration Registers:
AM39 Standard (A24) non-privileged.
AM3D Standard (A24) supervisory.

2.1.3 Carrier board Configuration ROM (A24 AM2Fh)

See **appendix B** for the contents of the configuration ROM.
Address modifiers
AM2F Configuration ROM/Control & Status Registers. Address selection as above.

2.2 IP Memory Access

The module uses A32/D16/D08 (EO) (Even and Odd byte) for accesses to the IP memory.
The base address of the memory can be set by either the Geographical address lines/jumpers or by using the Memory Offset Register. Writing a '1' to bit 6 of the CSR CB register (base + 0x0408h) selects the Memory Offset Register to set the base address.

MEM MODE (bit 6 CSRCB)	**Memory Addressing Mode**
0	Geographical address lines
1	Memory Offset register

Bit 6 CSR CB setting the memory address mode

Using the Memory Offset Register allows address lines A22 to A31 to be used to set the base address.
Geographical addressing uses the lines GA0=A22 to GA4=A26 – see table below.

2.2.1 IP Memory Size

Some controllers have a limited memory range so to take account of this when using geographical addressing the memory size allocated to each IP card can be controlled: -

CSR CB		IP Memory Size	Address Lines	
IPMS1 (bit 8)	IPMS0 (bit 7)		Geographical Addressing	Memory Offset Register
0	0	1MB	A22-A26 **	A22-A31
0	1	2MB	A23-A26 **	A23-A31
1	0	4MB	N/A	A24-A31
1	1	8MB	A27-A31	A25-A31

Here the GA address is shifted up one. This only allows 16 slots to be used with geographical Addressing

NOTE ** Upper address lines A27-A31 inclusive MUST all be zero in this mode.

2.2.2 Carrier Board Memory Map

Address	Memory Range				Memory Assignment
	1MB	2MB	4MB	8MB	
Memory Base +	0x000000 0x0FFFFE	0x000000 0x1FFFFE	0x000000 0x3FFFFE	0x000000 0x7FFFFE	IP A
Memory Base +	0x100000 0x1FFFFE	0x200000 0x3FFFFE	0x400000 0x7FFFFE	0x800000 0XFFFFFE	IP B
Memory Base +	0x200000 0x2FFFFE	0x400000 0x5FFFFE	0x800000 0xBFFFFE	0x1000000 0x17FFFE	IP C
Memory Base +	0x300000 0x3FFFFE	0x600000 0x7FFFFE	0xC00000 0xFFFFFE	0x1800000 0x1FFFFE	IP D

Address Modifiers
Memory: AM09 or AM0D (extended non-privileged or supervisory)

3. ON BOARD FEATURES

The configuration and control of the 8003 module is achieved by the following registers:

Base	Offset	Register	Description
Base +	0x400	IP Status	Allows state of IP INT and Error flags to be monitored
Base +	0x404	Memory Offset	Sets base address of IP memory areas
Base +	0x408	Control & Status Register CB	Set up of VME part of 8003
Base +	0x40C	IP Interrupt Select	Selects IP interrupts to be mapped to VME IRQ

8003 On-Board Registers

3.1 IP Status Register (Read Only)

Address: Read = Base + 0x0400

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
			IP TIME OUT	ERR D	ERR C	ERR B	ERR A	INT REQ D1	INT REQ C1	INT REQ B1	INT REQ A1	INT REQ D0	INT REQ C0	INT REQ B0	INT REQ A0

Two interrupt status and one error status bits for each of IP sites A – D plus the SHARC IP Timeout flag bit (see section 6.2.1).

3.2 Memory Offset (Read/Write)

Address: Read = Base + 0x0404, Write = Base + 0x0404

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	x	x	x	x	x	x

'x' = don't care

3.3 Control & Status Register Carrier Board (CSR CB)

Control (Write)
Address: Base + 0x0408

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
NU	NU	NU	NU	NU	NU	NU	IP MS1	IP MS0	BADD SEL	IPCLK SEL	INTSEL 2	INTSEL 1	INTSEL 0	INTEN	Rst

Status (Read)
Address: Base + 0x0408

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
NU	NU	NU	NU	NU	NU	NU	IPMS 1	IPMS 0	BADD SEL	IPCLK SEL	INTSEL 2	INTSEL 1	INTSEL 0	INTEN	Rst

Rst Clears status register to zero when written as a '1'.
INTEN Enable interrupt from carrier board to VMEbus backplane.
INTSEL0 Select VME interrupt level.
INTSEL1 Select VME interrupt level. (See section 4).
INTSEL2 Select VME interrupt level.
IPCLKSEL Select 8MHz IP clock =0 or 32MHz clock =1.
BADDSEL Select memory base address to be defined by geographical address lines=0 or by Memory offset register=1.
IP MS0 Set IP memory size.
IP MS1 Set IP memory size. (See section 2.2)

3.4 IP Interrupt Select Register (Read/Write)

Address: Base + 0x040C

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
NU	NU	NU	NU	NU	NU	NU	NU	IPINT D1	IPINT C1	IPINT B1	IPINT A1	IPINT D0	IPINT C0	IPINT B0	IPINT A0

This selects which IP interrupt lines will be enabled.
'1' = corresponding IP card interrupt enabled.

3.5 VME System and Board Resets

3.5.1 A VME system reset will clear the following registers:

- CSR CB
- Memory Offset Register
- IP Interrupt Select register

3.5.2 A board reset generated from the CSR CB bit 0 will clear the following registers:

- CSR CB
- IP Interrupt Select register

4. INTERRUPT SETTINGS

The interrupt level generated by the carrier board is set using the CSR CB register INTSEL0 (bit 2), INTSEL1 (bit 3), and INTSEL2 (bit 4).

Interrupt Level	INTSEL 2	INTSEL 1	INTSEL 0
None	0	0	0
IRQ 1	0	0	1
IRQ 2	0	1	0
IRQ 3	0	1	1
IRQ 4	1	0	0
IRQ 5	1	0	1
IRQ 6	1	1	0
IRQ 7	1	1	1

VME Interrupt Level Select

The IP Interrupt Select register allows the user to enable only the IP interrupts required and mask off the rest.
To select an IP interrupt write a '1' to the appropriate bit of the register see **section 3.4** above.
The interrupt vector is held on the individual IP cards.
To enable VME interrupts from the carrier board to the VMEbus backplane set bit 1 of the CSR CB to '1'.
Writing a '0' to this register disables the interrupts.
The VME interrupt is cleared when it is acknowledged [ROAK protocol].

The IP interrupts are prioritised in the 8003 where IP A has the highest and IP D the lowest.

Each IP card can be loaded with a separate IP vector and when an interrupt occurs the controller will be given the interrupt vector of the highest priority IP card currently asserting either of its interrupt lines.

If all four cards interrupt at the same time then IP A will be serviced first then IP B then IP C and finally IP D.

Reading the IP Status register of the 8003 at base + 0x0400 (READ ONLY) shows which IP cards have interrupts pending.

5. VME64x KEYING AND ALIGNMENT PINS

The keying mechanism provides for three key holes on top and three keying holes on the bottom of each board and subrack slot. Each key hole can be keyed with a "No Key" or a keying peg in one of four positions. With three key holes top and bottom the scheme provides a total of 15,625 keying combinations.

6. SHARC PROCESSOR AND ASSOCIATED DEVICES

6.1 Configurations available

The 8003 board is available in a number of versions with different processors and peripherals as follows:

Model Number	Processor	Additional features
8003.0	ADSP21061	None
8003.1	ADSP21062	None
8003.2	ADSP21061	Second Flash EPROM, 256K x 32 SRAM, PC16550 RS232 serial port and two SHARC serial links on front-panel micro-D connectors.
8003.3	ADSP21062	Six front-panel LVDS SHARC links on micro-D connectors.

All units are fitted with one 1M x 8 flash EPROM boot device. This flash EPROM plus the processor's internal RAM and the second flash EPROM and external RAM if fitted, are all accessible from VME on a write/read basis unless J22, the write protect jumper, is fitted. Two jumpers, J13 and J14, are used to select the boot mode of the processor as follows:

J13	J14	Mode selected
OUT	OUT	HOST-controlled mode, boot from Host (host writes program directly into SHARC).
OUT	IN	HOST-controlled mode, boot from Link Port.
IN	OUT	Stand-Alone mode, boot from Flash 0. (default)
IN	IN	Stand-Alone mode, boot from Flash 1. (PC16550 Remote serial connect).

6.2 SHARC Control Registers

The ADSP21061/2 has its own set of registers in the Xilinx through which its operation is controlled either by VME or the 21061/2. The set is positioned as shown in the table in Section 2.1 and comprises the following:

Base	Offset	Register	Description
Base +	0x420	IP Status	Allows state of IP INT and Error flags to be monitored
Base +	0x424	SHARC Memory Offset	Sets base address of SHARC memory areas in VME A32
Base +	0x428	Control & Status Register SH	Set up of SHARC part of 8003
Base +	0x42C	IP Interrupt Select	Selects IP interrupts to be mapped to SHARC IRQ

8003 SHARC Registers

6.2.1 IP Status Register (R/W)

Address: Read = Base + 0x0420

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
			SHARC IP ERROR	ERR D	ERR C	ERR B	ERR A	INT REQ D1	INT REQ C1	INT REQ B1	INT REQ A1	INT REQ D0	INT REQ C0	INT REQ B0	INT REQ A0

Two interrupt status and one error status bits for each of IP sites A – D. Plus a flag bit, bit 12, indicating a failure when the SHARC attempted an IP access. Any write to offset 0x420 clears this bit.

6.2.2 Memory Offset (Read/Write)

Address: Read = Base + 0x0424, Write = Base + 0x0424

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A31	A30	A29	A28	A27	A26	A25	A24	A23	x	x	x	x	x	x	x

'x' = don't care

6.2.3 Control & Status Register SHARC (CSR SH)

Address: Base + 0x0428

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
FLAG 3	FLAG 2	FLAG 1	FLAG 0	OE-F2/3	OE-F0/1	SYSRST	IPMS 1	IPMS 0	X	J22	IRQ1	IRQ0	J14	J13	RST

RST: Reset the SHARC processor (pulse on write '1') reads '1' for SHARC RUN enable.
J13/14 State of start-up jumpers, read only (RO): jumper OUT = '1'.
IRQ0 '1' = map selected IP interrupts to SHARC IRQ0. (R/W)
IRQ1 '1' = map selected IP interrupts to SHARC IRQ1. (R/W)
[Select only one of these!].
J22 State of the write protect jumper, read only (RO): jumper OUT = '1' = Write Enabled.
IPMS0, 1 Reflects state of IP memory size selection from CSRCB. (RO).
SYSRST '1' = Permit VME SYSRST to reset SHARC processor. (R/W).
OE-F0/1 Output enable for Flag0 and Flag1 outputs.
OE-F2/3 Output enable for Flag2 and Flag3 outputs.
Flag0 Writeable bit which, if enabled, will drive the SHARC Flag0 pin. Reads actual state.
Flag1 Writeable bit which, if enabled, will drive the SHARC Flag1 pin. Reads actual state.
Flag2 Writeable bit which, if enabled, will drive the SHARC Flag2 pin. Reads actual state.
Flag3 Writeable bit which, if enabled, will drive the SHARC Flag3 pin. Reads actual state.

6.2.4 IP Interrupt Select Register (Read/Write)

Address: Base + 0x042C

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
NU	NU	NU	SHARC IP ERROR	NU	NU	NU	NU	IPINT D1	IPINT C1	IPINT B1	IPINT A1	IPINT D0	IPINT C0	IPINT B0	IPINT A0

This selects which IP interrupt lines will be mapped to the SHARC IRQ line selected in CSR SH. Note that it would be incorrect to map an IP interrupt to both VME and SHARC. It also allows the SHARC IP ERROR bit to be mapped to the SHARC IRQ.
'1' = corresponding IP card interrupt enabled.

6.3 SHARC Memory Addressing

The internal RAM of the SHARC processor and its peripherals, the flash EPROM(s) and external RAM are all accessible from VME through offset addressing. The offset is specified in the register described in section 6.2.2.

Note also that the way that the SHARC processor addresses memory is quite different from that used in VME. That is, whatever the size of the addressed object, the address increment is always 1. Thus consecutive bytes of the flash EPROM as seen from the SHARC are at addresses 00000000, 00000001 and 00000002 and consecutive 32-bit data words in its memory or the external data memory are likewise addressed at 0xx00000, 0xx00001 and 0xx00002, where 'xx' represents upper address bits to select the appropriate area of memory. In order to connect this strange arrangement to VME, the least significant address line of VME, namely A1, has been connected to the least significant SHARC address line. Thus consecutive bytes in a flash EPROM will appear as lower (D00-D07) bits in consecutive words of VME space. When composing write commands to the flash, it should be remembered that in order to produce a particular EPROM address, double that value needs to be placed on the VME address lines.
[i.e. shift the address up one bit].

When consecutive 32-bit words of SHARC internal RAM or external RAM (if fitted) are addressed from VME in D32 mode (LWORD asserted), the VME address is further shifted down one bit in order to map these areas correctly and make them accessible to the host – see the address map below. If LWORD is not asserted (i.e.D16 mode) this address shift does not occur making SHARC internal memory 'Short Word Addressing' possible.

6.3.1 SHARC VME Memory Addressing Map.

Offset from Register -set Base Address	SHARC Address	Contents
000000-0003FC	000000-0000FF	SHARC IOP Registers – D32 only
080000-08FFFC	020000-023FFF	SHARC Internal RAM Block 0 - Normal Word Addressing - D32
090000-09FFFC	024000-027FFF	SHARC Internal RAM Block 1 - Normal Word Addressing - D32

[32-bit long words on long word boundaries or 16-bit lower/upper words on word boundaries if SHARC Short Word Addressing is selected by **NOT** asserting LWORD – D16].
For example, D32 write/read 0x12345678 at offset 0x090000, then D16 read 0x5678 at offset 0x090000 and 0x1234 at offset 0x090002.

200000-3FFFFE	MS0 or BMS	Flash EPROM 0 [D0-7 bytes on word boundaries]
400000-5FFFFE	MS0 + 0x100000	Flash EPROM 1 (if fitted) [D0-7 bytes on word boundaries]
600000-6FFFFC	MS2	SHARC external RAM (if fitted) [256K x 32-bit long words on long-word boundaries: D32 only]

6.3.2 SHARC Address Map

The way that the SHARC processor addresses external devices is on the basis of banks. Each bank has a chip select line associated with it and a register, which defines how cycles are completed. The four select lines are connected as follows:

MS0 or BMS (Boot memory select) connects to flash memory 0 or 1 (chosen by the Xilinx).
MS1 connects to the PC16550 UART device, if fitted.
MS2 connects to the external RAM
MS3 connects to the Xilinx for access to internal registers and the IP cards.

All except MS3 should have their cycles completed internally by the wait state machine. The default value of 6 internal clocks (of the 32MHz master clock) is OK for all these devices. Cycles to the Xilinx (and to the IP cards through the Xilinx) should be terminated externally by ACK after an internal wait of 6 clocks.

The actual access times of the external devices, if fitted, are as follows and the user may trim the wait state machine to these timings if desired:
Flash EPROM:90 nanoseconds.
SRAM: 20 nanoseconds

PC16550 UART: 150 nanoseconds approx. (use 6 wait states).

SHARC Address Map:

Address Range	Contents
00000000-0007FFFF	SHARC Internal RAM
00080000-003FFFFF	SHARC multi-processor space (not used).
00400000-004FFFFF	Flash EPROM 0.
00500000-005FFFFF	Flash EPROM 1.
00600000-00BFFFFF	Aliases of Flash EPROM's 0 and 1.
00C00000-013FFFFF	PC16550 UART Device – only a very small part used!
01400000-014FFFFF	256K X 32-bits External RAM (if fitted).
01500000-01BFFFFF	Aliases of external RAM.
01C00000-01C007FF	IP I/O and ID access plus Xilinx registers (as VME A16 map).
02000000-020FFFFF	IP 'A' Memory access (1M 16-bit words).
02100000-021FFFFF	IP 'B' Memory access.
02200000-022FFFFF	IP 'C' Memory access.
02300000-023FFFFF	IP 'D' Memory access.

Thus each of MS0, 1, 2 and 3 **MUST** to be set up as 8M blocks.

The Xilinx provides ACK termination for all accesses by MS3, whether the SHARC addresses internal registers, configuration data, dual-ported RAM or IP cards. It also provides termination even if the addressed device is not present (that is an absent or faulty IP card).

6.4 Operating Principles

The normal procedure for operating the SHARC processor on this card is to develop a program for it, load it into the flash EPROM and then let it run. Some applications may require the program to be downloaded to the card over a serial line and then programmed into the flash by the SHARC processor. This requires a 'secondary' boot program, which is held in the optional second flash device as a 'low level boot program'.

Care should be exercised when down-loading a program to the SHARC since in certain modes it is looking constantly for the appearance of valid code in certain locations, for example in host-booted mode. For this reason it is recommended that the first word of code be written last.

Internally, the 8003 has a shared address and data bus. There are two possible masters of this bus – the SHARC processor and the VME port (through the Xilinx). By default, the SHARC is bus master and the VME port requests use of the bus when it decodes a valid address and modifier. It does this by asserting host bus request (HBR) and receiving host bus grant (HBG). The time taken to achieve this will depend on what the SHARC is doing when the request arrives but there should be no more than a 1 microsecond delay. The SHARC experiences a similar 'interruption' if the VME port uses the bus. In order to be able to examine VME addresses while the SHARC is in control of the bus, the address lines are separated by a set of buffers. When the SHARC wishes to address the Xilinx-connected areas (that is the IP cards and Xilinx internal areas) or when the VME port wishes to access SHARC memory areas, the buffers are used to connect the address lines together. If the SHARC does access Xilinx-connected areas using MS3, this signal is used to inhibit the VME address-decoding scheme and turn off any VME buffers which would contend with the SHARC cycle.

It is important to bear in mind that if the SHARC processor attempts to address an area of memory which does not physically exist (that is outside the ranges shown in the above address map) then cycle termination will not take place and the processor will enter a 'hung' state. In the unlikely event that this should happen then a working program MUST replace the program that caused it to happen. The difficulty is that if the processor enters the 'hung' state then the usual mechanism for changing the program, writing to the flash from VME, will not work because it relies on the SHARC granting the bus to the VME port, which at this stage it is unable to do. Nor can the SHARC rectify the problem itself since it is unable to communicate with anything.

The only exit from this 'deadly embrace' is to power the board off and select a different start-up mode such as booting from a link port. The processor will not find a program to run and enter a dormant state in which it is possible for you to re-program the flash with working code.

6.5 Connector Pin Definitions

As described in Section 6.1, some of the variants of this board have front-panel connectors. The details of these are as follows:

8003.2:

CON1 'RS232' 9-way Micro-D Connector for the RS232 signals from the PC16550DV UART device.

Pins 1, 2, 3, 4, 5:	GND
Pin 6:	Clear to Send (CTS) Input
Pin 7:	Serial Data Input
Pin 8:	Serial Data Output
Pin 9:	Request to Send (RTS) Output.

Note: The 16550 can be programmed to ignore the state of the CTS input.

Connector part number: ITT Cannon MDSM-9PE-Z10-VR1; Electrospeed 17-0628K. Mating connector ITT Cannon MDSM-9SC-Z11-VS1; Electrospeed 17-0631F with crimp contacts MDS-S-H; Electrospeed 17-0634B..

CON3 'SSP0' 15-way Micro-D Connector for the TTL signals from the SHARC Synchronous Serial Port 0.

Pin 1:	GND
Pin 2:	Transmit Data Output (DT0)
Pin 3:	Receive Data Input (DR0)
Pin 4:	Transmit Clock Output (TCLK0)
Pin 5:	Receive Clock Input (RCLK0)
Pin 6:	Transmit Frame Sync. Output (TFS0)
Pin 7:	Receive Frame Sync. Input (RFS0)
Pins 8-15	No Connect.

Connector part number: ITT Cannon MDSM-15PE-Z10-VR1; Electrospeed 17-0629E. Mating connector ITT Cannon MDSM-15SC-Z11-VS1; Electrospeed 17-0632A with crimp contacts MDS-S-H; Electrospeed 17-0634B.

CON4 'SSP1' 15-way Micro-D Connector for the TTL signals from the SHARC Synchronous Serial Port 1.

Pin 1:	GND
Pin 2:	Transmit Data Output (DT1)
Pin 3:	Receive Data Input (DR1)
Pin 4:	Transmit Clock Output (TCLK1)
Pin 5:	Receive Clock Input (RCLK1)
Pin 6:	Transmit Frame Sync. Output (TFS1)
Pin 7:	Receive Frame Sync. Input (RFS1)
Pins 8-15	No Connect.

8003.3:

CON 2, CON3, CON4 Double-stacked 2 x 15-way Micro-D Connectors for the LVDS signals from SHARC Link Ports 0 and 1, 2 and 3 and 4 and 5 respectively.

Each of the six connector parts has the same pinout as follows:-

Pin 1:	GND
Pin 9:	Link Clock (-)
Pin 2:	Link Clock (+)
Pin 10:	Link Acknowledge (-)
Pin 3:	Link Acknowledge (+)
Pin 11:	Link Data Bit 2 (-)
Pin 4:	Link Data Bit 2 (+)
Pin 12:	Link Data Bit 3 (-)
Pin 5:	Link Data Bit 3 (+)
Pin 13:	Link Data Bit 0 (-)
Pin 6:	Link Data Bit 0 (+)
Pin 14:	Link Data Bit 1 (-)
Pin 7:	Link Data Bit 1 (+)
Pin 8:	VCC through a zero ohm resistor.
Pin 15:	No Connect.

Connector part number: ITT Cannon MDSM-30PE-Z10-VR22; Electrospeed 17-54859D. Mating connectors (2 off required for each) ITT Cannon MDSM-15SC-Z11-VS1; Electrospeed 17-0632A with crimp contacts MDS-S-H; Electrospeed 17-0634B.

APPENDIX A PCB JUMPERS

Hytec 8003 SHARC IP Carrier Board

J1 Connects the common strobe line from the Xilinx to Industry Pack C Logic Connector pin 46.
J2 Must be **IN** Factory set.
J3 Connects the common strobe line from the Xilinx to Industry Pack A Logic Connector pin 46.
J4 Supplies switched and fused +5V to pins P2 A32 and P2 C32 (Delivered Not selected).
J5 Connects the common strobe line from the Xilinx to Industry Pack B Logic Connector pin 46.
J6 – J10 Base address setting: Used to select either Geographical Addressing or jumper setting. Make according to required A11-A15 base address as follows:

	Fitted AUTO	Fitted MANUAL	Not fitted
J6	A11 must match GA0	A11 must be ‘0’	A11 must be ‘1’
J7	A12 must match GA1	A12 must be ‘0’	A12 must be ‘1’
J8	A13 must match GA2	A13 must be ‘0’	A13 must be ‘1’
J9	A14 must match GA3	A14 must be ‘0’	A14 must be ‘1’
J10	A15 must match GA4	A15 must be ‘0’	A15 must be ‘1’

J11 Connects the common strobe line from the Xilinx to Industry Pack D Logic Connector pin 46.
J12 Must be **IN** Factory set.
J13, J14 Set the SHARC processor start-up mode. See section 6.
J15 SHARC JTAG test disable – should be fitted unless using the JTAG test port.
J16 LVDS SHARC Link Port 0 RX/TX select – link centre pin to either TX or RX.
J19 LVDS SHARC Link Port 1 RX/TX select – link centre pin to either TX or RX.
J17 LVDS SHARC Link Port 2 RX/TX select – link centre pin to either TX or RX.
J20 LVDS SHARC Link Port 3 RX/TX select – link centre pin to either TX or RX.
J18 LVDS SHARC Link Port 4 RX/TX select – link centre pin to either TX or RX.
J21 LVDS SHARC Link Port 5 RX/TX select – link centre pin to either TX or RX.
J22 Write protects SHARC memory areas from VME – IN = write protect.

Note: The reference to the ‘Common Strobe Line’ refers to the front panel Inhibit signal which is passed through by the Xilinx unprocessed, thus asserting the Inhibit input low will drive all connected IP logic connector pins 46 low.

APPENDIX B Carrier Board Configuration ROM

Address Offset	Value	Definition
0x03	C1	Check Sum
0x07	00	Length of ID ROM MSB
0x0B	02	Length of ID ROM
0x0F	00	Length of ID ROM LSB
Configuration ROM data access width		
0x13	0x83	
CSR data access width		
0x17	0x83	
CSR space Specification ID		
0x1B	0x02	VME64x-1997
Identify a Valid CR		
0x1F	0x43	'C'
0x23	0x52	'R'
Manufacturer's ID		
0x27	0x00	
0x2B	0x80	
0x2F	0x03	
Board ID		
0x33	0x80	
0x37	0x03	
0x3B	0x00	
0x3F	0x00	Board build 0,1, 2 or 3.
Revision ID		
0x43	0x03	PCB issue
0x47	0x06	Xilinx version
0x4B	0x00	Xilinx revision nos
0x4F	0x03	Xilinx revision nos
ASCII string null terminated or 0x000000		
0x53	0x00	
0x57	0x00	
0x5B	0x00	
Reserved for future use		
0x5F to 0x7B		
Program ID code		
0x7F	0x01	No program, ID ROM only
Start of user defined area		
0x80		
Board Serial Number		
0xCB, 0xCF, 0xD3	0x	BEG_SN MSB
0xD7, 0xDB, 0xDF	0x	END_SN LSB
AM code mask		
0x123.. 0x13F	0x2200220000002200	AM codes 3D, 39, 2D, 29, 0D, 09

Reading the Configuration ROM using A16 (AM29h and AM2Dh) or A24 (AM39h and AM3Dh) the address is VME base address + 0x0600h, the Configuration ROM offset.

APPENDIX C ID PROM Registers (GreenSpring Format)

Address Offset	Value	Definition
0x481	0x49	ASCII “I”
0x483	0x50	ASCII “P”
0x485	0x41	ASCII “A”
0x487	0x43	ASCII “C”
0x489	0x80	Manufacturer’s ID
0x48B	0x83	Model Number
0x48D	0x0x	Revision
0x48F	0x00	Reserved
0x491	0x00	Driver ID, low byte
0x493	0x00	Driver ID, high byte
0x495	0x0C	No of bytes used
0x487		CRC

PRODUCT SPECIFICATIONS

Power Requirements
+5V @ 600mA typical
+12V @ 30mA
-12V @ 30mA
+3.3V @ approx 10mA
Additional power maybe consumed by Industry Packs.

Operating Temperature Range
0 to +45 deg Celsius ambient.

Mechanical
6U single width VME module with access to 5 row P0, P1 and P2 connectors.

IP Memory Mapping
VME Access A32:D16:D8 (EO) AM Codes: 09h and 0Dh.

IP I/O Mapping
VME Access A16:D16:D8 (EO) AM Codes: 29h and 2Dh.
VME Access A24:D16:D8 (EO) AM Codes: 39h and 3Dh.

Front Panel Indicators and Inputs

'VME'	LED (green)	Illuminates for a minimum of 20msecs whenever the module is accessed via the VME bus.
'Not Configured	LED (blue)	Indicates the state of the VME module during hot swap operation.
IP ACK	4 LED's (red)	Indicate when an IP card has sent an ACK.

Front Panel Inputs

Inhibit Single TTL. This input has a 10K pull-up resister to 5Volt supply.
Connector type: LEMO RA0302

VME64x PIN ASSIGNMENTS

ROW A	SIG	ROW B	SIG	ROW C	SIG	ROW D	SIG	ROW E	SIG	ROW F	SIG
P0.A01	IODO1	P0.B01	IOD02	P0.C01	IOD03	P0.DO1	IOD04	P0.E01	IOD05	P0.F01	GND
P0.A02	IOD06	P0.B02	IOD07	P0.C02	IOD08	P0.D02	IOD09	P0.E02	IODlO	P0.F02	GND
P0.A03	IOD11	P0.B03	IOD12	P0.C03	IOD13	P0.D03	IOD14	P0.E03	IOD15	P0.F03	GND
P0.A04	IOD16	P0.B04	IOD17	P0.C04	IOD18	P0.D04	IOD19	P0.E04	IOD20	P0.F04	GND
P0.A05	IOD21	P0.B05	IOD22	P0.C05	IOD23	P0.D05	IOD24	P0.E05	IOD25	P0.F05	GND
P0.A06	IOD26	P0.B06	IOD27	P0.C06	IOD28	P0.D06	IOD29	P0.E06	IOD30	P0.F06	GND
P0.A07	IOD31	P0.B07	IOD32	P0.C07	IOD33	P0.D07	IOD34	P0.E07	IOD35	P0.F07	GND
P0.A08	IOD36	P0.B08	IOD37	P0.C08	IOD38	P0.D08	IOD39	P0.E08	IOD40	P0.F08	GND
P0.A09	IOD41	P0.B09	IOD42	P0.C09	IOD43	P0.D09	IOD44	P0.E09	IOD45	P0.F09	GND
P0.A10	IOD46	P0.B10	IOD47	P0.C10	IOD48	P0.D10	IOD49	P0.E10	IOD50	P0.F10	GND
P0.A11	IOC01	P0 B11	IO002	P0.C11	IOC03	P0.D11	IOC04	P0 E11	IOC05	P0.F11	GND
P0.A12	IOC06	P0.B12	IO007	P0.C12	IOC08	P0.D12	IOC09	P0.E12	IOC10	P0.F12	GND
P0.A13	IOC11	P0.B13	IO012	P0.C13	IOC13	P0.D13	IOC14	P0.E13	IOC15	P0.F13	GND
P0.A14	IOC16	P0.B14	IO017	P0.C14	IOC18	P0.D14	IOC19	P0.E14	IOC20	P0.F14	GND
P0.A15	IOC21	P0.B15	IOC22	P0.C15	IOC23	P0.D15	IOC24	P0.E15	IOC25	P0.F15	GND
P0.A16	IOC26	P0.B16	IO027	P0.C16	IOC28	P0.D16	IOC29	P0.E16	IOC30	P0.F16	GND
P0.A17	IOC31	P0.B17	IO032	P0.C17	IOC33	P0.D17	IOC34	P0.E17	IOC35	P0.F17	GND
P0.A18	IOC36	P0.B18	IO037	P0.C18	IOC38	P0.D18	IOC39	P0.E18	IOC40	P0.F18	GND
P0.A19	IOC41	P0.B19	IO042	P0.C19	IOC43	P0.D19	IOC44	P0.E19	IOC45	P0.F19	GND

P0 pin assignments

P1 ROW A	SIGNAL	P1 ROW B	SIGNAL	P1 ROW C	SIGNAL	P1 ROW D	SIGNAL	P1 ROW Z	SIGNAL
P1.A01	D00	P1.B01	N/C	P1.C01	D08	P1.D01	N/C	P1.Z01	N/C
P1.A02	D01	P1.B02	N/C	P1.C02	D09	P1.D02	N/C	P1.Z02	GND
P1.A03	D02	P1.B03	N/C	P1.C03	D10	P1.D03	N/C	P1.Z03	N/C
P1.A04	D03	P1.B04	BG0IN*	P1.C04	D11	P1.D04	N/C	P1.Z04	GND
P1.A05	D04	P1.B05	BG0OUT*	P1.C05	D12	P1.D05	N/C	P1.Z05	N/C
P1.A06	D05	P1.B06	BG1IN*	P1.C06	D13	P1.D06	N/C	P1.Z06	GND
P1.A07	D06	P1.B07	BG1OUT*	P1.C07	D14	P1.D07	N/C	P1.Z07	N/C
P1.A08	D07	P1.B08	BG2IN*	P1.C08	D15	P1.D08	N/C	P1.Z08	GND
P1.A09	GND	P1.B09	BG2OUT*	P1.C09	GND	P1.D09	N/C	P1.Z09	N/C
P1.A10	N/C	P1.B10	BG3IN*	P1.C10	N/C	P1.D10	N/C	P1.Z10	GND
P1.A11	GND	P1.B11	BG3OUT*	P1.C11	BERR*	P1.D11	N/C	P1.Z11	N/C
P1.A12	DS1*	P1.B12	N/C	P1.C12	RESET	P1.D12	+3.3V	P1.Z12	GND
P1.A13	DS0*	P1.B13	N/C	P1.C13	LWORD*	P1.D13	N/C	P1.Z13	N/C
P1.A14	WRITE	P1.B14	N/C	P1.C14	AM5	P1.D14	+3.3V	P1.Z14	GND
P1.A15	GND	P1.B15	N/C	P1.C15	A23	P1.D15	N/C	P1.Z15	N/C
P1.A16	DTACK*	P1.B16	AM0	P1.C16	A22	P1.D16	+3.3V	P1.Z16	GND
P1.A17	GND	P1.B17	AM1	P1.C17	A21	P1.D17	N/C	P1.Z17	N/C
P1.A18	AS	P1.B18	AM2	P1.C18	A20	P1.D18	+3.3V	P1.Z18	GND
P1.A19	GND	P1.B19	AM3	P1.C19	A19	P1.D19	N/C	P1.Z19	N/C
P1.A20	IACK	P1.B20	GND	P1.C20	A18	P1.D20	+3.3V	P1.Z20	GND
P1.A21	IACKIN*	P1.B21	N/C	P1.C21	A17	P1.D21	N/C	P1.Z21	N/C
P1.A22	IACKOUT	P1.B22	N/C	P1.C22	A16	P1.D22	+3.3V	P1.Z22	GND
P1.A23	AM4	P1.B23	GND	P1.C23	A15	P1.D23	N/C	P1.Z23	N/C
P1.A24	A07	P1.B24	IRQ7*	P1.C24	A14	P1.D24	+3.3V	P1.Z24	GND
P1.A25	A06	P1.B25	IRQ6*	P1.C25	A13	P1.D25	N/C	P1.Z25	N/C
P1.A26	A05	P1.B26	IRQ5*	P1.C26	A12	P1.D26	+3.3V	P1.Z26	GND
P1.A27	A04	P1.B27	IRQ4*	P1.C27	A11	P1.D27	N/C	P1.Z27	N/C
P1.A28	A03	P1.B28	IRQ3*	P1.C28	A10	P1.D28	+3.3V	P1.Z28	GND
P1.A29	A02	P1.B29	IRQ2*	P1.C29	A09	P1.D29	N/C	P1.Z29	N/C
P1.A30	A0l	P1.B30	IRQ1*	P1.C30	A08	P1.D30	+3.3V	P1.Z30	GND
P1.A31	-12V	P1.B31	N/C	P1.C31	+12V	P1.D31	N/C	P1.Z31	N/C
P1.A32	+5V	P1.B32	+5V	P1.C32	+5V	P1.D32	+5V	P1.Z32	GND

P1 Pin Assignments

ROWA	SIG	ROWB	SIG	ROWC	SIG	ROWD	SIG	ROWZ	SIG
P2.A01	IOB41	P2.B01	+5V	P2.C01	IOB42	P2.D01	IOC47	P2.Z01	IOC46
P2.A02	IOB43	P2.B02	GND	P2.C02	IOB44	P2.D02	IOC48	P2.Z02	GND
P2.A03	IOB45	P2.B03	N/C	P2.C03	IOB46	P2.D03	IOC50	P2.Z03	IOC49
P2.A04	IOB47	P2.B04	A24	P2.C04	IOB48	P2.D04	IOB0l	P2.Z04	GND
P2.A05	IOB49	P2.B05	A25	P2.C05	IOB50	P2.D05	IOB03	P2.Z05	IOB02
P2.A06	IOA01	P2.B06	A26	P2.C06	IOA02	P2.D06	IOB04	P2.Z06	GND
P2.A07	IOA03	P2.B07	A27	P2.C07	IOA04	P2.D07	IOB06	P2.Z07	IOB05
P2.A08	IOA05	P2.B08	A28	P2.C08	IOA06	P2.D08	IOB07	P2.Z08	GND
P2.A09	IOA07	P2.B09	A29	P2.C09	IOA08	P2.D09	IOB09	P2.Z09	IOB08
P2.A10	IOA09	P2.B10	A30	P2.C10	IOA10	P2.D10	IOB10	P2.Z10	GND
P2.A11	IOA11	P2.B11	A31	P2.C11	IOA12	P2.D11	IOB12	P2.Z11	IOB11
P2.A12	IOA13	P2.B12	GND	P2.C12	IOA14	P2.D12	IOB13	P2.Z12	GND
P2.A13	IOA15	P2.B13	+5V	P2.C13	IOA16	P2.D13	IOB15	P2.Z13	IOB14
P2.A14	IOA17	P2.B14	N/C	P2.C14	IOA18	P2.D14	IOB16	P2.Z14	GND
P2.A15	IOA19	P2.B15	N/C	P2.C15	IOA20	P2.D15	IOB18	P2.Z15	IOB17
P2.A16	IOA21	P2.B16	N/C	P2.C16	IOA22	P2.D16	IOB19	P2.Z16	GND
P2.A17	IOA23	P2.B17	N/C	P2.C17	IOA24	P2.D17	IOB21	P2.Z17	IOB20
P2.A18	IOA25	P2.B18	N/C	P2.C18	IOA26	P2.D18	IOB22	P2.Z18	GND
P2.A19	IOA27	P2.B19	N/C	P2.C19	IOA28	P2.D19	IOB24	P2.Z19	IOB23
P2.A20	IOA29	P2.B20	N/C	P2.C20	IOA30	P2.D20	IOB25	P2.Z20	GND
P2.A21	IOA31	P2.B21	N/C	P2.C21	IOA32	P2.D21	IOB27	P2.Z21	IOB26
P2.A22	IOA33	P2.B22	GND	P2.C22	IOA34	P2.D22	IOB28	P2.Z22	GND
P2.A23	IOA35	P2.B23	N/C	P2.C23	IOA36	P2.D23	IOB30	P2.Z23	IOB29
P2.A24	IOA37	P2.B24	N/C	P2.C24	IOA38	P2.D24	IOB31	P2.Z24	GND
P2.A25	IOA39	P2.B25	N/C	P2.C25	IOA40	P2.D25	IOB33	P2.Z25	IOB32
P2.A26	IOA41	P2.B26	N/C	P2.C26	IOA42	P2.D26	IOB34	P2.Z26	GND
P2.A27	IOA43	P2.B27	N/C	P2.C27	IOA44	P2.D27	IOB36	P2.Z27	IOB35
P2.A28	IOA45	P2.B28	N/C	P2.C28	IOA46	P2.D28	IOB37	P2.Z28	GND
P2.A29	IOA47	P2.B29	N/C	P2.C29	IOA48	P2.D29	IOB39	P2.Z29	IOB38
P2.A30	IOA49	P2.B30	N/C	P2.C30	IOA50	P2.D30	IOB40	P2.Z30	GND
P2.A31	+3.3V	P2.B31	GND	P2.C31	+3.3V	P2.D31	N/C	P2.Z31	+3.3V
P2.A32	Out+5V	P2.B32	+5V	P2.C32	Out+5V	P2.D32	+5V	P2.Z32	GND

P2 pin assignments

	Denotes pins with thickened tracks which can be used for power inputs

Note:
'Out+5V' is provided by the 8003 board and can be put on to the pins by fitting jumper J4.