HYTEC ELECTRONICS Ltd
5 CRADOCK ROAD, READING, BERKS. RG2 0JT, UK

Telephone: +44 (0) 118 9757770 Fax: +44 (0)118 9757566

E-mail: sales@hytec-electronics.co.uk

ADC8401
8-CHANNEL 16-BIT ADC
INDUSTRY PACK

USERS MANUAL

PCB Issue 5
Xilinx Version 8401V516 - 8401V517
8MHz or 32MHZ IP Clock

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Author: MRN

CONTENTS

1. INTRODUCTION

The Hytec IP-ADC-8401 is a single-width Industry Pack that can run at 8MHz or 32MHz and provides 8 channels of simultaneously sampled analogue to digital conversion with the following characteristics:-

- 8 independently programmed channels
- Full 16 bits resolution
- Single full-scale trim
- Low offset error - +/- 6 LSBs max
- Low gain error - +/- 0.05% full scale
- Low error drift - 10ppm per deg C
- Code format 000Fh = –10v, 8000h = 0V and FFF1h = +10V.
- High input impedance – 10Mohms min.
- Good CMRR – 80dB
- Up to 100KHz sampling rate
- Simultaneous sampling – 2us acquisition time
- System to plant isolation to 100V when externally powered by DC/DC converter option
- 2Mbytes SRAM
- Serial number, PCB issue and firmware issue held in ID PROM

2. PRODUCT SPECIFICATIONS

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of channels:	8
ADC resolution:	16 bits
Diff. Non-linearity:	Monotonic to 15 bits (at 50kHz throughput)
Int. Non-linearity:	+/-0.012% of full scale (at 50kHz throughput)
Offset error:	+/-6LSBs With soft cal applied +/-!!mV max at 22 deg C ambient
Offset drift:	+/-10uV per deg C typical
Gain error:	+/-0.05% With soft cal +/-0.01% at 22 deg C ambient
Gain drift:	10 ppm per deg C typical
Range:	+/-10V full-scale
Overvoltage:	Protected to +/-40V differential
Bandwidth:	1MHz
Throughput:	100KHz max
Conversion time:	6.4us
Acquisition time:	2us
Slew rate:	Equivalent to 4V per us
Settling time:	18us to 0.01% of full scale
SNR:	80dB at 10kHz typical
SINAD:	80dB at 10kHz typical
Isolation:	100V via opto-isolators (if externally powered)
ADC device:	Burr-Brown ADS 8320
Data format:	16 bits straight binary
Memory:	1M x 16 bits (128K conversions per channel).
Power:	+5V @ 300mA typical +/-12V @ 200mA typical when switched to internal

3. Operating Modes

There are three operating modes:-
1. DC sampling – when the pack is armed the inputs are sampled at the programmed clock rate.
2. Triggered sampling – the inputs are sampled for the programmed number of samples and clock rate.
3. Register mode – the last ADC reading may be read at random.

4. Memory Map

There are two main conversion memories of 512k samples each (lower and upper buffers)
These are each divided into eight segments allocated to conversions from ADC1 to ADC8.
When the lower buffer has been filled the Half Full Flag status is set and when the upper memory is full the Full Flag status is set.

Lower Conversion Memory	Upper Conversion Memory
ADC8 conversions	ADC8 conversions
ADC7 conversions	ADC7 conversions
ADC6 conversions	ADC6 conversions
ADC5 conversions	ADC5 conversions
ADC4 conversions	ADC4 conversions
ADC3 conversions	ADC3 conversions
ADC2 conversions	ADC2 conversions
ADC1 conversion 64k ADC1 conversion 64k-1 ADC1 conversion 2 ADC1 conversion 1	ADC1 conversion 128k ADC1 conversion 128k-1 ADC1 conversion 64k+2 ADC1 conversion 64k+1

4.1 Memory Size

A bit in the control register of the 8401 allows selection of either 1Mb memory (64K samples/channel) when set at logic 1 or 2Mb (128K samples/channel) when set at logic 0.

5. ADC Register Read Out

There are eight ADC buffer registers (addresses 10hex – 1Ehex) which store the last sampled conversions and may be read at any time. The channel order is channel 1 at address 10hex to channel 8 at address 1E.
Data format 000Fh = –10v, 8000h = 0V and FFF0h = +10V.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0

6. Application Registers

There are five application specific (I/O) registers; the CSR, the number of samples per trigger (NCO), the memory conversion pointer, the clock rate and the interrupt vector value. There are also 8 ADC buffer registers.

6.1 Control & Status Register (CSR)

6.2 Control

Write Address: 0hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ARM	EX	ST	XC	ET	EE	FE	HE	1M	DA	EII	MII	x	CC	F	HF

Status

Read Address: 0hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ARM	EX	ST	XC	ET	EE	FE	HE	1M	DA	EII	MII	MIS	CC	F	HF

ARM Arm the ADCs. Allow conversions either continuous or triggered.

EX Enable trigger. If not set continuously sample at the clock rate. If set allows external trigger or software trigger

ST Software trigger. Triggers a programmed number of samples. ST is cleared on completion.

XC Enable the external clock. If 0 the internal clock is used for the sample rate. If set true the external clock is used for the sample clock without frequency division.

ET When logic '0' disable hardware memory inhibit input. When logic '1' enable hardware memory inhibit from IP **Strobe*** line *(on Hytec 800x IP carrier card, this signal is driven from the front panel INHIBIT lemo)*.

EE Enables interrupt at end of sampling sequence.

FE Enables interrupt when the upper conversion memory has been filled. (Memory Full).

HE Enables interrupt when the lower conversion memory has been filled. (Memory Half Full).

1M Enables 1Mb memory (64K samples/channel) when logic 1 and 2Mb (128K samples/channel) when logic 0.

DA Set to 1 allows the unit to disarm on completion of memory acquisition

EII This enables an interrupt to be generated when ever the memory inhibit bit (MIS) is set.

MII **(Write)** When set to logic '1' hardware memory inhibit interrupt is cleared but not disabled. **(Read)** Shows that an interrupt has been generated from hardware memory inhibit.

MIS **(Read Only)** this bit indicates that the hardware memory inhibited on the IP **Strobe*** line is asserted when at logic '1' (*driven from the front panel INHIBIT lemo on Hytec 800x IP carriers)*.

CC Conversions complete. Status bit set when the number of programmed samples has been completed. Generates IRQ0* if set and EE is set to a logic 1.

F Full status. Set when the upper conversion memory has been filled. Generates IRQ0* if set and FE is set to a logic 1.

HF Half full status. Set when the lower conversion memory has been filled. Generates IRQ0* if set and HE is set to a logic 1.

6.3 Conversion Pointer

Read/write Address: 2hex
The current conversion address is given by the conversion address offset by the ADC number. This register can be written too when the unit is ARMed.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

6.4 Number of conversions

Read/write Address: 4hex
The number of conversions register allows the number of samples per trigger to be programmed.
The maximum number of conversions is FFFFhex which gives 64K (1MB memory size) or 128K (2MB memory size) of samples per channel before an interrupt is generated.
If a number of triggers occur and the memory buffer size of 128K of conversions per channel is exceeded the conversions will wrap around from the upper memory to the base of the lower memory.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

6.5 Clock Rate/IP Clock Speed Select

Read/write Address: 6hex
The clock rate register is the first four bits which enables codes 0 – 15 to enable frequencies of 1 Hz to 100kHz in multiples of 1,2,5 or 10. (E.g. 0=1Hz, 1=2Hz, 2=5Hz, 3=10Hz and so on) Each clock pulse will initiate simultaneous ADC conversions and store them in memory.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
S15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	S3	S2	S1	S0

The clock speed the IP will run at is set by the top bit S15. 0=8MHz and 1=32MHz.

6.6 Vector

Read/write Address: 8hex
The vector register is a 16 bit register which stores the interrupt vector value.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

6.7 Extended Control & Status Register (CSR Ext)

Read/write Address: Ahex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	ISE	IS	SMI	TEN

TEN This shows the trigger status of the unit (Read only).
SMI This sets **S**oftware **M**emory **I**nhibit when at logic '1'. This does not generate an interrupt or set the MIS in the CSR.
IS **Read** -ADC Register update status. Set when the ADC Registers have been updated. Generates IRQ0* if set and ISE is set to a logic 1.
Write-When a logic '1' written clears IS generated interrupt is cleared but not disabled.
ISE Enables interrupt when ADC Registers have been updated.

6.8 ADC Registers

Read only Address: 10hex – 1Ehex
The eight ADC buffer registers store the last sample conversions and may be read at any time.
Data format 000Fh = –10v, 8000h = 0V and FFF1h = +10V.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

7. ADC OPERATION

7.1 Memory Update Inhibit and Interrupt

The updating of the conversion memory can be stopped by controlling the external IP **Strobe*** line *(on the Hytec 8002 IP carrier card, this signal is driven from the front panel INHIBIT lemo)*.
When the STROBE line is taken low and the enable hardware memory inhibit bit (ET) is set in CSR the updating of the conversion memory is stopped. This is indicated by the MIS bit in the CSR going high.
On memory update inhibit an interrupt can be generated if the **E**nable Memory **I**nhibit **I**nterrupt enable bit (EII) is set in the CSR. The **M**emory **I**nhibit **I**nterrupt (MII) bit of the CSR flags an interrupt. This is cleared by either clearing the EII in the CSR or by writing a '1' to MII bit in the CSR which clears the Memory Inhibit Interrupt without the need to clear the EII in the CSR.

7.2 Set Number of Conversions

The number of conversions register (NCO) at address 2hex allows the number of samples per trigger to be programmed. The maximum number of conversions is FFFFhex which gives 64K of samples 1MB and 128K of samples for 2MB for each channel before the Conversion Complete (CC) flag is set in the CSR.
An interrupt is generated if the Enable Interrupt on Last Sample (EE) bit is set in the CSR. To clear the interrupt write a '0' to the CC bit of the CSR.
If a number of triggers occur and the memory buffer size of 128K of conversions per channel is exceeded the conversions will wrap around from the upper memory to the base of the lower memory.

7.2.1 Number of Conversions set with External clock

When the number of conversions is set and the external clock is used to acquire data the number of clocks required before an interrupt is generated is one more than the number of samples required (as set in the NCO).
i.e. If number of samples required is 8 (NOC is set to 8) then need to supply 8 clock pulses before interrupt is generated 1MB memory size and 16 clk pulses for 2MB memory size.

7.3 Triggering

The triggering of the ADC8401 is only used when the number of conversions has been set in the Number of Conversions register and the Enable Trigger (EX) bit has been set in the CSR.

7.3.1 Software Trigger

The unit can be triggered by a software trigger by writing a '1' to the Software Trigger (ST) bit of the CSR.

7.3.2 Hardware Trigger

The external trigger is passed to the ADC8401 via designated pins see Appendices B, C and D.

7.4 Memory Update

All ADC channels are updated simultaneously and the memory pointer incremented. Therefore the memory pointer indicates what memory location has been reached by all the ADCs by adding the channel number to the pointer value with the channel number as the most significant bit.
E.g:- Channel 1 = xxxx Channel 2 = 1xxxx Channel 3 = 2xxxx etc.

With 2Mb operation it is necessary to include the half full flag to see whether the pointer is addressing lower or upper memory space.
E.g:- Channel 1 = xxxx Channel 2 = 1xxxx Channel 3 = 2xxxx when HF=0 for lower memory
Channel 1 = 8xxxx Channel 2 = 9xxxx Channel 3 = Axxxx when HF=1 for upper memory

8. ID PROM

The word addresses are as below:-

Base+80	ASCII 'VI'	5649h	
Base+82	ASCII 'TA'	5441h	
Base+84	ASCII '4 '	3420h	
Base+86	Hytec ID high byte	0080h	
Base+88	Hytec ID low word	0300h	
Base+8A	Model number	8401h	
Base+8C	Revision	5517h	This shows PCB Iss 5 Xilinx V517
Base+8E	Reserved	0000h	
Base+90	Driver ID	0000h	
Base+92	Driver ID	0000h	
Base+94	Flags	0006h	This shows 8MHz and 32MHz operation
Base+96	No of bytes used	001Ah	
Base+98	Cal Type	xxxxh	0 = No Calibration factors, 2 = Calibration factors Stored.
Base+9A	Serial Number	xxxxdec	
Base+9C	Not used	0000h	
Base+9E	WLO	5555h	
Base+A0	CH1 Cal data nFS	xxxxh	Neg Full Scale (-10Volts) Calibration Factor
Base+A2	CH1 Cal data nHS	xxxxh	Neg Half Scale (-5Volts) Calibration Factor
Base+A4	CH1 Cal data Zero	xxxxh	Zero (0 Volts) Calibration Factor
Base+A6	CH1 Cal data pHS	xxxxh	Pos Half Scale (+5Volts) Calibration Factor
Base+A8	CH1 Cal data pFS	xxxxh	Pos Full Scale (+10Volts) Calibration Factor
	:		
	:		
	:		
Base+E6	CH8 Cal data nFS	xxxxh	Neg Full Scale (-10Volts) Calibration Factor
Base+E8	CH8 Cal data nHS	xxxxh	Neg Half Scale (-5Volts) Calibration Factor
Base+EA	CH8 Cal data Zero	xxxxh	Zero (0 Volts) Calibration Factor
Base+EC	CH8 Cal data pHS	xxxxh	Pos Half Scale (+5Volts) Calibration Factor
Base+EE	CH8 Cal data pFS	xxxxh	Pos Full Scale (+10Volts) Calibration Factor

9. CALIBRATION

The type of calibration factors held in the ID PROM are specified by the Cal Type held at Base+98 in the ID PROM:-

0 = No Calibration factors held in ID PROM
2 = Calibration factors Stored in ID PROM

The Calibration Factors are held in the ID PROM as shown above in SECTION 8 starting at Base+A0. These values and are derived from reading the ADC values at specified voltages.
For the nFS value -10Volts is applied and the hex values from the ADC is stored and this is repeated for nHS at -5volts, zero at 0volts, pHS at +5Volts and pFS at +10volts.
These values can then be used in the following equations to correct the offset and gain errors of the individual cannels of the ADC8401 IP card.

$$rawval > pHS$$

$$CalVal = \frac{(rawval - pHS) \times 0x3FF8}{pFS - pHS} + BFF8$$

$$0 < rawval \leq pHS$$

$$CalVal = \frac{(rawval - zero) \times 0x3FF8}{pHS - zero} + 8000$$

$$rawval < nHS$$

$$CalVal = \frac{(rawval - nHS) \times 0x3FF9}{nHS - nFS} + 4007$$

$$0 > rawval \geq nHS$$

$$CalVal = \frac{(rawval - zero) \times 0x3FF9}{zero - nHS} + 8000$$

10. SELECTION OF THE +/-12 VOLT POWER SUPPLY

The ADC 8401 +/-12 volt power supply can be derived either internally from the carrier card or from an external source via a transition card. The source is selected using jumpers J1, J2 and the GND AGND link where:

J1 External +12V connect 1 & 2, Internal +12V connect 2 & 3
J2 External -12V connect 1 & 2, Internal -12V connect 2 & 3

GND AGND Link
IN for internal +/-12V
OUT for external +/-12V (supplied from transition card DC DC converter).

11. EPICS Software Driver

EPICS software driver written for the 8401 8 channel ADC Industry Pack on 8002 Carrier Board with 8201 Transition Board.
For down loads go to:
http://www.hytec-electronics.co.uk/Download.aspx

IMPORTANT NOTE

The 8401 ADC issue 5 PCB should not be operated with only one of the 12Volt power rail connected as this may cause damage to the unit. This situation can be caused by incorrect setting of the jumpers J1 or J2 which set the source of the +/-12Volt supplies to the 8401 ADC card.

Power supply in balance will occur if:

1. **one of the jumpers is set to select the 12Volt from an isolated power supply which is not fitted and the other being set for internal 12Volt supply.**
2. **one of the jumpers is not fitted.**

APPENDIX A

PCB JUMPERS

Issue 3 PCB
J1 Factory set
J2 External +12V connect 1 & 2, Internal +12V connect 2 & 3
J3 External -12V connect 1 & 2, Internal -12V connect 2 & 3

Issue 5 PCB
J1 External +12V connect 1 & 2, Internal +12V connect 2 & 3
J2 External -12V connect 1 & 2, Internal -12V connect 2 & 3
J3 Factory set

GND AGND Link
IN for internal +/-12V
OUT for external +/-12V (supplied from transition card DC DC converter).

APPENDIX B

I/O Connector – PL2 (50 way) on 8401 ADC Board

Pin	Signal	Pin	Signal
1	Input 1 +ve	26	N.C.
2	Input 1 -ve	27	N.C.
3	Input 2 +ve	28	N.C.
4	Input 2 -ve	29	N.C.
5	Input 3 +ve	30	N.C.
6	Input 3 -ve	31	N.C.
7	Input 4 +ve	32	N.C.
8	Input 4 -ve	33	N.C.
9	Input 5 +ve	34	N.C.
10	Input 5 -ve	35	XTrigger
11	Input 6 +ve	36	/XTrigger
12	Input 6 -ve	37	N.C.
13	Input 7 +ve	38	N.C.
14	Input 7 -ve	39	XClk
15	Input 8 +ve	40	/XClk
16	Input 8 -ve	41	+12VX
17	N.C.	42	AGND
18	N.C.	43	+12VX
19	N.C.	44	AGND
20	N.C.	45	-12VX
21	N.C.	46	AGND
22	N.C.	47	-12VX
23	N.C.	48	AGND
24	N.C.	49	AGND
25	N.C.	50	AGND

APPENDIX C
HYTEC TRANSITION CARD CONNECTIONS

I/O Connector – 50 way on transition

Card 8202 Where this feeds ONE IP sites

Pin	Signal	Pin	Signal
1	Chan 1 -	26	Chan 1 +
2	Chan 2 -	27	Chan 2 +
3	Chan 3 -	28	Chan 3 +
4	Chan 4 -	29	Chan 4 +
5	Chan 5 -	30	Chan 5 +
6	Chan 6 -	31	Chan 6 +
7	Chan 7 -	32	Chan 7 +
8	Chan 8 -	33	Chan 8 +
9		34	
10		35	
11		36	
12		37	
13		38	
14		39	
15		40	
16		41	
17		42	
18	XTRIG N	43	XTRIG P
19		44	
20	XCLK N	45	XCLK P
21		46	
22		47	
23		48	
24	AGND	49	AGND
25	AGND	50	AGND

I/O Connector – 50 way on transition
Card 8201 Where this feeds TWO IP sites

Pin	Signal	Pin	Signal
1	A Chan 1 -	26	A Chan 1 +
2	A Chan 2 -	27	A Chan 2 +
3	A Chan 3 -	28	A Chan 3 +
4	A Chan 4 -	29	A Chan 4 +
5	A Chan 5 -	30	A Chan 5 +
6	A Chan 6 -	31	A Chan 6 +
7	A Chan 7 -	32	A Chan 7 +
8	A Chan 8 -	33	A Chan 8 +
9	B Chan 1 -	34	B Chan 1 +
10	B Chan 2 -	35	B Chan 2 +
11	B Chan 3 -	36	B Chan 3 +
12	B Chan 4 -	37	B Chan 4 +
13	B Chan 5 -	38	B Chan 5 +
14	B Chan 6 -	39	B Chan 6 +
15	B Chan 7 -	40	B Chan 7 +
16	B Chan 8 -	41	B Chan 8 +
17		42	
18	A XTRIG N	43	A XTRIG P
19	B XTRIG N	44	B XTRIG P
20	A XCLK N	45	A XCLK P
21	B XCLK N	46	B XCLK P
22		47	
23		48	
24	A AGND	49	A AGND
25	B AGND	50	B AGND

APPENDIX D

VME64X PIN ASSIGNMENT ON HYTEC 8002 IP CARRIER BOARD FOR ADC8401

ROW A	SIG	ROW B	SIG	ROW C	SIG	ROW D	SIG	ROW E	SIG	ROW F	SIG
P0.A01	D Chan 1+	P0.B01	D Chan 1-	P0.C01	D Chan 2+	P0.DO1	D Chan 2 -	P0.E01	D Chan 3+	P0.F01	GND
P0.A02	D Chan 3 -	P0.B02	D Chan 4+	P0.C02	D Chan 4 -	P0.D02	D Chan 5+	P0.E02	D Chan 5 -	P0.F02	GND
P0.A03	D Chan 6+	P0.B03	D Chan 6 -	P0.C03	D Chan 7+	P0.D03	D Chan 7 -	P0.E03	D Chan 8+	P0.F03	GND
P0.A04	D Chan 8 -	P0.B04	N/C	P0.C04	N/C	P0.D04	N/C	P0.E04	N/C	P0.F04	GND
P0.A05	N/C	P0.B05	N/C	P0.C05	N/C	P0.D05	N/C	P0.E05	N/C	P0.F05	GND
P0.A06	N/C	P0.B06	N/C	P0.C06	N/C	P0.D06	N/C	P0.E06	N/C	P0.F06	GND
P0.A07	N/C	P0.B07	N/C	P0.C07	N/C	P0.D07	N/C	P0.E07	D XTrigger	P0.F07	GND
P0.A08	D/XTrigger	P0.B08	N/C	P0.C08	N/C	P0.D08	D XCLK	P0.E08	D /XCLK	P0.F08	GND
P0.A09	D +12V	P0.B09	D AGND	P0.C09	D +12V	P0.D09	D AGND	P0.E09	D -12V	P0.F09	GND
P0.A10	D AGND	P0.B10	D -12V	P0.C10	D AGND	P0.D10	N/C	P0.E10	D AGND	P0.F10	GND
P0.A11	C Chan 1+	P0 B11	C Chan 1 -	P0.C11	C Chan 2+	P0.D11	C Chan 2 -	P0 E11	C Chan 3+	P0.F11	GND
P0.A12	C Chan 3 -	P0.B12	C Chan 4+	P0.C12	C Chan 4 -	P0.D12	C Chan 5+	P0.E12	C Chan 5 -	P0.F12	GND
P0.A13	C Chan 6+	P0.B13	C Chan 6-	P0.C13	C Chan 7+	P0.D13	C Chan 7 -	P0.E13	C Chan 8+	P0.F13	GND
P0.A14	C Chan 8+	P0.B14	N/C	P0.C14	N/C	P0.D14	N/C	P0.E14	N/C	P0.F14	GND
P0.A15	N/C	P0.B15	N/C	P0.C15	N/C	P0.D15	N/C	P0.E15	N/C	P0.F15	GND
P0.A16	N/C	P0.B16	N/C	P0.C16	N/C	P0.D16	N/C	P0.E16	N/C	P0.F16	GND
P0.A17	N/C	P0.B17	N/C	P0.C17	N/C	P0.D17	N/C	P0.E17	C XTrigger	P0.F17	GND
P0.A18	C/XTrigger	P0.B18	N/C	P0.C18	N/C	P0.D18	C XCLK	P0.E18	C /XCLK	P0.F18	GND
P0.A19	C +12V	P0.B19	C AGND	P0.C19	C +12V	P0.D19	C AGND	P0.E19	C -12V	P0.F19	GND

P0 pin assignment

P1 ROW A	SIGNAL	P1 ROW B	SIGNAL	P1 ROW C	SIGNAL	P1 ROW D	SIGNAL	P1 ROW Z	SIGNAL
P1.A01	D00	P1.B01	N/C	P1.C01	D08	P1.D01	N/C	P1.Z01	N/C
P1.A02	D01	P1.B02	N/C	P1.C02	D09	P1.D02	N/C	P1.Z02	GND
P1.A03	D02	P1.B03	N/C	P1.C03	D10	P1.D03	N/C	P1.Z03	N/C
P1.A04	D03	P1.B04	BG0IN*	P1.C04	D11	P1.D04	N/C	P1.Z04	GND
P1.A05	D04	P1.B05	BG0OUT*	P1.C05	D12	P1.D05	N/C	P1.Z05	N/C
P1.A06	D05	P1.B06	BG1IN*	P1.C06	D13	P1.D06	N/C	P1.Z06	GND
P1.A07	D06	P1.B07	BG1OUT*	P1.C07	D14	P1.D07	N/C	P1.Z07	N/C
P1.A08	D07	P1.B08	BG2IN*	P1.C08	D15	P1.D08	N/C	P1.Z08	GND
P1.A09	GND	P1.B09	BG2OUT*	P1.C09	GND	P1.D09	N/C	P1.Z09	N/C
P1.A10	N/C	P1.B10	BG3IN*	P1.C10	N/C	P1.D10	N/C	P1.Z10	GND
P1.A11	GND	P1.B11	BG3OUT*	P1.C11	BERR*	P1.D11	N/C	P1.Z11	N/C
P1.A12	DS1*	P1.B12	N/C	P1.C12	RESET	P1.D12	+3.3V	P1.Z12	GND
P1.A13	DS0*	P1.B13	N/C	P1.C13	LWORD*	P1.D13	N/C	P1.Z13	N/C
P1.A14	WRITE	P1.B14	N/C	P1.C14	AM5	P1.D14	+3.3V	P1.Z14	GND
P1.A15	GND	P1.B15	N/C	P1.C15	A23	P1.D15	N/C	P1.Z15	N/C
P1.A16	DTACK*	P1.B16	AM0	P1.C16	A22	P1.D16	+3.3V	P1.Z16	GND
P1.A17	GND	P1.B17	AM1	P1.C17	A21	P1.D17	N/C	P1.Z17	N/C
P1.A18	AS	P1.B18	AM2	P1.C18	A20	P1.D18	+3.3V	P1.Z18	GND
P1.A19	GND	P1.B19	AM3	P1.C19	A19	P1.D19	N/C	P1.Z19	N/C
P1.A20	IACK	P1.B20	GND	P1.C20	A18	P1.D20	+3.3V	P1.Z20	GND
P1.A21	IACKIN*	P1.B21	N/C	P1.C21	A17	P1.D21	N/C	P1.Z21	N/C
P1.A22	IACKOUT	P1.B22	N/C	P1.C22	A16	P1.D22	+3.3V	P1.Z22	GND
P1.A23	AM4	P1.B23	GND	P1.C23	A15	P1.D23	N/C	P1.Z23	N/C
P1.A24	A07	P1.B24	IRQ7*	P1.C24	A14	P1.D24	+3.3V	P1.Z24	GND
P1.A25	A06	P1.B25	IRQ6*	P1.C25	A13	P1.D25	N/C	P1.Z25	N/C
P1.A26	A05	P1.B26	IRQ5*	P1.C26	A12	P1.D26	+3.3V	P1.Z26	GND
P1.A27	A04	P1.B27	IRQ4*	P1.C27	A11	P1.D27	N/C	P1.Z27	N/C
P1.A28	A03	P1.B28	IRQ3*	P1.C28	A10	P1.D28	+3.3V	P1.Z28	GND
P1.A29	A02	P1.B29	IRQ2*	P1.C29	A09	P1.D29	N/C	P1.Z29	N/C
P1.A30	A0l	P1.B30	IRQ1*	P1.C30	A08	P1.D30	+3.3V	P1.Z30	GND
P1.A31	-12V	P1.B31	N/C	P1.C31	+12V	P1.D31	N/C	P1.Z31	N/C
P1.A32	+5V	P1.B32	+5V	P1.C32	+5V	P1.D32	+5V	P1.Z32	GND

P1 Pin Assignment

ROWA	SIG	ROWB	SIG	ROWC	SIG	ROWD	SIG	ROWZ	SIG
P2.A01	B +12V	P2.B01	+5V	P2.C01	B AGND	P2.D01	C -12V	P2.Z01	C AGND
P2.A02	B +12V	P2.B02	GND	P2.C02	B AGND	P2.D02	C AGND	P2.Z02	GND
P2.A03	B -12V	P2.B03	N/C	P2.C03	B AGND	P2.D03	C AGND	P2.Z03	N/C
P2.A04	B -12V	P2.B04	A24	P2.C04	B AGND	P2.D04	B Chan 1 +	P2.Z04	GND
P2.A05	N/C	P2.B05	A25	P2.C05	B AGND	P2.D05	B Chan 2 +	P2.Z05	B Chan 1 -
P2.A06	A Chan 1 +	P2.B06	A26	P2.C06	A Chan 1 -	P2.D06	B Chan 2 -	P2.Z06	GND
P2.A07	A Chan 2 +	P2.B07	A27	P2.C07	A Chan 2 -	P2.D07	B Chan 3 -	P2.Z07	B Chan 3 +
P2.A08	A Chan 3 +	P2.B08	A28	P2.C08	A Chan 3 -	P2.D08	B Chan 4 +	P2.Z08	GND
P2.A09	A Chan 4 +	P2.B09	A29	P2.C09	A Chan 4 -	P2.D09	B Chan 5 +	P2.Z09	B Chan 4 -
P2.A10	A Chan 5 +	P2.B10	A30	P2.C10	A Chan 5 -	P2.D10	B Chan 5 -	P2.Z10	GND
P2.A11	A Chan 6 +	P2.B11	A31	P2.C11	A Chan 6 -	P2.D11	B Chan 6 -	P2.Z11	B Chan 6 +
P2.A12	A Chan 7 +	P2.B12	GND	P2.C12	A Chan 7 -	P2.D12	B Chan 7 +	P2.Z12	GND
P2.A13	A Chan 8 +	P2.B13	+5V	P2.C13	A Chan 8 -	P2.D13	B Chan 8 +	P2.Z13	B Chan 7 -
P2.A14	N/C	P2.B14	N/C	P2.C14	N/C	P2.D14	B Chan 8 -	P2.Z14	GND
P2.A15	N/C	P2.B15	N/C	P2.C15	N/C	P2.D15	N/C	P2.Z15	N/C
P2.A16	N/C	P2.B16	N/C	P2.C16	N/C	P2.D16	N/C	P2.Z16	GND
P2.A17	N/C	P2.B17	N/C	P2.C17	N/C	P2.D17	N/C	P2.Z17	N/C
P2.A18	N/C	P2.B18	N/C	P2.C18	N/C	P2.D18	N/C	P2.Z18	GND
P2.A19	N/C	P2.B19	N/C	P2.C19	N/C	P2.D19	N/C	P2.Z19	N/C
P2.A20	N/C	P2.B20	N/C	P2.C20	N/C	P2.D20	N/C	P2.Z20	GND
P2.A21	N/C	P2.B21	N/C	P2.C21	N/C	P2.D21	N/C	P2.Z21	N/C
P2.A22	N/C	P2.B22	GND	P2.C22	N/C	P2.D22	N/C	P2.Z22	GND
P2.A23	A X Trigger	P2.B23	N/C	P2.C23	A /XTrigger	P2.D23	N/C	P2.Z23	N/C
P2.A24	N/C	P2.B24	N/C	P2.C24	N/C	P2.D24	N/C	P2.Z24	GND
P2.A25	A XCLK	P2.B25	N/C	P2.C25	A /XCLK	P2.D25	N/C	P2.Z25	N/C
P2.A26	A +12V	P2.B26	N/C	P2.C26	A AGND	P2.D26	N/C	P2.Z26	GND
P2.A27	A +12V	P2.B27	N/C	P2.C27	A AGND	P2.D27	B /XTrigger	P2.Z27	B X Trigger
P2.A28	A -12V	P2.B28	N/C	P2.C28	A AGND	P2.D28	N/C	P2.Z28	GND
P2.A29	A -12V	P2.B29	N/C	P2.C29	A AGND	P2.D29	B XCLK	P2.Z29	N/C
P2.A30	N/C	P2.B30	N/C	P2.C30	A AGND	P2.D30	B /XCLK	P2.Z30	GND
P2.A31	Out+3.3V	P2.B31	GND	P2.C31	Out+3.3V	P2.D31	GND	P2.Z31	Out +3.3V
P2.A32	Out +5V	P2.B32	+5V	P2.C32	Out +5V	P2.D32	+5V	P2.Z32	GND

P2 pin assignment

Denotes pins with thickened tracks which can be used for power inputs