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DAC8402(+/-10V Output)
And
DAC8402U (0V to +10V Output)
16-CHANNEL 16-BIT DAC
INDUSTRY PACK

USERS MANUAL

PCB Issue 4.1 and Issue 5.0
Firmware Version 8402V403,
8402V405 & 8402V501

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CONTENTS

1. INTRODUCTION

The Hytec IP-DAC-8402 is a single-width Industry Pack that provides 16 channels of simultaneously updated digital to analogue conversion with the following characteristics:-

- 16 independently programmed channels
- 16 bits resolution
- 64K samples per channel
- Single offset and full-scale trims
- ***+/-10*** full scale output version Code format 0200h = –10v, 8000h = 0V and FE00h = +10V.
- ***0 to 10V*** full scale output version Code format 0000h = 0V and FE00h = +10V.
- Low offset error - +/-0.5mV typical (With soft cal applied +/-0.5mV)
- Low gain error - +/-5LSBs typical (With soft cal applied +/-2.5LSBs typ. +/-4.5LSBs max)
- Low error drift - 2ppm per deg C
- +/- 10mA current drive capability with continuous short-circuit protection
- Drives capacitive loads to 10000pF
- Straight binary code
- 20KHz update rate
- Simultaneous up-date Power-on disable (outputs set to 0V on boot up)
- System to plant isolation to 100V when externally powered
- Board serial number, PCB issue and firmware version held on ROM.
- External Triggering
- Continuous function generation.
- Internal/External update clock.
- Programmable internal update clock rates
  (20KHz,10KHz,5KHz,2KHz,1KHz,500Hz,200Hz,100Hz,50Hz,20Hz,10Hz,5Hz,2Hz and 1Hz)
- Calibration factors held on ROM.

The Hytec Industry pack type (IP 8402) which has 16 /16 bit resolution DAC's, which works via an internal serial bus, this is used primarily so that the group of 16 outputs can be optically isolated.

The unit are factory set to have an output of +/-10V or 0 to 10V. The voltage ranges are **NOT** user selectable.

2. PRODUCT SPECIFICATIONS

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of channels:	16
DAC resolution:	16 bits
Data format ***+/-10V***:	16 bits straight binary with 200h = –10.v, 8000h = 0V and FE00h = +10V
Range ***+/-10V***:	+/-10.158V full-scale
Data format ***0-10V***:	16 bits straight binary with 0000h = 0v, and FE00h = +10V
Range ***0-10V***:	+10.079V full-scale
Output current:	+/-10mA @ FS
Capacitive load:	Stable up to 10000pF
Short circuit duration:	Continuous
OverV withstand:	No internal protection from external voltages provided
Update rate:	20KHz max
Power:	+5V @ 300mA typical
	+/-12V @ 200mA typical when switched to internal
Isolation:	100V via opto-isolators (if externally powered by HYTEC 8912)
DAC device:	Linear Technology LTC1655 with serial interface
Integral non-linearity:	+/-8LSBs typ. +/-16LSBs max
Offset error:	+/-2mV max (NO SOFT CAL)
	With soft cal applied +/-0.5mV max at 22 deg C ambient
Offset drift:	+/-5uV per deg C typical
Gain error:	+/-5LSBs typ. +/-16LSBs max.
	With soft cal +/-2.5LSBs typ. +/-4.5LSBs max. at 22 deg C ambient
Output slew rate:	+/-0.7V/us typ. +/-0.3V/us min.
Settling time:	20us max.to 0.005% of final value for 1000pF load capacitance

3. Operating Modes

There are two operating modes:-

1. Registered – the DAC outputs are controlled by the contents of the DAC registers.
2. Memory – the outputs are updated for the programmed number of samples at the programmed clock rate.

All the outputs are updated serially but change together (there will be slight changes due to differences in the slew rate of the amplifiers (about +/-1uS) at the end of an internal update cycle.
The outputs may be updated at a rate of up to 20KHz. The two methods to update the 8402 DACs are detailed below.

3.1 USING REGISTER TO UP DATE DACs

Using registers there are 16 registers one per channel. These can be loaded one at a time, the module can then be ARMed and the data from the registers will be serially loaded from one DAC to the next until all the data has been passed to the DACs. At this point the DAC outputs are automatically updated giving 16 simultaneous outputs. While the unit is ARMed the DACs are constantly refreshed with the contents of the registers which can be changed during this time. There is a delay which is fixed at approximately 32us after ARM is set, before all the outputs change together.

3.2 USING MEMORY TO UP DATE DACs

In this method the memory is first loaded with the required data and the number of memory locations used is entered in to the Number of Updates (NCO) register. The Control and Status Register (CSR) is then set to enable memory updates and ARM to unit with a software command. A trigger can then be issued either by a software command or by an external trigger to start down loading the data held in memory to the DACs via the registers as detail above. In this mode the registers are updated with new data from the memory at the update clock rate which is derived either internally or externally. The memory address is automatically incremented.
When the programmed number of output has occurred the unit will stop and generate an interrupt if enabled or if set in continues mode the address counter will be zeroed and the output repeated (no interrupt generated in continues mode) until the ARM bit is cleared or the Continues bit in the CSR is cleared.

4. Memory Map

There are two main buffer memories of 512k updates each (lower and upper buffers)
These are each divided into sixteen segments allocated to updates for DAC1 to DAC16.
When DAC16 has been updated from the top of the lower buffer, the Half Full Flag status is set and when it has been updated from the top of the upper memory buffer the Full Flag status is set.

Lower Conversion Memory	Upper Conversion Memory
DAC16 conversions	DAC16 conversions
DAC15 conversions	DAC15 conversions
DAC14 conversions	DAC14 conversions
DAC13 conversions	DAC13 conversions
DAC12 conversions	DAC12 conversions
DAC11 conversions	DAC11 conversions
DAC10 conversions	DAC10 conversions
DAC9 conversions	DAC9 conversions
DAC8 conversions	DAC8 conversions
DAC7 conversions	DAC7 conversions
DAC6 conversions	DAC6 conversions
DAC5 conversions	DAC5 conversions
DAC4 conversions	DAC4 conversions
DAC3 conversions	DAC3 conversions
DAC2 conversions	DAC2 conversions
DAC1 conversion 32k DAC1 conversion 32k-1 DAC1 conversion 2 DAC1 conversion 1	DAC1 conversion 64k DAC1 conversion 64k-1 DAC1 conversion 32k+2 DAC1 conversion 32k+1

5. Application Registers

There are four application specific (I/O) registers; the CSR, the number of samples per trigger, the conversion pointer and the clock rate.

5.1 Control & Status Register (CSR)

Read/Write Address: 0hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ARM	EX	ST	XC	ET	EE	FE	HE	BS	SSU	1MB	MH	CONT	CC	F	HF

ARM Writing a '1' to ARM bit causes the values loaded in to the DAC registers or the memory (following a trigger) to be loaded in to the DACs on the next rising edge of the update clock.
When all the DACs have been updated from the registers (the EX bit set to '0') the ARM bit is cleared.
If the DACs are being updated from the memory (the EX bit set to '1') the ARM bit is not cleared.
In this mode if a number of triggers occur which cause the end of the memory to be reached, a subsequent trigger will cause the memory pointer to wrap around to the start of memory.

EX Enable trigger and memory update.
EX=0 If not set the outputs will be enabled from the registers transparently.
EX=1 If set allows external trigger or software trigger to initiate programmed updates from memory. In this mode the *Number Of Updates Register* needs to be set between 0 to 64K updates.

ST Software trigger. Triggers a programmed number of updates from the memory as set by the Number of Updates register.

XC Enable the external clock. 0 = internal clock used for the sample rate. 1 = external clock used for the sample rate.

ET When set to '1' enables signal the Inhibit Lemo of the 8002 via the IP Strobe line. The Inhibit signal when set stops the updating DAC from memory.

EE Enables interrupt at end of programmed number of DAC updates from memory.

FE Enables interrupt when the upper conversion memory has been filled. (Memory Full).

HE Enables interrupt when the lower conversion memory has been filled. (Memory Half Full).

BS Flag showing unit is busy shifting data to DAC's

SSU Writing a '1' will set all DAC outputs to zero (this bit is cleared on completion)

1MB Enable 1Mb memory (32K values/channel) when logic 1 and 2Mb (64K values/channel) when logic 0.

MH Set to '1' when the memory is in habited from the IP Strobe line and ET set.

CONT Sets continues function generation

CC Conversions complete. Status bit set when the number of programmed updates has been completed. Generates IRQ0* if set and EE is set to a logic 1.

F Full status. Set when DAC16 has been updated from the top of memory. Generates IRQ0* if set and FE is set to a logic 1.

HF Half full status. Set when DAC16 has been updated from the top of the lower memory buffer. Generates IRQ0* if set and HE is set to a logic 1.

5.2 Memory Pointer

Read/write Address: 2hex
The current conversion address is given by the conversion base address offset by the DAC number and the Half Full status. The buffer pointer base address is the number of updates output.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

5.3 Number of updates

Read/write Address: 4hex
The number of updates register allows the number of updates per trigger to be programmed. If the memory buffer size is exceeded the update values will wrap around from the upper memory to the base of the lower memory.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

Note: If '0' is entered in to the Number of Updates register then the whole of the memory will be used to update the DACs.

5.4 Update Clock Rate

Read/write Address: 6hex
The Update Clock Rate register is a four bit register (D00 t0 D03) which enables codes 0 – 13 to enable update rate frequencies of 1 Hz to 20kHz in multiples of 1,2,5 or 10. (E.g. 0=1Hz, 1=2Hz, 2=5Hz, 3=10Hz and so on). Each rising edge of the Update Clock will initiate 16 DAC updates from memory EX=1 or from DAC registers if EX=0.
For memory updates the ARM bit must be set and the unit triggered.
For register updates the ARM bit must be set after the data has been loaded to the DAC data register.

5.5 Interrupt Vector

Read/write Address: 8hex
The vector register is a 16 bit register which stores the interrupt vector value.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

5.6 DAC Registers

Read/write Address: 10hex – 2Ehex
The 16 DACs can be updated from these registers on the next rising edge of the Update Clock when EX=0 and ARM are set the CSR. After each update the ARM bit is cleared and the unit must be reARMed each new register update. The Update Clock should be set to its highest rate for the best response rate.
Data format for the ***+/-10*** version is straight binary with 200h representing –10.v, 8000h = 0V and FE00h = +10V.
Data format for the ***0V-10V*** version is straight binary with 0000h representing 0V and FE00h = +10V.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

6. ID PROM

The ID data is stored in a serial EEPROM. The byte addresses are as below:-

Base+80	ASCII 'VI'	5649h	
Base+82	ASCII 'TA'	5441h	
Base+84	ASCII '4 '	3420h	
Base+86	Hytec ID high byte	0080h	
Base+88	Hytec ID low word	0300h	
Base+8A	Model number	8402h	
Base+8C	Revision	5501h	This shows PCB Iss 5 Xilinx V501
Base+8E	Reserved	0000h	
Base+90	Driver ID	0000h	
Base+92	Driver ID	0000h	
Base+94	Flags	0002h	
Base+96	No of bytes used	001Ah	
Base+98	Cal Type	xxxxh	0 = No Calibration factors, 1 = Calibration factors Stored.
Base+9A	Serial Number	xxxxdec	
Base+9C	Not used	0000h	
Base+9E	WLO	xxxxh	0xxxh =+/-10V unit 8xxxh=0 to 10V Unit (FW8402V50x)

For +/-10V version

Base+A0	CH1 Cal data nFS	xxxxh	Neg Full Scale (-10Volts) Calibration Factor
Base+A2	CH1 Cal data Zero	xxxxh	Zero (0 Volts) Calibration Factor
Base+A4	CH1 Cal data pFS	xxxxh	Pos Full Scale (+10Volts) Calibration Factor
	:		
	:		
Base+FA	CH16 Cal data nFS	xxxxh	Neg Full Scale (-10Volts) Calibration Factor
Base+FC	CH16 Cal data Zero	xxxxh	Zero (0 Volts) Calibration Factor
Base+FE	CH16 Cal data pFS	xxxxh	Pos Full Scale (+10Volts) Calibration Factor

For 0 to 10V version

Base+A0	CH1 Cal data Zero	xxxxh	Zero (0.002 Volts) Calibration Factor
Base+A2	CH1 Cal data pHS	xxxxh	Pos Half Scale (+5Volts) Calibration Factor
Base+A4	CH1 Cal data pFS	xxxxh	Pos Full Scale (+10Volts) Calibration Factor
	:		
	:		
Base+FA	CH16 Cal data Zero	xxxxh	Zero (0.002 Volts) Calibration Factor
Base+FC	CH16 Cal data pHS	xxxxh	Pos Half Scale (+5Volts) Calibration Factor
Base+FE	CH16 Cal data pFS	xxxxh	Pos Full Scale (+10Volts) Calibration Factor

7. SOFTWARE CALIBRATION

The type of calibration factors held in the ID PROM are specified by the Cal Type held at Base+98 in the ID PROM:-

0 = No Calibration factors held in ID PROM
1 = Calibration factors Stored in ID PROM

The Calibration Factors are held in the ID PROM as shown above in SECTION 6 starting at Base+A0. These values and are derived from reading the ADC values at specified voltages.

7.1 For +/-10V version

For the nFS value -10Volts is applied and the hex values from the DAC is stored and this is repeated for zero at 0volts, and pFS at +10volts.
These values can then be used in the following equations to correct the offset and gain errors of the individual cannels of the DAC8402 IP card.

$$\text{rawval} > \text{zero}$$

$$\text{CalVal} = \frac{(\text{pFS} - \text{zero}) \times (\text{rawval} - 0\text{x}8000)}{0\text{x}7\text{E}00} + \text{zero}$$

$$rawval < zero$$

$$CalVal = \frac{(zero - nFS) \times (rawval - 0x8000)}{0x7E00} + zero$$

7.2 For 0 to 10V version

For the pFS value +10Volts is applied and the hex values from the DAC is stored and this is repeated for zero at 0.002volts, and pHS at +5volts.
These values can then be used in the following equations to correct the offset and gain errors of the individual cannels of the DAC8402 IP card.

$$rawval > psHS$$

$$CalVal = \frac{(pFS) \times (rawval)}{0xFE00}$$

$$rawval \leq psHS$$

$$CalVal = \frac{(psHS) \times (rawval)}{0x7F00}$$

8. POWER UP AND POWER DOWN OF 8402 DAC

During power up the output voltages of the DAC will rise to approx 2 to 3 Volts for 10 -15 ms.
When the DAC is powered up it loads 8000hex into all DAC channels to give 0Volts output on all channels.
During power down voltage may rise to 3 to 4 volts for 10-15 ms.

A VME reset will not change the DAC output voltage.

9. EPICS Software Driver

EPICS software driver written for the 8402 16 channel DAC Industry Pack on 8002 Carrier Board with 8202 Transition Board.
For down loads go to:
www.hytec-electronics.co.uk/EPICS%20Drivers.html

10. Accuracy and Output current

Please note that the DAC has an accuracy of only 12 / 13 bits, and has +/-10 volt output at 10 mA max. The output current may be limited by the DC/DC converter when used in an isolated mode.

11. SELECTION OF THE +/-12 VOLT POWER SUPPLY

The DAC 8402 +/-12 volt power supply can be derived either internally from the carrier card or from an external source via a transition card. The source is selected using jumpers J2, J3 and the GND AGND link LNK1 where:

J2 External +12V connect 1 & 2, Internal +12V connect 2 & 3
J3 External -12V connect 1 & 2, Internal -12V connect 2 & 3

LNK1 (GND AGND)
IN for internal +/-12V
OUT for external +/-12V (supplied from transition card DC DC converter).

APPENDIX A

PCB JUMPERS

Issue 2 PCB
J1 Factory set IN
J2 External +12V connect 1 & 2, Internal +12V connect 2 & 3
J3 External -12V connect 1 & 2, Internal -12V connect 2 & 3

LNK1 Factory set IN links VME GND and AGND

APPENDIX B

I/O Connector – PL2 (50 way) on 8402 DAC PCB

Pin	Signal	Pin	Signal
1	Output 1	26	AGND
2	AGND	27	Output14
3	Output 2	28	AGND
4	AGND	29	Output15
5	Output 3	30	AGND
6	AGND	31	Output16
7	Output 4	32	AGND
8	AGND	33	N.C.
9	Output 5	34	N.C.
10	AGND	35	XTrigger
11	Output 6	36	/XTrigger
12	AGND	37	N.C.
13	Output 7	38	N.C.
14	AGND	39	XClk
15	Output 8	40	/XClk
16	AGND	41	+12VX
17	Output9	42	AGND
18	AGND	43	+12VX
19	Output10	44	AGND
20	AGND	45	-12VX
21	Output11	46	AGND
22	AGND	47	-12VX
23	Output12	48	AGND
24	AGND	49	N.C.
25	Output13	50	AGND

APPENDIX C

HYTEC TRANSITION CARD 8202 CONNECTIONS

I/O Connector – 50 way on transition panel

Pin	Signal	Pin	Signal
1	AGND	26	Output1
2	AGND	27	Output 2
3	AGND	28	Output 3
4	AGND	29	Output 4
5	AGND	30	Output 5
6	AGND	31	Output 6
7	AGND	32	Output 7
8	AGND	33	Output 8
9	AGND	34	Output 9
10	AGND	35	Output 10
11	AGND	36	Output 11
12	AGND	37	Output 12
13	AGND	38	Output 13
14	AGND	39	Output 14
15	AGND	40	Output 15
16	AGND	41	Output 16
17		42	
18	XTRIG N	43	XTRIG P
19		44	
20	XCLK N	45	XCLK P
21		46	
22		47	
23		48	
24	AGND	49	AGND
25	AGND	50	AGND

APPENDIX D

VME64X PIN ASSIGNMENT ON HYTEC 8002 IP CARRIER BOARD FOR DAC8402

ROW A	SIG	ROW B	SIG	ROW C	SIG	ROW D	SIG	ROW E	SIG	ROW F	SIG
P0.A01	D Chan 1+	P0.B01	D Chan 1-	P0.C01	D Chan 2+	P0.DO1	D Chan 2 -	P0.E01	D Chan 3+	P0.F01	GND
P0.A02	D Chan 3 -	P0.B02	D Chan 4+	P0.C02	D Chan 4 -	P0.D02	D Chan 5+	P0.E02	D Chan 5 -	P0.F02	GND
P0.A03	D Chan 6+	P0.B03	D Chan 6 -	P0.C03	D Chan 7+	P0.D03	D Chan 7 -	P0.E03	D Chan 8+	P0.F03	GND
P0.A04	D Chan 8 -	P0.B04	N/C	P0.C04	N/C	P0.D04	N/C	P0.E04	N/C	P0.F04	GND
P0.A05	N/C	P0.B05	N/C	P0.C05	N/C	P0.D05	N/C	P0.E05	N/C	P0.F05	GND
P0.A06	N/C	P0.B06	N/C	P0.C06	N/C	P0.D06	N/C	P0.E06	N/C	P0.F06	GND
P0.A07	N/C	P0.B07	N/C	P0.C07	N/C	P0.D07	N/C	P0.E07	D XTrigger	P0.F07	GND
P0.A08	D/XTrigger	P0.B08	N/C	P0.C08	N/C	P0.D08	D XCLK	P0.E08	D /XCLK	P0.F08	GND
P0.A09	D +12V	P0.B09	D AGND	P0.C09	D +12V	P0.D09	D AGND	P0.E09	D -12V	P0.F09	GND
P0.A10	D AGND	P0.B10	D -12V	P0.C10	D AGND	P0.D10	N/C	P0.E10	D AGND	P0.F10	GND
P0.A11	C Chan 1+	P0 B11	C Chan 1 -	P0.C11	C Chan 2+	P0.D11	C Chan 2 -	P0 E11	C Chan 3+	P0.F11	GND
P0.A12	C Chan 3 -	P0.B12	C Chan 4+	P0.C12	C Chan 4 -	P0.D12	C Chan 5+	P0.E12	C Chan 5 -	P0.F12	GND
P0.A13	C Chan 6+	P0.B13	C Chan 6-	P0.C13	C Chan 7+	P0.D13	C Chan 7 -	P0.E13	C Chan 8+	P0.F13	GND
P0.A14	C Chan 8+	P0.B14	N/C	P0.C14	N/C	P0.D14	N/C	P0.E14	N/C	P0.F14	GND
P0.A15	N/C	P0.B15	N/C	P0.C15	N/C	P0.D15	N/C	P0.E15	N/C	P0.F15	GND
P0.A16	N/C	P0.B16	N/C	P0.C16	N/C	P0.D16	N/C	P0.E16	N/C	P0.F16	GND
P0.A17	N/C	P0.B17	N/C	P0.C17	N/C	P0.D17	N/C	P0.E17	C XTrigger	P0.F17	GND
P0.A18	C/XTrigger	P0.B18	N/C	P0.C18	N/C	P0.D18	C XCLK	P0.E18	C /XCLK	P0.F18	GND
P0.A19	C +12V	P0.B19	C AGND	P0.C19	C +12V	P0.D19	C AGND	P0.E19	C -12V	P0.F19	GND

P0 pin assignment

P1 ROW A	SIGNAL	P1 ROW B	SIGNAL	P1 ROW C	SIGNAL	P1 ROW D	SIGNAL	P1 ROW Z	SIGNAL
P1.A01	D00	P1.B01	N/C	P1.C01	D08	P1.D01	N/C	P1.Z01	N/C
P1.A02	D01	P1.B02	N/C	P1.C02	D09	P1.D02	N/C	P1.Z02	GND
P1.A03	D02	P1.B03	N/C	P1.C03	D10	P1.D03	N/C	P1.Z03	N/C
P1.A04	D03	P1.B04	BG0IN*	P1.C04	D11	P1.D04	N/C	P1.Z04	GND
P1.A05	D04	P1.B05	BG0OUT*	P1.C05	D12	P1.D05	N/C	P1.Z05	N/C
P1.A06	D05	P1.B06	BG1IN*	P1.C06	D13	P1.D06	N/C	P1.Z06	GND
P1.A07	D06	P1.B07	BG1OUT*	P1.C07	D14	P1.D07	N/C	P1.Z07	N/C
P1.A08	D07	P1.B08	BG2IN*	P1.C08	D15	P1.D08	N/C	P1.Z08	GND
P1.A09	GND	P1.B09	BG2OUT*	P1.C09	GND	P1.D09	N/C	P1.Z09	N/C
P1.A10	N/C	P1.B10	BG3IN*	P1.C10	N/C	P1.D10	N/C	P1.Z10	GND
P1.A11	GND	P1.B11	BG3OUT*	P1.C11	BERR*	P1.D11	N/C	P1.Z11	N/C
P1.A12	DS1*	P1.B12	N/C	P1.C12	RESET	P1.D12	+3.3V	P1.Z12	GND
P1.A13	DS0*	P1.B13	N/C	P1.C13	LWORD*	P1.D13	N/C	P1.Z13	N/C
P1.A14	WRITE	P1.B14	N/C	P1.C14	AM5	P1.D14	+3.3V	P1.Z14	GND
P1.A15	GND	P1.B15	N/C	P1.C15	A23	P1.D15	N/C	P1.Z15	N/C
P1.A16	DTACK*	P1.B16	AM0	P1.C16	A22	P1.D16	+3.3V	P1.Z16	GND
P1.A17	GND	P1.B17	AM1	P1.C17	A21	P1.D17	N/C	P1.Z17	N/C
P1.A18	AS	P1.B18	AM2	P1.C18	A20	P1.D18	+3.3V	P1.Z18	GND
P1.A19	GND	P1.B19	AM3	P1.C19	A19	P1.D19	N/C	P1.Z19	N/C
P1.A20	IACK	P1.B20	GND	P1.C20	A18	P1.D20	+3.3V	P1.Z20	GND
P1.A21	IACKIN*	P1.B21	N/C	P1.C21	A17	P1.D21	N/C	P1.Z21	N/C
P1.A22	IACKOUT	P1.B22	N/C	P1.C22	A16	P1.D22	+3.3V	P1.Z22	GND
P1.A23	AM4	P1.B23	GND	P1.C23	A15	P1.D23	N/C	P1.Z23	N/C
P1.A24	A07	P1.B24	IRQ7*	P1.C24	A14	P1.D24	+3.3V	P1.Z24	GND
P1.A25	A06	P1.B25	IRQ6*	P1.C25	A13	P1.D25	N/C	P1.Z25	N/C
P1.A26	A05	P1.B26	IRQ5*	P1.C26	A12	P1.D26	+3.3V	P1.Z26	GND
P1.A27	A04	P1.B27	IRQ4*	P1.C27	A11	P1.D27	N/C	P1.Z27	N/C
P1.A28	A03	P1.B28	IRQ3*	P1.C28	A10	P1.D28	+3.3V	P1.Z28	GND
P1.A29	A02	P1.B29	IRQ2*	P1.C29	A09	P1.D29	N/C	P1.Z29	N/C
P1.A30	A0l	P1.B30	IRQ1*	P1.C30	A08	P1.D30	+3.3V	P1.Z30	GND
P1.A31	-12V	P1.B31	N/C	P1.C31	+12V	P1.D31	N/C	P1.Z31	N/C
P1.A32	+5V	P1.B32	+5V	P1.C32	+5V	P1.D32	+5V	P1.Z32	GND

P1 Pin Assignment

ROWA	SIG	ROWB	SIG	ROWC	SIG	ROWD	SIG	ROWZ	SIG
P2.A01	B +12V	P2.B01	+5V	P2.C01	B AGND	P2.D01	C -12V	P2.Z01	C AGND
P2.A02	B +12V	P2.B02	GND	P2.C02	B AGND	P2.D02	C AGND	P2.Z02	GND
P2.A03	B -12V	P2.B03	N/C	P2.C03	B AGND	P2.D03	C AGND	P2.Z03	N/C
P2.A04	B -12V	P2.B04	A24	P2.C04	B AGND	P2.D04	B Chan 1 +	P2.Z04	GND
P2.A05	N/C	P2.B05	A25	P2.C05	B AGND	P2.D05	B Chan 2 +	P2.Z05	B Chan 1 -
P2.A06	A Chan 1 +	P2.B06	A26	P2.C06	A Chan 1 -	P2.D06	B Chan 2 -	P2.Z06	GND
P2.A07	A Chan 2 +	P2.B07	A27	P2.C07	A Chan 2 -	P2.D07	B Chan 3 -	P2.Z07	B Chan 3 +
P2.A08	A Chan 3 +	P2.B08	A28	P2.C08	A Chan 3 -	P2.D08	B Chan 4 +	P2.Z08	GND
P2.A09	A Chan 4 +	P2.B09	A29	P2.C09	A Chan 4 -	P2.D09	B Chan 5 +	P2.Z09	B Chan 4 -
P2.A10	A Chan 5 +	P2.B10	A30	P2.C10	A Chan 5 -	P2.D10	B Chan 5 -	P2.Z10	GND
P2.A11	A Chan 6 +	P2.B11	A31	P2.C11	A Chan 6 -	P2.D11	B Chan 6 -	P2.Z11	B Chan 6 +
P2.A12	A Chan 7 +	P2.B12	GND	P2.C12	A Chan 7 -	P2.D12	B Chan 7 +	P2.Z12	GND
P2.A13	A Chan 8 +	P2.B13	+5V	P2.C13	A Chan 8 -	P2.D13	B Chan 8 +	P2.Z13	B Chan 7 -
P2.A14	N/C	P2.B14	N/C	P2.C14	N/C	P2.D14	B Chan 8 -	P2.Z14	GND
P2.A15	N/C	P2.B15	N/C	P2.C15	N/C	P2.D15	N/C	P2.Z15	N/C
P2.A16	N/C	P2.B16	N/C	P2.C16	N/C	P2.D16	N/C	P2.Z16	GND
P2.A17	N/C	P2.B17	N/C	P2.C17	N/C	P2.D17	N/C	P2.Z17	N/C
P2.A18	N/C	P2.B18	N/C	P2.C18	N/C	P2.D18	N/C	P2.Z18	GND
P2.A19	N/C	P2.B19	N/C	P2.C19	N/C	P2.D19	N/C	P2.Z19	N/C
P2.A20	N/C	P2.B20	N/C	P2.C20	N/C	P2.D20	N/C	P2.Z20	GND
P2.A21	N/C	P2.B21	N/C	P2.C21	N/C	P2.D21	N/C	P2.Z21	N/C
P2.A22	N/C	P2.B22	GND	P2.C22	N/C	P2.D22	N/C	P2.Z22	GND
P2.A23	A X Trigger	P2.B23	N/C	P2.C23	A /XTrigger	P2.D23	N/C	P2.Z23	N/C
P2.A24	N/C	P2.B24	N/C	P2.C24	N/C	P2.D24	N/C	P2.Z24	GND
P2.A25	A XCLK	P2.B25	N/C	P2.C25	A /XCLK	P2.D25	N/C	P2.Z25	N/C
P2.A26	A +12V	P2.B26	N/C	P2.C26	A AGND	P2.D26	N/C	P2.Z26	GND
P2.A27	A +12V	P2.B27	N/C	P2.C27	A AGND	P2.D27	B /XTrigger	P2.Z27	B X Trigger
P2.A28	A -12V	P2.B28	N/C	P2.C28	A AGND	P2.D28	N/C	P2.Z28	GND
P2.A29	A -12V	P2.B29	N/C	P2.C29	A AGND	P2.D29	B XCLK	P2.Z29	N/C
P2.A30	N/C	P2.B30	N/C	P2.C30	A AGND	P2.D30	B /XCLK	P2.Z30	GND
P2.A31	Out+3.3V	P2.B31	GND	P2.C31	Out+3.3V	P2.D31	GND	P2.Z31	Out +3.3V
P2.A32	Out+5V	P2.B32	+5V	P2.C32	Out+5V	P2.D32	+5V	P2.Z32	GND

P2 pin assignment

Denotes pins with thickened tracks which can be used for power inputs