



HYTEC ELECTRONICS Ltd

HEAD OFFICE: 5 CRADOCK ROAD, READING, BERKS. RG2 0JT, UK

Telephone: +44 (0) 118 9757770 Fax: +44 (0)118 9757566

E-mail: sales@hytec-electronics.co.uk

ADC8403 TWO 24 bit MULTIPLEXED ADCs INDUSTRY PACK

USERS MANUAL

For issue 6 PCB

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Author: MRN

CONTENTS

1. INTRODUCTION	3
2. PRODUCT SPECIFICATIONS	3
2.1 ADC.....	3
2.2 IDAC.....	4
2.3 VREF OUT	4
3. OPERATING MODES	4
3.1 SCANNING	4
3.2 EXCITATION	4
3.3 SAMPLING CLOCK.....	4
4. MEMORY MAP.....	5
4.1 CONVERSION MEMORY.....	5
5. APPLICATION REGISTERS	6
5.1 CONTROL & STATUS REGISTER (CSR)	6
5.2 CONTROL	6
5.3 CONVERSION POINTER BASE ADDRESS.....	7
5.4 NUMBER OF CONVERSIONS	7
5.5 CLOCK RATE/NUMBER OF CHANNELS.....	7
5.6 VECTOR.....	7
5.7 ADC1 AND ADC2 CONTROL	8
5.8 ADC1 AND ADC2 DATA.....	9
5.9 ON BOARD ADC CONFIGURATION REGISTERS.....	9
5.10 ACR ANALOGUE CONTROL REGISTER	10
5.11 SET IDAC CODE REGISTER.....	10
5.12 PGA_MUX REGISTERS	11
5.13 ADC DATA REGISTERS	12
6. ADC OPERATION	13
6.1 MEMORY UPDATE INHIBIT AND INTERRUPT.....	13
6.2 SET NUMBER OF CONVERSIONS.....	13
6.3 TRIGGERING.....	14
6.3.1 <i>Software Trigger</i>	14
6.3.2 <i>Hardware Trigger</i>	14
6.4 MEMORY UPDATE.....	14
7. ID PROM.....	14
APPENDIX A.....	16
APPENDIX B.....	17
APPENDIX C.....	18
APPENDIX D.....	19

1. INTRODUCTION

The Hytec IP-MADC-8403 is a single-width Industry Pack that provides up to 16 channels single ended or 8 channels differentially connected of simultaneously sampled analogue to digital conversion with the following characteristics:-

- 1 Two 24 bit ADCs
- 2 Each ADC multiplexer has 4 differential or 8 pseudo-differential inputs
- 3 On-chip ADC temperature sensors
- 4 Open-circuit and short-circuit input detection
- 5 Programmable current sources for excitation
- 6 Programmable gain amplifiers provide gains from 1 to 128
- 7 Programmable offset DACs allow input to amplifier to be offset to $\pm\frac{1}{2}$ FSR
- 8 Programmable self-calibration.
- 9 Fast settling and sync notch filters for interference rejection
- 10 Front-end isolated to 100V when used with DC-DC Converters
- 11 Choice of straight-through or filtered transition board with excitation options.

2. PRODUCT SPECIFICATIONS

Size: Single width Industry Pack 1.8ins x 3.9 ins
 Operating temp: 0 to 45 deg C ambient
 Power: +5V @ 300mA typical
 +12V @ 100mA, -12V @ 10mA typical
 Isolation: 100V (external power) ISOGND-VMEGND

2.1 ADC

Number of channels: 8 differential /16 pseudo-differential inputs plus Common
 Input voltage range: $\pm 2.5V$ with respect to Common or another input in the range 0V to +5V
 Resolution: Up to 19 bits dependent on ADC setup.
 No missing codes: 24 bits
 Conversion time per channel: Depending on clock, decimation values (set by ADC sample rate) and number of channels sampled e.g. 8 channels at an ADC sample rate of 200Hz = 100ms/chan
 Int. Non-linearity: $\pm 0.0015\%$ of full scale max.
 Offset : 7.5ppm of full scale range typical
 Offset drift: 0.02 ppm per deg C typical
 Gain error: $\pm 0.0025\%$ of full scale range (with standard calibration factors)
 Gain error: $\pm 0.05\%$ of full scale range (with out calibration factors)
 Gain error drift: 0.002 ppm per deg C typical
 Bandwidth: 10Hz to -3dB
 Throughput: 100 conversions per sec max with ext clock
 Noise: 10uV r.m.s.
 Distortion: -105dB for 1kHz input
 CMRR: -100dB (Better than)
 CMV: +5V, -0.2V with respect to ISOGND
 Data format: Binary
 Memory: 512K x 32 bits (32K samples per channel).

2.2 IDAC

Number of channels	2
Full-scale current course	0.500mA (range 1), 1.000mA (range 2), 2.000mA (range 3)
Full-scale current fine	0.140mA (range 1), 0.283mA (range 2), 0.567mA (range 3)
Short circuit duration	Indefinite
Resolution	8 bits
Monotonicity	8 bits
INL	+/-0.4LSB typical
DNL	+0.4/-0.1 LSB typical
Compliance voltage	+4V
Absolute Error	5%
Offset Drift	+/- 2 ppm/deg C typical
Gain Drift	+/-125ppm/deg C typical

2.3 Vref Out

Number of outputs	2
Voltage	+2.5V
Error	+/-0.04% max
Drift	1ppm/degC max.
Current available	10mA min.

3. Operating Modes

3.1 Scanning

There are three operating modes:-

1. DC sampling – when the 8403 is armed the inputs are scanned and logged to memory and channel registers hold the last ADC reading. This will cause an interrupt when the memory is full and will wrap around until halted by the user.
2. Triggered sampling – as above but where the inputs are scanned for a programmed number of scans as entered in to the NCO register.
3. User controlled – Here the user controls the ADC.

3.2 Excitation

Three excitation signal types are available:-

1. +5V regulated output derived from the +12V (as selected from external or VME supplies)
2. Two +2.5V buffered Vref outputs
3. Two 8 bit programmable IDAC outputs.

An isolated digital calibration enable (/CALEN) signal can be generated by command for switching calibration voltages.

3.3 Sampling Clock

On-chip, programmed or external sampling clocks may be selected according to filter and conversion rate requirements. The conversion rate and the filtering are setup using the on board registers of the ADC ICs.

4. Memory Map

The memory is used to record ADC data.

4.1 Conversion Memory

The conversion memory contains 512k samples of 32 bits each.

These are each divided into sixteen segments allocated to conversions from ADC A chan 1 to chan 8 and ADC B chan 1 to chan 8 .

When the memory is full the Full Flag status is set.

Memory
ADC16 conversions
ADC15 conversions
:
:
ADC4 conversions
ADC3 conversions
ADC2 conversions
ADC1 conversion 32k high word
ADC1 conversion 32 k low word
:
ADC1 conversion 1 high word
ADC1 conversion 1 low word

5. Application Registers

There are 8 application specific (I/O) registers; the CSR, the number of samples per trigger (NCO), the memory conversion pointer, the clock rate/number of channels and the interrupt vector value. There are also 32 longword ADC buffer registers.

5.1 Control & Status Register (CSR)

5.2 Control

Write Address: 0hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Arm	EX	ST	XC	ET	EE	FE	NU	2M	ECal	EII	MII	NU	CC	F	Rdy

Status

Read Address: 0hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Arm	EX	ST	XC	ET	EE	FE	NU	1M	ECal	EII	MII	MIS	CC	F	Rdy

NU = Not Used

- Arm** Arm the ADCs. Allow conversions either continuous or triggered. It also clears the memory address counter when taken low.
- EX** Enable trigger. If not set continuously scans at the clock rate. If set allows external trigger or software trigger
- ST** Software trigger. Triggers a programmed number of scans. ST is cleared on completion.
- XC** Enable the external clock. If 0 the internal clock is used for the conversion rate. If set true the external clock is used for the conversion clock.
- ET** Enable memory inhibit. The STROBE line on the 8403 is the inhibit signal. On the 8002 the STROBE line can be driven from the INHIBIT input lemo on the front panel.
- EE** Enables interrupt at end of sampling sequence.
- FE** Enables interrupt when the upper conversion memory has been filled. (Memory Full).
- 1M** Enables 1Mb memory (32K samples/channel) when logic 1 and 2Mb (64K samples/channel) when logic 0.
- ECal** Enables external calibration on transition board (Inputs to ref. voltage)
This can be used to switch external voltages in applications such as Cernox sensor measurement.
- EII** This enables an interrupt to be generated whenever the memory inhibit bit (MIS) is set.
- MII** Signifies that an interrupt has been generated by memory inhibit being enabled.
- MIS** This bit indicates if the memory update is inhibited. 1 = memory update inhibited.
- CC** Conversions complete. Status bit set when the number of programmed scans has been completed. Generates IRQ0* if set and EE is set to a logic 1.
- F** Full status. Set when the upper conversion memory has been filled. Generates IRQ0* if set and FE is set to a logic 1.
- Rdy** Ready status. Cleared to zero when a control word is sent to an ADC. Set true on completion of the control execution.

5.3 Conversion Pointer Base Address

Read/write Address: 2hex

The current conversion address is given by the conversion base address offset by the ADC number. .

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

5.4 Number of conversions

Read/write Address: 4hex

The number of conversions register allows the number of samples per trigger to be programmed.

The maximum number of conversions is 7FFF hex which gives 32K of samples per channel before an interrupt is generated.

If a number of triggers occur and the memory buffer size of 32K conversions per channel is exceeded the conversions will wrap

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
NU	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

NU = Not Used

5.5 Clock Rate/Number of Channels

Read/write Address: 6hex

The clock rate register is a four bit register which provides codes 0 – 16 to enable ADC external oscillator frequencies of 1 Hz to 200Hz 0=1Hz, 1=2Hz, 2=5Hz, 3=10Hz, 4=20Hz, 7=50Hz 8=100 9=200. This is the update rate that data is logged in to memory.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
NU	N14	N13	N12	NU	NU	NU	NU	NU	NU	NU	C4	C3	C2	C1	C0

NU = Not Used

Bits D12 to D14 signify the number of channels per ADC to be read. 1 to 8 (if zero will read 1 channel).

0 = read one channel from each of the ADCs

1 = two channel from each of the ADCs

:

:

6 = 7 channel from each of the ADCs

7 = 8 channel from each of the ADCs

5.6 Vector

Read/write Address: 8hex

The vector register is a 16 bit register which stores the interrupt vector value.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
NU	NU	NU	NU	NU	NU	NU	NU	V7	V6	V5	V4	V3	V2	V1	V0

NU = Not Used

5.7 ADC1 and ADC2 Control

Read /write Address: A hex

Control commands for ADC1 and ADC2 this can be 8bit or 16 bit .

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ADC sel															

X = ADC select X = 0= ADC A X = 1= ADC B

Code	Description
x0r 1h	Write Register 8bit 'r' = register address 0 to 16
x1r1h	Write two 8 bit concurrent Register 'r' = register address
x0r2h	Read Register 8bit 'r' = register address 0 to 16
x1r2h	Read two 8 bit concurrent Register. 'r' = register address
x013h	Read Data
x004h	Self Cal Offset and Gain
x014h	Self Cal Offset
x024h	Self Cal Gain
x034h	System Cal Offset
x044h	System Cal Gain
x0C4h	Sync /DRDY <i>No need to use this command</i>
x0D4h	Put in Sleep Mode <i>No need to use this command</i>
x0E4h	Reset to Power Up Values
x0a5h	Copy registers to RAM bank 'a' = RAM page number 0 to 16
x0a6h	Copy RAM Bank 'a' = RAM page number

5.8 ADC1 and ADC2 Data

Read/write Address: C hex

Data to be transferred to ADC1 and ADC2 Data register.

This is a shift register that shifts MSB first therefore 8bit data must be loaded to the top byte.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

5.9 On Board ADC configuration Registers

The ADC configuration is achieved by setting ADC registers on the ADC chip.

REG	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SETUP	ID	ID	ID	SPEED	REFEN	REFHI	BUFEN	BORD
MUX	PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0
ACR	BOCS	IDAC2R1	IDAC2R0	IDAC1R1	IDAC1R0	PGA2	PGA1	PGA0
IDAC1	IDAC1-7	IDAC1-6	IDAC1-5	IDAC1-4	IDAC1-3	IDAC1-2	IDAC1-1	IDAC1-0
IDAC2	IDAC2-7	IDAC2-6	IDAC2-5	IDAC2-4	IDAC2-3	IDAC2-2	IDAC2-1	IDAC2-0
ODAC	SIGN	OSET-6	OSET-5	OSET-4	OSET-3	OSET-2	OSET-1	OSET-0
DIO	DIO-7	DIO-6	DIO-5	DIO-4	DIO-3	DIO-2	DIO-1	DIO-0
DIR	DIR-7	DIR-6	DIR-5	DIR-4	DIR-3	DIR-2	DIR-1	DIR-0
DEC0	DEC07	DEC06	DEC05	DEC04	DEC03	DEC02	DEC01	DEC00
M/DEC1	/DRDY	U/B	SMODE1	SMODE0	RESERV	DEC10	DEC09	DEC08
OCR0	OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00
OCR1	OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08
OCR2	OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
FSR0	FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00
FSR1	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08
FSR2	FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

SETUP Speed/Ref/Buffer/Bit order

MUX Multiplexer Control Register – connects channel high and low inputs

ACR Analogue Control – gain ranges ADC & IDACs

IDAC1 Current DAC1 setting

IDAC2 Current DAC2 setting

ODAC Offset DAC setting

DIO Digital I/O (reserved)

DIR Direction control for digital I/O (reserved)

DEC0 With DEC1, defines decimation range 20-2047

M/DEC1 Mode (/DRDY, unipolar/bipolar, settling) and decimation msbs

OCR0 Offset Calibration Coefficient lsbs

OCR1 Offset Calibration Coefficient

OCR2 Offset Calibration Coefficient msbs

FSR0 Full Scale Register lsbs

FSR1 Full Scale Register

FSR2 Full Scale Register msbs

5.10 ACR Analogue Control Register

Read/write Address: E hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
BOCS	NU	NU	IDAC1R1	IDAC1R0	NU	NU	NU	BOCS	NU	NU	IDAC1R1	IDAC1R0	NU	NU	NU

NU = Not Used

This register will setup the ACR of both ADCs on the board for all channels when the unit ARM bit is set. This register can be written to when ARMED with out corruption of data.

The first byte of the register D00 to D07 set the ACR of the ADC A the second byte setup ADC B.

IDAC1R1: IDAC1R0: Full-Scale Range Select

- 00 = Off
- 01 = RANGE 1
- 10 = RANGE 2
- 11 = RANGE 3

BOCS: Burnout current source

- 0 = Disabled
- 1 = Enabled

5.11 Set IDAC Code Register

Read/write Address: 10 hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
IDB C1 B 7	IDB C1 B 6	IDB C1 B 5	IDB C1 B 4	IDB C1 B 3	IDB C1 B 2	IDB C1 B 1	IDB C1 B 0	IDA C1A 7	IDA C1A 6	IDA C1A 5	IDA C1A 4	IDA C1A 3	IDA C1A 2	IDA C1A 1	IDA C1A 0

This register will sets the IDAC output of both ADCs on the board for all channels when the unit ARM bit is set. This register can be written to when ARMED with out corruption of data.

The first byte of the register D00 to D07 set the IDAC1 of the ADC A the second byte setup IDAC1 of ADC B.

Calculation of output current

$$IDAC\ Current = \left(\frac{V_{REF}}{8 \times R_{DAC}} \right) \left(2^{RANGE-1} \right) (DAC\ Code)$$

For issue 6 PCB and up Rdac is selectable between 150k (course) and 562k (fine). To select 150k

To select Write to A & B ADC1216 DIO reg (8 bits) and DIR (8 bits)

For 150k Write 0xXXFE to DATA reg at address 0xC this hold data to be written to ADC1216

This sets DIR Direction Control reg bit 0 set to output all the reset to inputs and DIO Digital Output bit 0 set to 0 = 150kohm High current output 1 = 562kohm Low current output.

Command 0x0161 writes two 8 bit concurrent registers. The top bit selects ADC A ('0') or B ('1')

ADC1216 A 0x0161 to address 0xA Send data held in DATA reg to DIO and DIR registers

Wait for done bit to be set bit '0' CSR address 0x0

ADC1216 B 0x8161 to address 0xA Send data held in DATA reg to DIO and DIR registers

Wait for done bit to be set bit '0' CSR address 0x0

5.12 PGA_MUX Registers

Read/write Address: 20 to 3E hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
NU	NU	NU	NU	NU	PG A2	PG A1	PG A0	PSE L3	PSE L2	PSE L1	PSE L0	NS EL3	NS EL2	NS EL1	NS EL0

NU = Not Used

This register allows which inputs are to be used and the gain of each channel. This register should be set before the unit is ARMED. This register can be written to while the unit is ARMED but this may cause the ADC data to be invalidated for 1 reading. The register can be read at any time.

The registers are arranged as follows

Address

20 = A 1st chan

22 = B 1st chan

24 = A 2nd chan

26 = B 2nd chan

:

:

3C = A 16th chan

3E = B 16th chan

Bits 0 to 7 control the Multiplexer Control Register

Bits 7-4 PSEL3: PSEL2: PSEL1: PSEL0: Positive Channel Select

0000 = AIN0

0001 = AIN1

0010 = AIN2

0011 = AIN3

0100 = AIN4

0101 = AIN5

0110 = AIN6

0111 = AIN7

1xxx = AINCOM (except when all bits are 1's)

1111 = Temperature Sensor Diode Anode.

Bits 3-0 NSEL3: NSEL2: NSEL1: NSEL0: Negative Channel Select

0000 = AIN0

0001 = AIN1

0010 = AIN2

0011 = AIN3

0100 = AIN4

0101 = AIN5

0110 = AIN6

0111 = AIN7

1xxx = AINCOM (except when all bits are 1's)

1111 = Temperature Sensor Diode Cathode Analoge GND.

Bits 8 to 10 set the Programmable gain bits in the ACR registers of the ADCs when the unit is ARMed.

Gain Selection

000 = 1
 001 = 2
 010 = 4
 011 = 8
 100 = 16
 101 = 32
 110 = 64
 111 = 128

5.13 ADC Data Registers

Read Address: 40hex – 7Ehex

The 32 ADC buffer registers store the last sample conversions and may be read at any time as two words.

16 BIT DATA REG	ADDRESS
ADC A CHAN 1 LOW DATA	40hex
ADC A CHAN 1 HIGH DATA	42hex
ADC B CHAN 1 LOW DATA	44hex
ADC B CHAN 1 HIGH DATA	46hex
ADC A CHAN 2 LOW DATA	48hex
ADC A CHAN 2 HIGH DATA	4Ahex
ADC B CHAN 2 LOW DATA	4Chex
ADC B CHAN 2 HIGH DATA	4Ehex

To

ADC B CHAN 7 HIGH DATA	76hex
ADC A CHAN 8 LOW DATA	78hex
ADC A CHAN 8 HIGH DATA	7Ahex
ADC B CHAN 8 LOW DATA	7Chex
ADC B CHAN 8 HIGH DATA	7Ehex

UNIPOLAR

Data format UNIPOLAR is straight binary with 00000000h representing 0V and 00FFFFFFh, +2.5V.

$$V = (\text{Raw} * ((V_{\text{ref}} / (2 * \text{PGA})) / 2^{24}));$$

For single ended 0 to 2.5 volts.

ADC A Channel 1

Connect input between pin 26 and pin 9, 10, 11 or 12 on terminal block.

ADC B Channel 1

Connect input between pin 30 and pin 13, 14, 15 or 16 on terminal block.

Pins 9, 10, 11 and 12 are connected to the common line A_{INCOM} of ADC 'A' see page 15 of ADS1216 data sheet.

Pins 13, 14, 15 and 16 are connected to the common line A_{INCOM} of ADC 'B' see page 15 of ADS1216 data sheet.

BIPOLAR

Data Format BIPOLAR is +FS =0x007FFFFFF Zero = 0x00000000 -FS=0x00800000

For Bipolar operation 16 channels differential inputs +/-2.5v connect AINCOM to 2.5V ref by fitting J6 and J7. Connect input between AINx and AINCOM.

$$V = (((Raw + 0x800000) \& 0xFFFFFFFF) * (((Vref * 2) / (2 ** PGA)) / 2 ** 24)) - 2.5;$$

Most important turn OFF the BUF EN bit in the ADC configuration registers.

For Unipolar operation 16 channels single ended inputs 0 to 5v connect AINCOM to 2.5V ref by fitting J6 and J7. Connect input between AINx and AGND.

$$V = (((Raw + 0x800000) \& 0xFFFFFFFF) * (((Vref * 2) / (2 ** PGA)) / 2 ** 24));$$

ADC A COMMON and B COMMON must be left open.

Most important turn OFF the BUF EN bit in the ADC configuration registers.

Need to set for Bipolar mode in the ADC configuration register M/DEC1 (bit 6)

6. ADC OPERATION

The 8403 can be used in two ways

1. The register on the ADCs can be written to directly to control the ADCs
2. The unit can be set up then triggered to update the ADC data registers and memory. The ADC registers can be read while the unit is ARMED and running. The memory should not be read during data acquisition i.e. while ARMED and running.

The first ARMED data read after power ON will be in error.

6.1 Memory Update Inhibit and Interrupt

The updating of the conversion memory can be stopped from the external IP STROBE line (on the Hytec 8002 IP carrier card this signal is driver from the front panel INHIBIT lermo).

When the STROBE line is taken low and the external enable signal (ET) set in CSR the updating of the conversion memory is stopped. This is indicated by the MIS bit in the CSR going high.

On memory update inhibit an interrupt can be generated if the memory inhibit interrupt enable bit (EII) is set in the CSR. The Memory Inhibit Interrupt (MII) bit of the CSR flags an interrupt. This is cleared by writing to the MII bit in the CSR.

6.2 Set Number of Conversions

The number of conversions register (NCO) at address 2hex allows the number of samples per trigger to be programmed. The maximum number of conversions is FFFFhex which gives 64K of samples for each channel before the Conversion Complete (CC) flag is set in the CSR. An interrupt is generated if the Enable Interrupt on Last Sample (EE) bit is set in the CSR. To clear the interrupt write a '0' to the CC bit of the CSR.

If a number of triggers occur and the memory buffer size of 128K of conversions per channel is exceeded the conversions will wrap around from the upper memory to the base of the lower memory

6.3 Triggering

The triggering of the ADC8403 is only used when the number of conversions has been set in the Number of Conversions register and the Enable Trigger (EX) bit has been set in the CSR.

6.3.1 Software Trigger

The unit can be triggered by a software trigger by writing a '1' to the Software Trigger (ST) bit of the CSR.

6.3.2 Hardware Trigger

The external trigger is passed to the ADC8403 via designated pins see Appendices B, C and D.

6.4 Memory Update

All ADC channels are updated simultaneously and the memory pointer incremented. Therefore the memory pointer indicates what memory location has been reached by all the ADCs by adding the channel number to the pointer value with the channel number as the most significant bit.

E.g:- Channel 1 = xxxx Channel 2 = 1xxxx Channel 3 = 2xxxx etc.

7. ID PROM

The byte addresses are as below:-

Base+80	ASCII 'VI'	5649h	
Base+82	ASCII 'TA'	5441h	
Base+84	ASCII '4 '	3420h	
Base+86	Hytec ID high byte	0080h	
Base+88	Hytec ID low word	0300h	
Base+8A	Model number	8403h	
Base+8C	Revision	6601h	This shows the PDB at Issue 6 and Xilinx issue is V601 (which means Xilinx firmware at issue 1 for PCB issue 6.
Base+8E	Reserved	0000h	
Base+90	Driver ID	0000h	
Base+92	Driver ID	0000h	
Base+94	Flags	0002h	
Base+96	No of bytes used	001Ah	
Base+98	Cal Type	xxxxh	1 = Calibration factors Stored.
Base+9A	Serial Number	xxxxdec	
Base+9C	NU		
Base+9F	NU		

Base+A0 Cal Factor

.
.

.

.

Base+BE Cal Factor

APPENDIX A

PCB JUMPERS

Issue 4 PCB

J1 Factory set

J2 External +12V connect 1 & 2, Internal +12V connect 2 & 3

J3 External -12V connect 1 & 2, Internal -12V connect 2 & 3

J4 Jumper IN to connect IDAC1 of ADC A to output

J5 Jumper IN to connect IDAC1 of ADC B to output

J6 IN connects A IN COM to Vref

J7 IN connects B IN COM to Vref

LNK 1 This connects AGND to GND. This should be removed when using External +/-12V.

APPENDIX B
I/O Connector – 50 way on 8403 ADC Board

Pin	Signal	Pin	Signal
1	ADC A Input 1	26	ADC B COMMON
2	ADC A Input 2	27	V Ref out ADC B
3	ADC A Input 3	28	ADC B COMMON
4	ADC A Input 4	29	+5VA
5	ADC A Input 5	30	ADC B COMMON
6	ADC A Input 6	31	N.C.
7	ADC A Input 7	32	ADC B COMMON
8	ADC A Input 8	33	*CAL EX
9	ADC B Input 1	34	N.C.
10	ADC B Input 2	35	XTrigger
11	ADC B Input 3	36	/XTrigger
12	ADC B Input 4	37	IDAC0 A
13	ADC B Input 5	38	N.C.
14	ADC B Input 6	39	XClk
15	ADC B Input 7	40	/XClk
16	ADC B Input 8	41	+12VX
17	N.C.	42	AGND
18	ADC A COMMON	43	+12VX
19	V Ref out ADC A	44	AGND
20	ADC A COMMON	45	-12VX
21	+5VA	46	AGND
22	ADC A COMMON	47	-12VX
23	N.C.	48	AGND
24	ADC A COMMON	49	IDAC0 B
25	N.C.	50	AGND

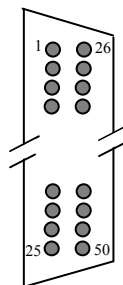
APPENDIX C

I/O Connector – 50 way on transition

TB 8210 TCTP Transition Board

Where this feeds ONE IP sites

Pin	Signal		Pin	Signal
	JP =1-2 Single Ended	JP=2-3 Differential		
1	ADC A COMMON	ADC A Input 2	26	ADC A Input 1
2	ADC A COMMON	ADC A Input 3	27	ADC A Input 2
3	ADC A COMMON	ADC A Input 4	28	ADC A Input 3
4	ADC A COMMON	ADC A Input 5	29	ADC A Input 4
5	ADC A COMMON	ADC A Input 6	30	ADC A Input 5
6	ADC A COMMON	ADC A Input 7	31	ADC A Input 6
7	ADC A COMMON	ADC A Input 8	32	ADC A Input 7
8	ADC A COMMON	ADC B Input 1	33	ADC A Input 8
9	ADC B COMMON	ADC B Input 2	34	ADC B Input 1
10	ADC B COMMON	ADC B Input 3	35	ADC B Input 2
11	ADC B COMMON	ADC B Input 4	36	ADC B Input 3
12	ADC B COMMON	ADC B Input 5	37	ADC B Input 4
13	ADC B COMMON	ADC B Input 6	38	ADC B Input 5
14	ADC B COMMON	ADC B Input 7	39	ADC B Input 6
15	ADC B COMMON	ADC B Input 8	40	ADC B Input 7
16	ADC B COMMON	NC	41	ADC B Input 8
17	N.C.		42	*CAL EN
18	XTRIG N		43	XTRIG P
19	IDAC0 B		44	IDAC0 A
20	XCLK N		45	XCLK P
21	AGND		46	+12VX
22	AGND		47	+12VX
23	AGND		48	-12VX
24	AGND		49	-12VX
25	AGND		50	AGND

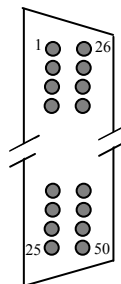


APPENDIX D
HYTEC TRANSITION CARD CONNECTIONS

I/O Connector – 50 way on transition

VTB8304 STRAIGHT-THROUGH TRANSITION CARD
Where this feeds ONE IP sites

Pin	Signal	Pin	Signal
1	ADC A Input 2	26	ADC A Input 1
2	ADC A Input 4	27	ADC A Input 3
3	ADC A Input 6	28	ADC A Input 5
4	ADC A Input 8	29	ADC A Input 7
5	ADC B Input 2	30	ADC B Input 1
6	ADC B Input 4	31	ADC B Input 3
7	ADC B Input 6	32	ADC B Input 5
8	ADC B Input 8	33	ADC B Input 7
9	ADC A COMMON	34	N.C.
10	ADC A COMMON	35	V Ref out ADC A
11	ADC A COMMON	36	+5VA
12	ADC A COMMON	37	N.C.
13	ADC B COMMON	38	N.C.
14	ADC B COMMON	39	V Ref out ADC B
15	ADC B COMMON	40	+5VA
16	ADC B COMMON	41	N.C.
17	N.C.	42	*CAL EN
18	XTRIG N	43	XTRIG P
19	N.C.	44	IDAC0 A
20	XCLK N	45	XCLK P
21	AGND	46	+12VX
22	AGND	47	+12VX
23	AGND	48	-12VX
24	AGND	49	-12VX
25	AGND	50	IDAC0 B



APPENDIX D
VME64X PIN ASSIGNMENT ON HYTEC 8002 IP CARRIER BOARD FOR ADC8403

ROW A	SIG	ROW B	SIG	ROW C	SIG	ROW D	SIG	ROW E	SIG	ROW F	SIG
P0.A01	D Chan 1+	P0.B01	D Chan 1-	P0.C01	D Chan 2+	P0.D01	D Chan 2 -	P0.E01	D Chan 3+	P0.F01	GND
P0.A02	D Chan 3 -	P0.B02	D Chan 4+	P0.C02	D Chan 4 -	P0.D02	D Chan 5+	P0.E02	D Chan 5 -	P0.F02	GND
P0.A03	D Chan 6+	P0.B03	D Chan 6 -	P0.C03	D Chan 7+	P0.D03	D Chan 7 -	P0.E03	D Chan 8+	P0.F03	GND
P0.A04	D Chan 8 -	P0.B04	N/C	P0.C04	N/C	P0.D04	N/C	P0.E04	N/C	P0.F04	GND
P0.A05	N/C	P0.B05	N/C	P0.C05	N/C	P0.D05	N/C	P0.E05	N/C	P0.F05	GND
P0.A06	N/C	P0.B06	N/C	P0.C06	N/C	P0.D06	N/C	P0.E06	N/C	P0.F06	GND
P0.A07	N/C	P0.B07	N/C	P0.C07	N/C	P0.D07	N/C	P0.E07	D XTrigger	P0.F07	GND
P0.A08	D/XTrigger	P0.B08	N/C	P0.C08	N/C	P0.D08	D XCLK	P0.E08	D /XCLK	P0.F08	GND
P0.A09	D +12V	P0.B09	D AGND	P0.C09	D +12V	P0.D09	D AGND	P0.E09	D -12V	P0.F09	GND
P0.A10	D AGND	P0.B10	D -12V	P0.C10	D AGND	P0.D10	N/C	P0.E10	D AGND	P0.F10	GND
P0.A11	C Chan 1+	P0.B11	C Chan 1 -	P0.C11	C Chan 2+	P0.D11	C Chan 2 -	P0.E11	C Chan 3+	P0.F11	GND
P0.A12	C Chan 3 -	P0.B12	C Chan 4+	P0.C12	C Chan 4 -	P0.D12	C Chan 5+	P0.E12	C Chan 5 -	P0.F12	GND
P0.A13	C Chan 6+	P0.B13	C Chan 6-	P0.C13	C Chan 7+	P0.D13	C Chan 7 -	P0.E13	C Chan 8+	P0.F13	GND
P0.A14	C Chan 8+	P0.B14	N/C	P0.C14	N/C	P0.D14	N/C	P0.E14	N/C	P0.F14	GND
P0.A15	N/C	P0.B15	N/C	P0.C15	N/C	P0.D15	N/C	P0.E15	N/C	P0.F15	GND
P0.A16	N/C	P0.B16	N/C	P0.C16	N/C	P0.D16	N/C	P0.E16	N/C	P0.F16	GND
P0.A17	N/C	P0.B17	N/C	P0.C17	N/C	P0.D17	N/C	P0.E17	C XTrigger	P0.F17	GND
P0.A18	C/XTrigger	P0.B18	N/C	P0.C18	N/C	P0.D18	C XCLK	P0.E18	C /XCLK	P0.F18	GND
P0.A19	C +12V	P0.B19	C AGND	P0.C19	C +12V	P0.D19	C AGND	P0.E19	C -12V	P0.F19	GND


P0 pin assignment

PI ROW A	SIGNAL	PI ROW B	SIGNAL	PI ROW C	SIGNAL	PI ROW D	SIGNAL	PI ROW Z	SIGNAL
P1.A01	D00	P1.B01	N/C	P1.C01	D08	P1.D01	N/C	P1.Z01	N/C
P1.A02	D01	P1.B02	N/C	P1.C02	D09	P1.D02	N/C	P1.Z02	GND
P1.A03	D02	P1.B03	N/C	P1.C03	D10	P1.D03	N/C	P1.Z03	N/C
P1.A04	D03	P1.B04	BG0IN*	P1.C04	D11	P1.D04	N/C	P1.Z04	GND
P1.A05	D04	P1.B05	BG0OUT*	P1.C05	D12	P1.D05	N/C	P1.Z05	N/C
P1.A06	D05	P1.B06	BG1IN*	P1.C06	D13	P1.D06	N/C	P1.Z06	GND
P1.A07	D06	P1.B07	BG1OUT*	P1.C07	D14	P1.D07	N/C	P1.Z07	N/C
P1.A08	D07	P1.B08	BG2IN*	P1.C08	D15	P1.D08	N/C	P1.Z08	GND
P1.A09	GND	P1.B09	BG2OUT*	P1.C09	GND	P1.D09	N/C	P1.Z09	N/C
P1.A10	N/C	P1.B10	BG3IN*	P1.C10	N/C	P1.D10	N/C	P1.Z10	GND
P1.A11	GND	P1.B11	BG3OUT*	P1.C11	BERR*	P1.D11	N/C	P1.Z11	N/C
P1.A12	DS1*	P1.B12	N/C	P1.C12	RESET	P1.D12	+3.3V	P1.Z12	GND
P1.A13	DS0*	P1.B13	N/C	P1.C13	LWORD*	P1.D13	N/C	P1.Z13	N/C
P1.A14	WRITE	P1.B14	N/C	P1.C14	AM5	P1.D14	+3.3V	P1.Z14	GND
P1.A15	GND	P1.B15	N/C	P1.C15	A23	P1.D15	N/C	P1.Z15	N/C
P1.A16	DTACK*	P1.B16	AM0	P1.C16	A22	P1.D16	+3.3V	P1.Z16	GND
P1.A17	GND	P1.B17	AM1	P1.C17	A21	P1.D17	N/C	P1.Z17	N/C
P1.A18	AS	P1.B18	AM2	P1.C18	A20	P1.D18	+3.3V	P1.Z18	GND
P1.A19	GND	P1.B19	AM3	P1.C19	A19	P1.D19	N/C	P1.Z19	N/C
P1.A20	IACK	P1.B20	GND	P1.C20	A18	P1.D20	+3.3V	P1.Z20	GND
P1.A21	IACKIN*	P1.B21	N/C	P1.C21	A17	P1.D21	N/C	P1.Z21	N/C
P1.A22	IACKOUT	P1.B22	N/C	P1.C22	A16	P1.D22	+3.3V	P1.Z22	GND
P1.A23	AM4	P1.B23	GND	P1.C23	A15	P1.D23	N/C	P1.Z23	N/C
P1.A24	A07	P1.B24	IRQ7*	P1.C24	A14	P1.D24	+3.3V	P1.Z24	GND
P1.A25	A06	P1.B25	IRQ6*	P1.C25	A13	P1.D25	N/C	P1.Z25	N/C
P1.A26	A05	P1.B26	IRQ5*	P1.C26	A12	P1.D26	+3.3V	P1.Z26	GND
P1.A27	A04	P1.B27	IRQ4*	P1.C27	A11	P1.D27	N/C	P1.Z27	N/C
P1.A28	A03	P1.B28	IRQ3*	P1.C28	A10	P1.D28	+3.3V	P1.Z28	GND
P1.A29	A02	P1.B29	IRQ2*	P1.C29	A09	P1.D29	N/C	P1.Z29	N/C
P1.A30	A01	P1.B30	IRQ1*	P1.C30	A08	P1.D30	+3.3V	P1.Z30	GND
P1.A31	-12V	P1.B31	N/C	P1.C31	+12V	P1.D31	N/C	P1.Z31	N/C
P1.A32	+5V	P1.B32	+5V	P1.C32	+5V	P1.D32	+5V	P1.Z32	GND

P1 Pin Assignment

ROWA	SIG	ROWB	SIG	ROWC	SIG	ROWD	SIG	ROWZ	SIG
P2.A01	B +12V	P2.B01	+5V	P2.C01	B AGND	P2.D01	C -12V	P2.Z01	C AGND
P2.A02	B +12V	P2.B02	GND	P2.C02	B AGND	P2.D02	C AGND	P2.Z02	GND
P2.A03	B -12V	P2.B03	N/C	P2.C03	B AGND	P2.D03	C AGND	P2.Z03	N/C
P2.A04	B -12V	P2.B04	A24	P2.C04	B AGND	P2.D04	B Chan 1 +	P2.Z04	GND
P2.A05	N/C	P2.B05	A25	P2.C05	B AGND	P2.D05	B Chan 2 +	P2.Z05	B Chan 1 -
P2.A06	A Chan 1 +	P2.B06	A26	P2.C06	A Chan 1 -	P2.D06	B Chan 2 -	P2.Z06	GND
P2.A07	A Chan 2 +	P2.B07	A27	P2.C07	A Chan 2 -	P2.D07	B Chan 3 -	P2.Z07	B Chan 3 +
P2.A08	A Chan 3 +	P2.B08	A28	P2.C08	A Chan 3 -	P2.D08	B Chan 4 +	P2.Z08	GND
P2.A09	A Chan 4 +	P2.B09	A29	P2.C09	A Chan 4 -	P2.D09	B Chan 5 +	P2.Z09	B Chan 4 -
P2.A10	A Chan 5 +	P2.B10	A30	P2.C10	A Chan 5 -	P2.D10	B Chan 5 -	P2.Z10	GND
P2.A11	A Chan 6 +	P2.B11	A31	P2.C11	A Chan 6 -	P2.D11	B Chan 6 +	P2.Z11	B Chan 6 +
P2.A12	A Chan 7 +	P2.B12	GND	P2.C12	A Chan 7 -	P2.D12	B Chan 7 +	P2.Z12	GND
P2.A13	A Chan 8 +	P2.B13	+5V	P2.C13	A Chan 8 -	P2.D13	B Chan 8 +	P2.Z13	B Chan 7 -
P2.A14	N/C	P2.B14	N/C	P2.C14	N/C	P2.D14	B Chan 8 -	P2.Z14	GND
P2.A15	N/C	P2.B15	N/C	P2.C15	N/C	P2.D15	N/C	P2.Z15	N/C
P2.A16	N/C	P2.B16	N/C	P2.C16	N/C	P2.D16	N/C	P2.Z16	GND
P2.A17	N/C	P2.B17	N/C	P2.C17	N/C	P2.D17	N/C	P2.Z17	N/C
P2.A18	N/C	P2.B18	N/C	P2.C18	N/C	P2.D18	N/C	P2.Z18	GND
P2.A19	N/C	P2.B19	N/C	P2.C19	N/C	P2.D19	N/C	P2.Z19	N/C
P2.A20	N/C	P2.B20	N/C	P2.C20	N/C	P2.D20	N/C	P2.Z20	GND
P2.A21	N/C	P2.B21	N/C	P2.C21	N/C	P2.D21	N/C	P2.Z21	N/C
P2.A22	N/C	P2.B22	GND	P2.C22	N/C	P2.D22	N/C	P2.Z22	GND
P2.A23	A X Trigger	P2.B23	N/C	P2.C23	A /XTrigger	P2.D23	N/C	P2.Z23	N/C
P2.A24	N/C	P2.B24	N/C	P2.C24	N/C	P2.D24	N/C	P2.Z24	GND
P2.A25	A XCLK	P2.B25	N/C	P2.C25	A /XCLK	P2.D25	N/C	P2.Z25	N/C
P2.A26	A +12V	P2.B26	N/C	P2.C26	A AGND	P2.D26	N/C	P2.Z26	GND
P2.A27	A +12V	P2.B27	N/C	P2.C27	A AGND	P2.D27	B /XTrigger	P2.Z27	B X Trigger
P2.A28	A -12V	P2.B28	N/C	P2.C28	A AGND	P2.D28	N/C	P2.Z28	GND
P2.A29	A -12V	P2.B29	N/C	P2.C29	A AGND	P2.D29	B XCLK	P2.Z29	N/C
P2.A30	N/C	P2.B30	N/C	P2.C30	A AGND	P2.D30	B /XCLK	P2.Z30	GND
P2.A31	+3.3V	P2.B31	GND	P2.C31	+3.3V	P2.D31	GND	P2.Z31	+3.3V
P2.A32	+5V	P2.B32	Out+5V	P2.C32	Out+5V	P2.D32	+5V	P2.Z32	GND

P2 pin assignment

 Denotes pins with thickened tracks which can be used for power inputs