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DAC8404
16-CHANNEL 16-BIT DAC
INDUSTRY PACK

User Manual

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CONTENTS

1. Features

The Hytec IP-DAC-8404 is a single-width Industry Pack that provides 16 channels of simultaneously updated digital to analogue conversion with the following characteristics:-

- 16 independently programmed channels
- 5 programmable ranges per channel 0-5V, 0-10V +/-5V, +/-10V and +/-2.5V
- 16 bits resolution
- 64K samples per channel memory.
- Registered or memory fetch updates.
- Two independent digitally controlled full-scale trims for each group of eight channels.
- Low offset error - +/-5mV typical (With software Cal applied +/-0.5mV)
- Low gain error - +/-5LSBs typical (With software Cal applied +/-2.5LSBs typ.+/-4.5LSBs max)
- Low error drift - 2ppm per deg C
- +/- 10mA current drive capability with continuous short-circuit protection
- Straight binary code
- 10KHz update rate
- Power-On Reset to 0V
- 100V system to plant isolation when externally powered
- Board serial number, PCB issue and firmware version held on ROM.
- External Triggering
- Continuous function generation.
- Internal/External update clock rates
- Internal update clock rates programmable (10KHz,5KHz,2KHz,1KHz,500Hz,200Hz,100Hz,50Hz,20Hz,10Hz,5Hz,2Hz and 1Hz)
- Pin-out compatible with DAC8402 (in command default mode).

2. Product Specifications

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of channels:	16
DAC resolution:	16 bits
Data format:	16 bits binary
Range:	Programmable 0V to 5V, 0V to 10V, +/-5V, +/-10V, and +/-2.5V FSR (Full Scale Reading)
Output current:	+/-10mA @ FS
Capacitive load:	Stable up to 20,000pF
Short circuit duration:	Continuous
OverV withstand:	No internal protection from external voltages provided
Update rate:	10KHz max
Power:	+5V @ 300mA typical +/-12V @ 120mA typical when switched to internal (external load dependent)
Isolation:	100V via opto-isolators (if externally powered)
Integral non-linearity:	+/-1LSB max
Diff non-linearity:	+/-1LSB max
Offset error:	+/-200uV max
Gain drift:	3ppm per deg C
Gain error:	+/-5LSBs typ. +/-16LSBs max.
Output slew rate:	+/-13V/us min.
Settling time:	20us max.to 0.005% of final value for 1000pF load capacitance

3. Operating Modes

There are two operating modes:-

1. *Registered* – the DAC outputs are controlled by the contents of the DAC registers.
2. *Memory* – the outputs are updated for the programmed number of samples at the programmed clock rate.

All the outputs are updated serially but change together (there will be slight changes due to differences in the slew rate of the amplifiers (about +/-1uS) at the end of an internal update cycle.

The outputs may be updated at a rate of up to 10KHz. The two methods to update the 8404 DACs are detailed below.

3.1 USING REGISTERS TO UP DATE DACs

There are 16 individual DACs on the IP Card with 16 Data & Command DAC registers to access each one. This allows the user to set if required each DAC to different voltage ranges. The DACs are serially loaded with a 32 bit data stream comprising of the first 16 bits with the command word, to set the required voltage range, and the last 16 bits correspond to the data to set the output of the DAC to. Therefore, both the data and command registers must both be set the DACs to operate correctly.

The DACs are arranged in two groups, DACs 1 to 8 are daisy chained together to form bank A and DACs 9 to 16 daisy chained to form bank B.

Once the registers have been loaded, the module can then be ARMed and the data from the registers will be serially loaded from one DAC to the next until all the data has been passed to all of the DACs. At this point the DAC outputs are automatically updated giving 16 simultaneous outputs. While the unit is ARMed the DACs are constantly refreshed with the contents of the registers which can be changed during this time. There is a delay which is fixed of approximately 32us after ARM is set, before all the outputs change together.

3.2 USING MEMORY TO UP DATE DACs

In this mode the data to be sent to the DACs is loaded from memory instead of the DAC Data register, however the command for each DAC is still required, but only has to be set once at the start. Once the DAC Command has been set this remains unchanged, unless the voltage range is changed, then the new command must be written again.

The onboard memory is first loaded with the required data and the number of memory locations used is entered in to the Number of Updates (NCO) register. With the DAC Command Register already written and set, the Control and Status Register (CSR) is then set to enable memory updates and ARM to unit with a software command. A trigger can then be issued either by a software command or by an external trigger to start down loading the data held in memory to the DACs via the registers as detail above. In this mode the registers are updated with new data from the memory at the update clock rate which is derived either internally or externally. The memory address is automatically incremented.

When the programmed number of output has occurred the unit will stop and generate an interrupt if enabled or if set in continues mode the address counter will be zeroed and the output repeated (no interrupt generated in continues mode) until the ARM bit is cleared or the continues bit CC in the CSR is cleared.

4. Memory Map

There are two main buffer memories of 512k updates each (lower and upper buffers)
These are each divided into sixteen segments allocated to updates for DAC1 to DAC16.
When DAC16 has been updated from the top of the lower buffer, the Half Full Flag status is set and when it has been updated from the top of the upper memory buffer the Full Flag status is set.

Lower Conversion Memory	Upper Conversion Memory
DAC16 conversions	DAC16 conversions
DAC15 conversions	DAC15 conversions
DAC14 conversions	DAC14 conversions
DAC13 conversions	DAC13 conversions
DAC12 conversions	DAC12 conversions
DAC11 conversions	DAC11 conversions
DAC10 conversions	DAC10 conversions
DAC9 conversions	DAC9 conversions
DAC8 conversions	DAC8 conversions
DAC7 conversions	DAC7 conversions
DAC6 conversions	DAC6 conversions
DAC5 conversions	DAC5 conversions
DAC4 conversions	DAC4 conversions
DAC3 conversions	DAC3 conversions
DAC2 conversions	DAC2 conversions
DAC1 conversion 32k	DAC1 conversion 64k
DAC1 conversion 32k-1	DAC1 conversion 64k-1
DAC1 conversion 2	DAC1 conversion 32k+2
DAC1 conversion 1	DAC1 conversion 32k+1

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5. Application Registers

There are eight application specific (I/O) registers; the CSR, the number of samples per trigger, the Conversion Pointer, Clock Rate, Interrupt Vector, Full Scale Trim & ID Page No, DAC Data Registers and DAC Command Registers.

5.1 Control & Status Register (CSR)

Read/Write Address: 0 hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ARM	EX	ST	XC	ET	EE	FE	HE	0	0	1MB	MH	CONT	CC	F	HF

ARM Writing a '1' to ARM bit causes the values loaded in to the DAC registers or the memory to be loaded in to the DACs.
When all the DACs have been updated from the registers (the EX bit set to '0') the ARM bit is cleared.
If the DACs are being updated from the memory (the EX bit set to '1') the ARM bit is not cleared.
In this mode if a number of triggers occur which cause the end of the memory to be reached, a subsequent trigger will cause the memory pointer to wrap around to the start of memory.

EX Enable trigger and memory update.
EX=0 If not set the outputs will be enabled from the registers transparently.
EX=1 If set allows external trigger or software trigger to initiate programmed updates from memory. In this mode the *Number Of Updates Register* needs to be set between 0 to 64K updates.

ST Software trigger. Triggers a programmed number of updates from the memory as set by the Number of Updates register.

XC Enable the external clock. 0 = internal clock used for the sample rate. 1 = external clock used for the sample rate.

ET When set to '1' enables signal the Inhibit Lemo of the 8002 via the IP Strobe line. The Inhibit signal when set stops the updating DAC from memory.

EE Enables interrupt at end of programmed number of DAC updates from memory.

FE Enables interrupt when the upper conversion memory has been filled. (Memory Full).

HE Enables interrupt when the lower conversion memory has been filled. (Memory Half Full).

1MB Enable 1Mb memory, (32K values/channel), when logic 1 and 2Mb (64K values/channel) when logic 0.

MH Set to '1' when the memory is inhibited from the IP Strobe line and ET set.

CONT Sets continues function generation

CC Conversions complete. Status bit set when the number of programmed updates has been completed. Generates IRQ0* if set and EE is set to a logic 1.

F Full status. Set when DAC16 has been updated from the top of memory. Generates IRQ0* if set and FE is set to a logic 1.

HF Half full status. Set when DAC16 has been updated from the top of the lower memory buffer. Generates IRQ0* if set and HE is set to a logic 1.

5.2 Memory Pointer

Read/write Address: 2 hex
The current conversion address is given by the conversion base address offset by the DAC number and for mode 0 the Half Full status. The buffer pointer base address is the number of updates output.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

5.3 Number of Updates 1

Read/write Address: 4 hex
The number of updates register allows the number of updates per trigger to be programmed. It is basically which sample to start a memory waveform output from. If the memory buffer size is exceeded the update values will wrap around from the upper memory to the base of the lower memory. Number of Updates 1 and Number of Updates 2 should be set to the same value.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

Note 1: If DACs are being driven by the DAC Data Registers (10 – 1E Hex) rather than from the Waveform Memory then both Number of Updates registers must be loaded with FFFF Hex.

Note 2: If '0' is entered in to the Number of Updates register then the whole of the memory will be used to update the DACs.

5.4 Clock Rate

Read/write Address: 6 hex
The clock rate register allows you to set all 16 channels conversion frequency. It comprises of two four bit register (D00 to D03 and D04 to D07) both are written with codes 0 – 12 to generate frequencies of 1 Hz to 10 kHz in multiples of 1, 2, 5 or 10. (E.g. 0=1Hz, 1=2Hz, 2=5Hz, 3=10Hz and so on up to 10KHz).

Note: Both four bit registers must be loaded with the same desired clock rate value.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	X	X	X	X	X	X	X	F03	F02	F01	F00	F03	F02	F01	F00

5.5 Interrupt Vector

Read/write Address: 8 hex
The vector register is a 16 bit register which stores the interrupt vector value.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

5.6 Full-scale Trim & ID Page No

Read/write Address: A hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
PG2	PG1	PG0									U/D	STORE	S2	S1	INC

This first 5 bits D00 to D04 are used to control the resistor pot adjustments for the voltage reference to the DACs. There are 2 pots that can set the voltage reference for the common DACs 1-8(Bank A) and 9-16 (Bank B). There are 100 steps of approximately 1 bit/step per one of two gain adjustments selected by S1 or S2.

INC When asserted INC causes 1 step of adjustment up or down, dependent upon the U/D setting and if S1 or S2 are set.
S1 Select Voltage reference adjustment for bank A (DAC 1-8)
S2 Select Voltage reference adjustment for bank B (DAC 9-16)
STORE When high the current setting is stored in non-volatile memory.
U/D Programs the direction of the wiper adjustment. (Up=0, Down = 1)

For example to increment the wiper position on S1 set S1, INC high. To decrement S2 wiper position set S2, U/D and INC high

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PG0 Bit 0 of ID PROM Paging.*
PG1 Bit 1 of ID PROM Paging.*
PG2 Bit 2 of ID PROM Paging.*

*Since some carrier devices only support 64 locations in the ID PROM and the 8404 have up to 80 16-bit calibration values. Therefore it is required to page the ID PROM; these three bits are used to switch between pages of the ID PROM.

PG2	PG1	PG0	PAGE	NOTES
0	0	0	0 (Default)	Normal VITA4 format for ID PROM.
0	0	1	1	Calibration Values for +/-V Scan DAC Channel 0-5.
0	1	0	2	Calibration Values for +/-V Scan DAC Channel 6-11.
0	1	1	3	Calibration Values for +/-V Scan DAC Channel 12-16.
1	0	1	4	Calibration Values for +V Scan DAC Channel 0-5.
1	1	0	5	Calibration Values for +V Scan DAC Channel 6-11.
1	1	1	6	Calibration Values for +V Scan DAC Channel 12-16.

5.7 Number of Updates 2

Read/write Address: E hex

See Number of Updates 1

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

5.8 DAC Data Registers

Read/write Address: 10hex – 1Ehex
The 16 DACs are updated by these registers whenever they are overwritten and the EX bit is zero.
Dependent upon the voltage range the data format is straight binary, as shown in the table below:-

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

Bipolar Voltage Range	**Negative Full Scale**	**Zero**	**Positive Full Scale**
+/-10V	0Hex	8000h	7FFF Hex
+/-5V	0Hex	8000h	7FFF Hex
+/-2.5V	0Hex	8000h	7FFF Hex
Uni-polar Voltage Range	**Zero**	**Positive-Half Scale**	**Positive Full Scale**
+10V	0Hex	8000h	7FFF Hex
+5V	0Hex	8000h	7FFF Hex

Table showing data format dependent upon Voltage Range

5.9 DAC Command Registers

Read/write Address 30-4E hex

The command registers are used in conjunction with the DAC data registers. Due to the nature of the DACs the data and command registers must be set at the same time because the information is serially transferred to the DACs. Each DAC requires a 32 bit serial data stream, the first 16 bits form the command word and the last 16bits form the data to be written to the DACs. If the user wants to change the voltage range these command registers require modifying to reflect the range required. This allows each DAC to be at different voltage ranges if required.

D07	D06	D05	D04	D03	D02	D01	D00
C3	C2	C1	C0	0	0	0	0

Command Code (hex)	Action
	Copy data in Shift Register to Buffer 1
0	Copy the data in Buffer 1 to Buffer 2
1	Copy the data in Shift Register to Buffers 1 & 2
2	Not used
3	Not used
4	Not used
5	Not used
6	Not used
7	Set Range to 5V. Copy data in SR to Buffers 1 & 2.
8	Set Range to 10V. Copy data in SR to Buffers 1 & 2.
9	Set Range to +/-5V. Copy data in SR to Buffers 1 & 2.
10	Set Range to +/-10V. Copy data in SR to Buffers 1 & 2.
11	Set Range to +/-2.5V. Copy data in SR to Buffers 1 & 2.
12	Set Range to –2.5V to 7.5V. Copy data in SR to Buffers 1&2.
13	Not used.
14	No operation – no change.

On power up this register is set to zero and therefore must be set before the unit can be used as an initial setup. The DAC can be set to various modes of operation; the voltage ranges supported are +/-10V, 0V to +5V, 0V to +10V, +/-5V and +/-2.5V, which are hex codes 11, 8, 9, 10 and 12 respectively

6. ID PROM

As some IP Carrier Cards only support 64 16-Bit locations in the ID Space, we page the ID Space to provide extra space for DAC calibration data. To switch between pages, there are control bits in Full-Scale Trim & ID Page No Register (A Hex). The default setting is the standard 'VITA4' layout, but there are additional pages as shown below…

PG2	PG1	PG0	PAGE	NOTES
0	0	0	0 (Default)	Normal VITA4 format for ID PROM.
0	0	1	1	Calibration Values for +/-V Scan DAC Channel 0-5.
0	1	0	2	Calibration Values for +/-V Scan DAC Channel 6-11.
0	1	1	3	Calibration Values for +/-V Scan DAC Channel 12-16.
1	0	1	4	Calibration Values for +V Scan DAC Channel 0-5.
1	1	0	5	Calibration Values for +V Scan DAC Channel 6-11.
1	1	1	6	Calibration Values for +V Scan DAC Channel 12-16.

The +/- calibration factors are stored under pages 1 to 3. These are calculated for the +/-10V range, but these figures can be used to correct the errors for the +/-5V and +/-2.5V ranges. Similarly the positive calibration figures are stored under pages 4 to 6 and are calculated for the +10V range, but can also be used to correct errors on the +5V range.

The word addresses are as below:-

Base+80	ASCII 'VI'	5649h	
Base+82	ASCII 'TA'	5441h	
Base+84	ASCII '4 '	3420h	
Base+86	Hytec ID high byte	0080h	
Base+88	Hytec ID low word	0300h	
Base+8A	Model number	8404h	
Base+8C	Revision	1101h	This shows PCB Iss 1 Xilinx V101
Base+8E	Reserved	0000h	
Base+90	Driver ID	0000h	
Base+92	Driver ID	0000h	
Base+94	Flags	0002h	
Base+96	No of bytes used	001Ah	
Base+98	Cal Type	xxxxh	0 = No Calibration, 1 = Calibration factors Stored.
Base+9A	Serial Number	xxxxdec	
Base+9C	Not used	xxxxh	
Base+9E	WLO	5555h	

7. Calibration

The type of calibration factors held in the ID PROM are specified by the Cal Type held at Base+98 in the ID PROM:-

0 = No Calibration factors held in ID PROM.
1 = 3 Point Calibration factors Stored in ID PROM.

The Calibration Factors are held in the ID PROM pages 1 to 3 as shown the following Tables and as described in SECTION 7. These are the stored DAC values, derived from reading the DAC at the following specified voltages…

Value	Bipolar Calibration Voltage
nFS	-10V
zero	0V
pFS	+10V

Value	Uni-polar Calibration Voltage
zero	0V
pHS	+5V
pFS	+10V

Bipolar Voltage Range	Negative Full Scale	Zero	Positive Full Scale
+/-10V	40Hex	8000h	7FC0Hex
+/-5V	40Hex	8000h	7FC0Hex
+/-2.5V	40Hex	8000h	7FC0Hex
Uni-polar Voltage Range	**Zero**	**Positive-Half Scale**	**Positive Full Scale**
+10V	DHex	8000h	7FC0Hex
+5V	DHex	8000h	7FC0Hex

Calibration range

These values can then be used in the following equations to correct the offset and gain errors of the individual cannels of the DAC8404 IP card.

7.1 Bipolar Calibration Formula

$rawval > zero$

$$CalVal = \frac{(pFS - zero) \times (rawval - 0x8000)}{0x7FC0} + zero$$

$rawval < zero$

$$CalVal = \frac{(zero - nFS) \times (rawval - 0x8000)}{0x7FC0} + zero$$

7.2 Uni-polar Calibration Formula

$rawval > zero$

$rawval > pHS$

$$CalVal = \frac{(pFS - zero) \times (rawval)}{0xFFC0}$$

$rawval > zero$

$rawval < pHS$

$$CalVal = \frac{(pHS - zero) \times (rawval)}{0x7FE0}$$

$rawval < zero$

$$CalVal = \frac{(zero - 0) \times (rawval)}{0x000D}$$

7.3 ID Page 1 (PG2 = 0, PG1 = 0, PG0 = 1) +/- 10V Scan Calibration Values Layout.

The layout of the calibration pages is additionally dependant on the ‘Cal Type’ Value from the Default (Page 0) page of the ID PROM Section.

Address	Cal Type = 1
Base+80	DAC0 Cal data nFS
Base+82	DAC0 Cal data Zero
Base+84	DAC0 Cal data pFS
Base+86	DAC1 Cal data nFS
Base+88	DAC1 Cal data Zero
Base+8A	DAC1 Cal data pFS
Base+8C	DAC2 Cal data nFS
Base+8E	DAC2 Cal data Zero
Base+90	DAC2 Cal data pFS
Base+92	DAC3 Cal data nFS
Base+94	DAC3 Cal data Zero
Base+96	DAC3 Cal data pFS
Base+98	DAC4 Cal data nFS
Base+9A	DAC4 Cal data Zero
Base+9C	DAC4 Cal data pFS
Base+9E	DAC5 Cal data nFS
Base+A0	DAC5 Cal data Zero
Base+A2	DAC5 Cal data pFS
Base+A4	
Base+A6	
Base+A8	
Base+AA	
Base+AC	
Base+AE	
Base+B0	
Base+B2	
Base+B4	
Base+B6	
Base+B8	
Base+BA	

Table Key -

Cal data nFS - Negative Full Scale Calibration Factor.
Cal data Zero- Zero (0 Volts) Calibration Factor.
Cal data pFS - Positive Full Scale Calibration Factor.

7.4 ID Page 2 (PG2 = 0, PG1 = 1, PG0 = 0) +/- 10V Scan Calibration Values Layout.

The layout of the calibration pages is additionally dependant on the 'Cal Type' Value from the Default (Page 0) page of the ID PROM Section.

Address	Cal Type = 1
Base+80	DAC6 Cal data nFS
Base+82	DAC6 Cal data Zero
Base+84	DAC6 Cal data pFS
Base+86	DAC7 Cal data nFS
Base+88	DAC7 Cal data Zero
Base+8A	DAC7 Cal data pFS
Base+8C	DAC8 Cal data nFS
Base+8E	DAC8 Cal data Zero
Base+90	DAC8 Cal data pFS
Base+92	DAC9 Cal data nFS
Base+94	DAC9 Cal data Zero
Base+96	DAC9 Cal data pFS
Base+98	DAC10 Cal data nFS
Base+9A	DAC10 Cal data Zero
Base+9C	DAC10 Cal data pFS
Base+9E	DAC11 Cal data nFS
Base+A0	DAC11 Cal data Zero
Base+A2	DAC11 Cal data pFS
Base+A4	
Base+A6	
Base+A8	
Base+AA	
Base+AC	
Base+AE	
Base+B0	
Base+B2	
Base+B4	
Base+B6	
Base+B8	
Base+BA	

Table Key -

Cal data nFS - Negative Full Scale Calibration Factor.
Cal data Zero - Zero (0 Volts) Calibration Factor.
Cal data pFS - Positive Full Scale Calibration Factor.

7.5 ID Page 3 (PG2 = 0, PG1 = 1, PG0 = 1) +/- 10V Scan Calibration Values Layout.

The layout of the calibration pages is additionally dependant on the 'Cal Type' Value from the Default (Page 0) page of the ID PROM Section.

Address	Cal Type = 1
Base+80	DAC12 Cal data nFS
Base+82	DAC12 Cal data Zero
Base+84	DAC12 Cal data pFS
Base+86	DAC13 Cal data nFS
Base+88	DAC13 Cal data Zero
Base+8A	DAC13 Cal data pFS
Base+8C	DAC14 Cal data nFS
Base+8E	DAC14 Cal data Zero
Base+90	DAC14 Cal data pFS
Base+92	DAC15 Cal data nFS
Base+94	DAC15 Cal data Zero
Base+96	DAC15 Cal data pFS
Base+98	
Base+9A	
Base+9C	
Base+9E	
Base+A0	
Base+A2	
Base+A4	
Base+A6	
Base+A8	
Base+AA	
Base+AC	
Base+AE	
Base+B0	
Base+B2	
Base+B4	
Base+B6	
Base+B8	
Base+BA	

Table Key -

Cal data nFS - Negative Full Scale Calibration Factor.
Cal data Zero - Zero (0 Volts) Calibration Factor.
Cal data pFS - Positive Full Scale Calibration Factor.

7.6 ID Page 4 (PG2 = 1, PG1 = 0, PG0 = 1) +10V Scan Calibration Values Layout.

The layout of the calibration pages is additionally dependant on the 'Cal Type' Value from the Default (Page 0) page of the ID PROM Section.

Address	Cal Type = 1
Base+80	DAC0 Cal data zero
Base+82	DAC0 Cal data pHS
Base+84	DAC0 Cal data pFS
Base+86	DAC1 Cal data zero
Base+88	DAC1 Cal data pHS
Base+8A	DAC1 Cal data pFS
Base+8C	DAC2 Cal data zero
Base+8E	DAC2 Cal data pHS
Base+90	DAC2 Cal data pFS
Base+92	DAC3 Cal data zero
Base+94	DAC3 Cal data pHS
Base+96	DAC3 Cal data pFS
Base+98	DAC4 Cal data zero
Base+9A	DAC4 Cal data pHS
Base+9C	DAC4 Cal data pFS
Base+9E	DAC5 Cal data zero
Base+A0	DAC5 Cal data pHS
Base+A2	DAC5 Cal data pFS
Base+A4	
Base+A6	
Base+A8	
Base+AA	
Base+AC	
Base+AE	
Base+B0	
Base+B2	
Base+B4	
Base+B6	
Base+B8	
Base+BA	

Table Key -
Cal data Zero - Zero (0 Volts) Calibration Factor.
Cal data pHS - Positive Half-Full Scale Calibration Factor.
Cal data pFS - Positive Full Scale Calibration Factor.

7.7 ID Page 5 (PG2 =1, PG1 = 1, PG0 = 0) +10V Scan Calibration Values Layout.

The layout of the calibration pages is additionally dependant on the ‘Cal Type’ Value from the Default (Page 0) page of the ID PROM Section.

Address	Cal Type = 1
Base+80	DAC6 Cal data zero
Base+82	DAC6 Cal data pHS
Base+84	DAC6 Cal data pFS
Base+86	DAC7 Cal data zero
Base+88	DAC7 Cal data pHS
Base+8A	DAC7 Cal data pFS
Base+8C	DAC8 Cal data zero
Base+8E	DAC8 Cal data pHS
Base+90	DAC8 Cal data pFS
Base+92	DAC9 Cal data zero
Base+94	DAC9 Cal data pHS
Base+96	DAC9 Cal data pFS
Base+98	DAC10 Cal data zero
Base+9A	DAC10 Cal data pHS
Base+9C	DAC10 Cal data pFS
Base+9E	DAC11 Cal data zero
Base+A0	DAC11 Cal data pHS
Base+A2	DAC11 Cal data pFS
Base+A4	
Base+A6	
Base+A8	
Base+AA	
Base+AC	
Base+AE	
Base+B0	
Base+B2	
Base+B4	
Base+B6	
Base+B8	
Base+BA	

Table Key -

Cal data Zero - Zero (0 Volts) Calibration Factor.
Cal data pHS - Positive Half-Full Scale Calibration Factor.
Cal data pFS - Positive Full Scale Calibration Factor.

7.8 ID Page 6 (PG2 = 1. PG1 = 1, PG0 = 1) +10V Scan Calibration Values Layout.

The layout of the calibration pages is additionally dependant on the ‘Cal Type’ Value from the Default (Page 0) page of the ID PROM Section.

Address	Cal Type = 1
Base+80	DAC12 Cal data zero
Base+82	DAC12 Cal data pHS
Base+84	DAC12 Cal data pFS
Base+86	DAC13 Cal data zero
Base+88	DAC13 Cal data pHS
Base+8A	DAC13 Cal data pFS
Base+8C	DAC14 Cal data zero
Base+8E	DAC14 Cal data pHS
Base+90	DAC14 Cal data pFS
Base+92	DAC15 Cal data zero
Base+94	DAC15 Cal data pHS
Base+96	DAC15 Cal data pFS
Base+98	
Base+9A	
Base+9C	
Base+9E	
Base+A0	
Base+A2	
Base+A4	
Base+A6	
Base+A8	
Base+AA	
Base+AC	
Base+AE	
Base+B0	
Base+B2	
Base+B4	
Base+B6	
Base+B8	
Base+BA	

Table Key -

Cal data Zero - Zero (0 Volts) Calibration Factor.
Cal data pHS - Positive Half-Full Scale Calibration Factor.
Cal data pFS - Positive Full Scale Calibration Factor.

8. SELECTION OF THE +/-12 VOLT POWER SUPPLY

The DAC 8404 +/-12 volt power supply can be derived either internally from the carrier card or from an external source via a transition card. The source is selected using jumpers J1, J2 and the GND AGND link LNK1 where:

J1 External +12V connect 1 & 2, Internal +12V connect 2 & 3
J2 External -12V connect 1 & 2, Internal -12V connect 2 & 3
J3 Make link to boot FPGA from PROM (Factory setting), remove to use JTAG test header

LNK1 (GND AGND)
IN for internal +/-12V
OUT for external +/-12V (supplied from transition card DC DC converter).

9. I/O Connector – 50 way on 8404 DAC Board

Pin	Signal	Pin	Signal
1	Output 1	26	AGND
2	AGND	27	Output14
3	Output 2	28	AGND
4	AGND	29	Output15
5	Output 3	30	AGND
6	AGND	31	Output16
7	Output 4	32	AGND
8	AGND	33	N.C.
9	Output 5	34	N.C.
10	AGND	35	XTrigger
11	Output 6	36	/XTrigger
12	AGND	37	N.C.
13	Output 7	38	N.C.
14	AGND	39	XClk
15	Output 8	40	/XClk
16	AGND	41	+12VX
17	Output9	42	AGND
18	AGND	43	+12VX
19	Output10	44	AGND
20	AGND	45	-12VX
21	Output11	46	AGND
22	AGND	47	-12VX
23	Output12	48	AGND
24	AGND	49	N.C.
25	Output13	50	AGND

10.HYTEC TRANSITION CARD 8204 CONNECTIONS

I/O Connector – 50 way on transition panel

Pin	Signal	Pin	Signal
1	AGND	26	Output1
2	AGND	27	Output 2
3	AGND	28	Output 3
4	AGND	29	Output 4
5	AGND	30	Output 5
6	AGND	31	Output 6
7	AGND	32	Output 7
8	AGND	33	Output 8
9	AGND	34	Output 9
10	AGND	35	Output 10
11	AGND	36	Output 11
12	AGND	37	Output 12
13	AGND	38	Output 13
14	AGND	39	Output 14
15	AGND	40	Output 15
16	AGND	41	Output 16
17		42	
18	XTRIG N	43	XTRIG P
19		44	
20	XCLK N	45	XCLK P
21		46	
22		47	
23		48	
24	AGND	49	AGND
25	AGND	50	AGND

11. Appendix A: Pseudo Code Examples

11.1 DAC update by Register

The following pseudo code is the sequence of actions required to immediately update any DAC Channel's output via the Data Registers.

1. Update Clock Rate Register. The Desired Clock Rate MUST Be Written to Both Nibbles of Least Significant Byte of the Clock Rate Register.
2. Both Number of Update Registers MUST Be Loaded with 0xFFFF.
3. Set the DAC Voltage Range via the relevant DAC Command Register.
4. Write DAC Value to the output via the relevant DAC Data Register.
5. Set the Arm bit in CSR.

11.2 Update DAC from Waveform Memory Data

The following pseudo code is the sequence of actions required to allow a waveform from memory update of any DAC Channel's output. It assumes the 1 Mb Version of the 8404 is being used and the output will be triggered by the software.

1. Ensure the DAC is disarmed (i.e. the Arm bit in the CSR is NOT set).
2. Ensure the 1Mb Memory Bit in the CSR is Set.
3. Set the DAC Voltage Range via the relevant DAC Command Register.
4. Write the initial Waveform Value to the output (via the relevant DAC Data Register).
5. Write 32K of 16 Bit Samples of the required Waveform into the desired DAC channel's Memory.
6. Both Upgrade Registers MUST Be Loaded with 0 (For Whole Memory)
7. Setup Waveform Output by arming the DAC and allowing it to accept a trigger, i.e. set the arm and external trigger bits in the CSR. If you want the output to be cyclically continuously updated from the memory also set the continuous bit in the CSR at the same time.
8. To start the waveform output set the software trigger bit in the CSR.