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ADC8411
ADC INDUSTRY PACK
16BIT RESOLUTION
16 CHANNELS

USERS MANUAL

PCB Issue 1.0
Xilinx Version 8411V103

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CONTENTS

1. Description

The Hytec IP-ADC-8411 is an Industry Pack that provides 16 channels of simultaneously sampled analogue digitisation with the following characteristics:-

- 16 independently programmed channels
- 16 bits resolution
- Single full-scale and offset trim.
- Differential inputs.
- 0V to 5V unipolar full-scale standard.
- 0V to 10V unipolar full-scale 'version U'.
- Front-end instrumentation amplifiers can be factory set for gains of up to x1000.
- FIFO memory gives 256 16bit samples for each of the 16 channels.
- Low offset error - +/- 1.5mV max
- Low gain error - +/- 0.05% full scale standard.
- Low gain error - +/- 0.1% full scale 'version U'.
- Low error drift - 10ppm per deg C
- Code format: 0000h = 0V, and FFFFh = +5V.
- High input impedance – 5Gohms.
- Up to 100KHz sampling rate
- Simultaneous sampling – 2us acquisition time
- System to plant isolation to 100V when externally powered by DC/DC converter option
- Serial number, PCB issue and firmware issue held in ID PROM
- 8MHz and 32MHz operation.

2. Overall Specifications

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of channels:	16
ADC resolution:	16 bits
Diff. Non-linearity:	Monotonic to 15 bits (at 50kHz throughput)
Int. Non-linearity:	+/-0.018% of full scale (at 50kHz throughput)
Offset error:	+/-1.5mV uncorrected.
Offset drift:	+/-0.5ppm per deg C typical
Gain error:	+/-0.05% uncorrected standard or +/-0.10% uncorrected 'version U'.
Gain drift:	+/-0.5 ppm per deg C typical
Range:	+5V or +10V full-scale (+ve input referred to –ve input)
Cross-talk:	+/-1LSB channel to channel for FS input on adjacent channel.
CMRR	Greater than 60dB
CMV	+/-12V.
Overvoltage:	+/-40V.
Throughput:	100KHz max
Acquisition time:	2us
Conversion time:	8us
Bandwidth:	20kHz (factory set – other cut-offs can be specified)
SNR:	-90dB at 1kHz typical
SINAD:	-90dB at 1kHz typical
Isolation:	100V via opto-isolators (if externally powered)
Data format:	16 bits straight binary
Memory:	Buffer register for each conversion and FIFO for all 16
Power:	+5V @ 300mA typical +/-12V @ 200mA typical when switched to internal

3. Operating Modes

There are two operating modes:-

1. Register mode – the last ADC reading may be read at random from each addressed ADC register.
2. Triggered sampling – When the board is triggered conversions are stored in to the FIFO memory which will hold 256 16bit samples for each of the 16 channels. An interrupt can be generated when the FIFO is full. Once triggered and FULL the external FIFO remains unchanged until it is read completely. The unit can only be retriggered once the FIFO had been emptied. Once the unit has been triggered by software or hardware trigger the trigger cannot be removed until the FIFO is full.

4. Application Registers

There are five application specific (I/O) registers; the CSR, the clock rate, the interrupt vector value, the ADC FIFO and the FIFO fullness counter. There are also 16 ADC buffer registers.

4.1 Control & Status Register (CSR)

4.2 Control

Write Address: 0 hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ARM	ET	ST	XC	EG	x	ETF	x	x	x	x	RSTF IFO	x	x	x	x

Status

Read Address: 0 hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ARM	ET	ST	XC	EG	x	ETF	x	x	ARM GO	x	RST FIFO	EFE	x	EFF	x

X = Not Used

ARM Software ARM when set, arms the ADCs and sets ‘ARM GO’ bit (when EG not set).
ET Enable trigger. If set allows external trigger or software trigger to route sampled conversions to the FIFO. The action is synchronised to the first sample clock after the rising edge of trigger.
ST Software trigger. Allows trigger action to be initiated by software command.
XC Enable External Sample Clock. If set to zero internal clock is used for the sample rate. If set true the external clock is used for the sample clock without frequency division.
EG Enable Hardware ARM. When IP Strobe* (pin 46 of the IP logic interface connector) signal is released ‘ARM GO’ bit is set (on Hytec 8001/2/4 carrier cards IP Strobe from front panel ‘INHIBIT’).
ETF Enables interrupt when the FIFO memory is full.
ARM GO This indicates the unit is ARMed and acquiring ADC data at the sample clock rate.
RST FIFO If this is set to a ‘1’ the FIFO and control logic are reset.
EFE The FIFO memory is empty.
EFF The FIFO memory is full.

4.3 Clock Rate

Read/write Address: 6 hex

The clock rate register is a four bit register which enables codes 0 – 15 to enable frequencies of 1 Hz to 100kHz in multiples of 1,2,5 or 10. (E.g. 0=1Hz, 1=2Hz, 2=5Hz, 3=10Hz and so on to 15=100KHz) Each clock pulse will initiate simultaneous ADC conversions and store them in memory.

4.4 Vector

Read/write Address: 8 hex
The vector register is a 16 bit register which stores the interrupt vector value.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

4.5 Register Not used

Read/write Address: A hex

4.6 ADC FIFO

Read/write Address: C hex
Read/write the FIFO memory (256 conversions per channel). The FIFO can also be read in IP memory space.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

4.7 FIFO Fullness Counter

Read Address: E hex
Up/down counter which count conversions as they are entered / read from the FIFO. At the end of each trigger/readout sequence the value in the registers should be zero.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0

4.8 ADC Registers

Read/write Address: 10hex – 2Ehex
The sixteen ADC buffer registers store the last sample conversions and may be read at any time.
Data format 0000h = 0V and FFFFh = +5V or Data format 0000h = 0V and FFFFh = +10V.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

5. ADC Operation

5.1 FIFO Memory

The FIFO memory when triggered will store 256 16bit samples of each of the 16 channels as shown in the figure below. Once the FIFO is triggered it will continue to store all 256 samples of each channel until it is full. This may be indicated to the carrier board by setting 8411 IntReq0* line. Once full the entire contents of the FIFO must be read out completely before a new trigger can be initiated (this is to ensure the integrity of the memory map below).

The FIFO may be readout as it is filling but is not recommended as the channel locations may not follow the memory map below.

External FIFO Memory Map			
Sample Number	**Channel Number**	**FIFO Location**	**FIFO Contents**
1	1	1	16 bit sample 1 of channel 1
1	2	2	16 bit sample 1 of channel 2
1	3	3	16 bit sample 1 of channel 3
1	4	4	16 bit sample 1 of channel 4
1	5	5	16 bit sample 1 of channel 5
1	6	6	16 bit sample 1 of channel 6
1	7	7	16 bit sample 1 of channel 7
1	8	8	16 bit sample 1 of channel 8
1	9	9	16 bit sample 1 of channel 9
1	10	10	16 bit sample 1 of channel 10
1	11	11	16 bit sample 1 of channel 11
1	12	12	16 bit sample 1 of channel 12
1	13	13	16 bit sample 1 of channel 13
1	14	14	16 bit sample 1 of channel 14
1	15	15	16 bit sample 1 of channel 15
1	16	16	16 bit sample 1 of channel 16
2	1	17	16 bit sample 2 of channel 1
2	2	18	16 bit sample 2 of channel 2
--	--	--	--
Repeat	Repeat	Repeat	Repeat
--	--	--	--
256	13	4093	16 bit sample 256 of channel 13
256	14	4094	16 bit sample 256 of channel 14
256	15	4095	16 bit sample 256 of channel 15
256	16	4096	16 bit sample 256 of channel 16

FIFO Memory Map

5.2 ADC Register Update

There are sixteen ADC buffer registers (addresses 10hex – 1Ehex) which store the last sampled conversions and may be read at any time. The channel order is channel 1 at address 10hex to channel 16 at address 2E. All 16 ADC registers are updated simultaneously.
Data format 0000h = 0V, and FFFFh = +5V.

6. FIFO IN IP MEMORY SPACE

The FIFO memory can also be read out from IP memory space. This allows the FIFO to be read out using BLT or MBLT from the Hytec 8004 carrier card. Using the Hytec 8004 fully populated with 8411 can read all 4 cards FIFO memory at once using VME MBLT 64bit operation.

7. ID PROM

The word addresses are as below:-

Base+80	ASCII 'VI'	5649h	
Base+82	ASCII 'TA'	5441h	
Base+84	ASCII '4 '	3420h	
Base+86	Hytec ID high byte	0080h	
Base+88	Hytec ID low word	0300h	
Base+8A	Model number	8411h	
Base+8C	Revision	0103h	This shows PCB Iss 1 Xilinx V03
Base+8E	Reserved	0000h	
Base+90	Driver ID	0000h	
Base+92	Driver ID	0000h	
Base+94	Flags	0002h	
Base+96	No of bytes used	001Ah	
Base+98	Cal Type	xxxxh	0 = No Calibration factors, 2 = Calibration factors Stored.
Base+9A	Serial Number	xxxxdec	
Base+9C	Not used	0000h	
Base+9E	WLO	5555h	

8. Isolation

The ADC 8411 +/-12 volt power supply can be derived either internally (non-isolated) from the carrier card (VME +/-12V) or from external isolating DC-DC converters (type 8912) mounted on an 8211 transition card. The source is selected using jumpers J1, J2 and the GND-AGND link.

J1 External +12V connect 1 & 2, Internal +12V connect 2 & 3
J2 External -12V connect 1 & 2, Internal -12V connect 2 & 3
J3 Select unipolar 0 to5V (2-3) or bipolar +/-2.5V (1-2)
J4 Factory set (boot jumper)

GND-AGND Link
IN for internal +/-12V (non-isolated)
OUT for external +/-12V (isolated and supplied from transition card DC-DC converter).

9. I/O Connector – 50 way on 8411 ADC Board

Pin	Signal	Pin	Signal
1	Input 1 +	26	Input 13 -
2	Input 1 -	27	Input 14 +
3	Input 2 +	28	Input 14 -
4	Input 2 -	29	Input 15 +
5	Input 3 +	30	Input 15 -
6	Input 3 -	31	Input 16 +
7	Input 4 +	32	Input 16 -
8	Input 4 -	33	
9	Input 5 +	34	
10	Input 5 -	35	XTrig+
11	Input 6 +	36	XTrig-
12	Input 6 -	37	N.C.
13	Input 7 +	38	N.C.
14	Input 7 -	39	XClk+
15	Input 8 +	40	XClk-
16	Input 8 -	41	+12VX
17	Input 9 +	42	AGND
18	Input 9 -	43	+12VX
19	Input 10 +	44	AGND
20	Input 10 -	45	-12VX
21	Input 11 +	46	AGND
22	Input 11 -	47	-12VX
23	Input 12 +	48	AGND
24	Input 12 -	49	AGND
25	Input 13 +	50	AGND

10. Transition Card Connections

TB 8211 I/O Connector – 50 way on transition

Connectors 1-4

Pin	Signal	Pin	Signal
1	Inp1 -	26	Inp1 +
2	Inp2 -	27	Inp2 +
3	Inp3 -	28	Inp3 +
4	Inp4 -	29	Inp4 +
5	Inp5 -	30	Inp5 +
6	Inp6 -	31	Inp6 +
7	Inp7 -	32	Inp7 +
8	Inp8 -	33	Inp8 +
9	Inp9 -	34	Inp9 +
10	Inp10 -	35	Inp10 +
11	Inp11 -	36	Inp11 +
12	Inp12 -	37	Inp12 +
13	Inp13 -	38	Inp13 +
14	Inp14 -	39	Inp14 +
15	Inp15 -	40	Inp15 +
16	Inp16 -	41	Inp16 +
17		42	
18	Xtrig -	43	Xtrig +
19		44	
20	XClk -	45	XClk +
21	AGnd	46	+12V
22	AGnd	47	+12V
23	AGnd	48	-12V
24	AGnd	49	-12V
25	AGnd	50	