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ADC8414
16-CHANNEL 16-BIT ADC INDUSTRY PACK

USERS MANUAL

PCB Issue 2
Firmware Version 8414V202
8MHz or 32MHZ IP Clock

Document Nos.: ADC8414/UTM/G/x/2.3
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Author: MRN

Revision History

The following table shows the revision history for this document.

Date	Version	Change Notes
02/12/10	0.2	Preliminary
16/03/11	1.0	PCB issue 1
14/07/11	2.0	Issue 2 PCB enables System to plant isolation to 100V when externally powered by DC/DC converter option. Separate register to allow gain range to be split in to two banks.
19/01/12	2.1	CONT bit added to ExtCSR to allow multiple triggers in CC mode. Unit can be set to trigger from rising, falling or both edges via bits in register Firmware up issue to 8414v202
19/01/12	2.2	CC and DA more explanation
19/04/12	2.3	The manual highlights the preferred type of Transition card to use and the need to use proper grounding techniques.

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1. INTRODUCTION

The Hytec IP-ADC-8414 is an Industry Pack that provides 16 channels of simultaneously sampled analogue digitisation and programmable gain ranges with the following characteristics:-

- 16 independent channels (one ADC per input).
- True full differential inputs.
- High input impedance - 1Gohms.
- Over voltage +/-25V.
- 8401 register superset and connection pin layout.
- 16 bits resolution – 16 bits no missing codes.
- 14 bits accuracy.
- On board RAM Memory 1M x 16 bits (64K conversions per channel).
- Programmable full-scale resolution all inputs +/-10V or +/-5V.
- Front-end programmable gain instrumentation amplifiers giving gains of 1, 2, 4 and 8.
- Active low pass filter.
- On-board calibration by FPGA firmware using stored offset and gain.
- Gain drift - 2ppm per deg C (typ).
- Offset drift - +/-3.5uV/degC (typ).
- +/-10V offset error - +/-3LSBs with firmware calibration (+/- 2.5mV without calibration).
- +/-5V offset error - +/-4LSBs with firmware calibration (+/- 2.5mV without calibration).
- +/-10V gain error - +/-3LSBs with firmware calibration (+/- 0.75% FS without calibration).
- +/-5V gain error - +/-4LSBs with firmware calibration (+/- 0.75% FS without calibration).
- Up to 200KHz sampling rate.
- On-board sample clock programmable to 200kHz.
- Ext sample clock input.
- Ext trigger input
- Aperture Delay 5 ns typ
- Aperture Delay Matching 250 ps typ
- Aperture Jitter 50 ps typ
- ADC voltage reference drift 1.0ppm/^{o}C (max)
- Board type, Serial number, PCB issue and firmware issue held in ID PROM.
- 8/32MHz IP system clock operation.
- Field upgradeable firmware (requires Xilinx/compatible device to program built in FPGA flash memory via the FPGA JTAG port).
- EPICS and ASYN driver support.
- System to plant isolation to 100V when externally powered by DC/DC converter option.
- PCB temperature measurement via onboard chip.

2. PRODUCT SPECIFICATIONS

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of channels:	16
ADC resolution:	16 bits
Diff. Non-linearity:	+/-0.75 LSB TYP
Int. Non-linearity:	+/-1.5 LSB TYP
Offset error:	+/-10V offset error - +/-3LSBs with firmware calibration (+/- 2.5mV without calibration). +/-5V offset error - +/-4LSBs after firmware calibration (+/- 2.5mV without calibration).
Offset drift:	+/-3uV/degC (typ).
Gain error:	+/-10V gain error - +/-3LSBs after firmware calibration @ 25 deg C (+/- 0.75% FS without calibration). +/-5V gain error - +/-4LSBs after firmware calibration @ 25 deg C (+/- 0.75% FS without calibration).
Gain drift:	2ppm per deg C (typ).
Range:	+/-10V or +/-5V full scale (+ve input referred to –ve input)
Overvoltage:	+/-25V
Bandwidth (-3dB):	125KHz
Throughput:	200KHz
SNR:	ADC Signal-to-Noise 90dB(min) 91.5dB (typ)
SINAD:	ADC Signal-to-Noise + Distortion (SINAD) 87dB(min) 89.5dB (typ)
Isolation:	100V via opto-isolators (if externally powered)
ADC device:	TI ADS8556
Data format:	16 bits straight binary
Memory:	1M x 16 bits (16 channels gives 64K conversions per channel).
Power:	+5V @ 200mA typical +12V @ 230mA typical when switched to internal -12V @ 120mA typical when switched to internal

3. Operating Modes

3.1 Register mode

This mode is enabled by setting ARM = '1' (bit 15 of the CSR) and EX='0' (bit 14 of the CSR).
As soon as the ARM bit is set (no trigger required) the ADCs sample at the sample rate which is derived either from the internal clock whose rate is set by the Internal Sample Rate register or by the external sample clock supplied by the user via the rear transition card see .
The ADC data registers are updated at the conversion rate. These registers can be read in any order at any time.
The memory is also updated at the sample rate and is continuously updated rapping round on reaching the end of the memory until the ARM bit is cleared.
There are sixteen ADC buffer registers (addresses 10hex – 2Ehex) which store the last sampled conversions and may be read at any time. The channel order is channel 1 at address 10hex to channel 16 at address 2E.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0

Data format 000Fh = –10v, 8000h = 0V and FFF1h = +10V.
Data format 000Fh = –5v, 8000h = 0V and FFF1h = +5V.

3.2 Triggered sampling

This mode is enabled by setting ARM = '1' (bit 15 of the CSR) and EX='1' (bit 14 of the CSR). Then when a software or hardware trigger is detected conversions are stored in the RAM memory at the sample rate set.
The sample rate is derived either from the internal clock whose rate is set by the Internal Clock Rate register or by the external clock supplied by the user.
The value written to the memory pointer register gives the starting point in memory that the conversions are stored to.
The point at which conversions are stopped is set by the Number of Counts register.
The address the unit stops at is given by the Memory Conversion pointer register.
This mode also updates the ADC Data registers at the conversion rate. These registers can be read in any order at any time.
The Hardware trigger can be set by a bit in the extended CSR to trigger on the rising edge or falling edge or both. The unit defaults to Rising edge.

4. Memory Map

A bit in the control register of the 8414 allows selection of either 1Mb memory (32K samples/channel) when set at logic 1 or 2Mb (64K samples/channel) when set at logic 0.
When set to 2Mb memory size the memory is split up in to two halves giving an upper and lower conversion memory.
These areas are further divided into sixteen segments allocated to conversions from ADC1 to ADC16 as shown in the table below.
When the lower buffer has been filled the Half Full Flag status is set and when the upper memory is full the Full Flag status is set.

1M = '0' (bit 7 of the CSR) this sets memory size to 2Mb

Lower Conversion Memory	Upper Conversion Memory
ADC16 conversions	ADC16 conversions
ADC15 conversions	ADC15 conversions
ADC14 conversions	ADC14 conversions
ADC3 conversions	ADC3 conversions
ADC2 conversions	ADC2 conversions
ADC1 conversion 32k ADC1 conversion 32k-1 ADC1 conversion 2 ADC1 conversion 1	ADC1 conversion 64k ADC1 conversion 64k-1 ADC1 conversion 32k+2 ADC1 conversion 32k+1

When 1Mb memory size set the channels are arranged as shown in the table below.

1M = '1' (bit 7 of the CSR) this sets memory size to 1Mb

Lower Conversion Memory	Upper Conversion Memory
ADC16 conversions	
ADC15 conversions	
ADC14 conversions	
ADC3 conversions	
ADC2 conversions	
ADC1 conversion 32k ADC1 conversion 32k-1 ADC1 conversion 2 ADC1 conversion 1	Not Used

5. Application Registers

There are six application specific (I/O) registers and consists of the following the:

- CSR,
- memory conversion pointer,
- number of samples per trigger (NCO),
- clock rate,
- interrupt vector value
- Extended CSR.

There are also 16 ADC buffer registers.

5.1 Control & Status Register (CSR)

5.2 Control

Write Address: 0hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ARM	EX	ST	XC	ET	EE	FE	HE	1M	DA	EII	MII	x	CC	F	HF

Status

Read Address: 0hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ARM	EX	ST	XC	ET	EE	FE	HE	1M	DA	EII	MII	MIS	CC	F	HF

ARM Arm the ADCs. Allow conversions either continuous or triggered.

EX Enable trigger. If not set continuously sample at the clock rate. If set allows external trigger or software trigger

ST Software trigger. Triggers a programmed number of samples. ST is cleared on completion.

XC Enable the external clock. If 0 the internal clock is used for the sample rate. If set true the external clock is used for the sample clock without frequency division.

ET When logic '0' disable hardware memory inhibit input. When logic '1' enable hardware memory inhibit from IP **Strobe*** line *(on Hytec 800x IP carrier card, this signal is driven from the front panel INHIBIT lemo)*.

EE Enables interrupt at end of sampling sequence.

FE Enables interrupt when the upper conversion memory has been filled. (Memory Full).

HE Enables interrupt when the lower conversion memory has been filled. (Memory Half Full).

1M Enables 1Mb memory (64K samples/channel) when logic 1 and 2Mb (128K samples/channel) when logic 0.

DA Set to 1 allows the unit to disarm on completion of memory acquisition. Set which event this occurs on by setting EE, FE or HE. If continues mode set and EE set then the disarm will override the continues mode and the unit will stop.

EII This enables an interrupt to be generated when ever the memory inhibit bit (MIS) is set.

MII **(Write)** When set to logic '1' hardware memory inhibit interrupt is cleared but not disabled. **(Read)** Shows that an interrupt has been generated from hardware memory inhibit.

MIS **(Read Only)** this bit indicates that the hardware memory inhibited on the IP **Strobe*** line is asserted when at logic '1' (*driven from the front panel INHIBIT lemo on Hytec 800x IP carriers)*.

CC Conversions complete. Status bit set when the number of programmed samples has been completed. Generates IRQ0* if set and EE is set to a logic 1. Clear by writing '0' to this bit this removes the interrupt and allows the unit to be triggered again (when **not** set in continues mode).

In continues mode this bit is set after the first programmed number of samples has been completed. Again this bit can be cleared by writing '0' and will again set its self after the next programmed number of samples has been completed.

F Full status. Set when the upper conversion memory has been filled. Generates IRQ0* if set and FE is set to a logic 1.

HF Half full status. Set when the lower conversion memory has been filled. Generates IRQ0* if set and HE is set to a logic 1.

5.3 Conversion Pointer

Read/write Address: 2hex
The current conversion address is given by the conversion address offset by the ADC number. This register can be written too when the unit is ARMed.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

5.4 Number of conversions

Read/write Address: 4hex
The number of conversions register allows the number of samples per trigger to be programmed.
If a number of triggers occur and the memory buffer size of 64K of conversions per channel is exceeded the conversions will wrap around from the upper memory to the base of the lower memory.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

The following should be loaded in to the NOC to output whole or half the memory in the following modes.

Mode	NOC Values	
	Half Full	Full
16 Bit 2Mb	0x8000 (32K samples)	0x0 (64K samples)
16 Bit 1Mb	0x4000 (16K samples)	0x8000 (32K samples)

When 1Mb is set it only changes when the Full and Half Full flags and interrupts occur as shown in the above table. The user must ensure that the correct NOC value is entered as the setting of the 1Mb in the CSR does not effect the NOC operation.

5.5 ADC Sample Rate

Read/write Address: 6hex

The first five bits in the sample rate register are used to enables codes 0 – 16 to enable frequencies of 1 Hz to 200KHz in multiples of 1,2,5 or 10. (E.g. 0=1Hz, 1=2Hz, 2=5Hz, 3=10Hz and so on to 15=100KHz, 16=200KHz) Each clock pulse will initiate simultaneous ADC conversions and store them in memory.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	S4	S3	S2	S1	S0

Clock rate Reg (S4 to S0)	Frequency Hz	Clock rate Reg (S4 to S0)	Frequency Hz
00000	1	01001	1KHz
00001	2	01010	2KHz
00010	5	01011	5KHz
00011	10	01100	10KHz
00100	20	01101	20KHz
00101	50	01110	50KHz
00110	100	01111	100KHz
00111	200	10000	200KHz
01000	500		

5.6 Interrupt Vector

Read/write Address: 8hex

The vector register is a 16 bit register which stores the interrupt vector value.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

5.7 Extended Control & Status Register (CSR Ext)

Read/write Address: Ahex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
	CAL	BTE	TE		E	EFW	IFW		R		Cont	ISE	IS	SMI	TEN

TEN This shows the trigger status of the unit (Read only).

SMI This sets **S**oftware **M**emory **I**nhibit when at logic '1'. This does not generate an interrupt or set the MIS in the CSR.

IS ADC Register update status. Set when the ADC Registers have been updated. Generates IRQ0* if set and ISE is set to a logic 1.

ISE Enables interrupt when ADC Registers have been updated.

CONT If set to '1' then will allow multiple triggers in CC mode. On each trigger the Sample clock is restarted. A max delay of 100ns between Trigger and the first conversion is guaranteed.

R Set ADC range set to 0 = +/-10V and range set to 1 = +/-5V.

IFW **Do not set this bit as setup and calibration data maybe lost.** This bit enables the FPGA flash write from buffer command

EFW **Do not set this bit as setup and calibration data maybe lost.** This bit enables the External flash write by writing to IP mem i.e. switches off RAM

E **Do not set this bit as setup and calibration data maybe lost.** This bit enables the External flash chip or sector erase when do a IP write to mem. If IP data is 0x10 then chip erase (64s time taken) if IP data is 0x30 then sector erase where the sector address is given in the IP memory address lines. If chip erase then IP mem address = 0x555 and data 0x10.

TE When set to '0' = Ext Trigger on rising edge when '1' ext trigger on falling edge

BTE When set to '1' = Ext trigger on both edges

CAL If set to '1' unit does not use on board flash calibration ***for register updates only.*** If EX=1 then this has no effect. Used for production test.

5.8 Front End Instrumentation Amplifier Gain Register

Read/write Address: Chex

Set gain of front end instrumentation amplifier 1, 2, 4 or 8.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
												A1 B2	A0 B2	A1 B1	A0 B1

A0_B1 and A1_B1 control the gain of the first 8 instrumentation amplifiers.
A0_B2 and A1_B2 control the gain of the last 8 instrumentation amplifiers.

5.9 ADC Registers

Read only Address: 10hex – 2Ehex
The sixteen ADC buffer registers store the last sample conversions and may be read at any time.
Data format 000Fh = –10v, 8000h = 0V and FFF1h = +10V.
Data format 000Fh = –5v, 8000h = 0V and FFF1h = +5V.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

6. ADC OPERATION

6.1 Memory Update Inhibit and Interrupt

The updating of the conversion memory can be stopped by controlling the external IP **Strobe*** line *(on the Hytec 8002 IP carrier card, this signal is driven from the front panel INHIBIT lemo)*.
When the STROBE line is taken low and the enable hardware memory inhibit bit (ET) is set in CSR the updating of the conversion memory is stopped. This is indicated by the MIS bit in the CSR going high.
On memory update inhibit an interrupt can be generated if the **E**nable Memory **I**nhibit **I**nterrupt enable bit (EII) is set in the CSR. The **M**emory **I**nhibit **I**nterrupt (MII) bit of the CSR flags an interrupt. This is cleared by either clearing the EII in the CSR or by writing a '1' to MII bit in the CSR which clears the Memory Inhibit Interrupt without the need to clear the EII in the CSR.
The IP **Strobe*** line needs to be taken high then low after interrupt cleared to generate a new interrupt.

6.2 Set Number of Conversions

The number of conversions register (NCO) at address 2hex allows the number of samples per trigger to be programmed. The maximum number of conversions is 32K of samples 1MB and 64K of samples for 2MB for each channel before the Conversion Complete (CC) flag is set in the CSR. An interrupt is generated if the Enable Interrupt on Last Sample (EE) bit is set in the CSR. To clear the interrupt write a '0' to the CC bit of the CSR.
If a number of triggers occur and the memory buffer size of 64K of conversions per channel is exceeded the conversions will wrap around from the upper memory to the base of the lower memory.

6.3 Triggering

The triggering of the ADC8414 is only used when the number of conversions has been set in the Number of Conversions register and the Enable Trigger (EX) bit has been set in the CSR.

6.3.1 Software Trigger

The unit can be triggered by a software trigger by writing a '1' to the Software Trigger (ST) bit of the CSR.

6.3.2 Hardware Trigger

The external trigger is passed to the ADC8414 via designated pins see Appendices B, C and D.

6.4 Memory Update

All ADC channels are updated simultaneously and the memory pointer incremented. Therefore the memory pointer indicates what memory location has been reached by all the ADCs by adding the channel number to the pointer value with the channel number as the most significant bit.

E.g:- Channel 1 = xxxx Channel 2 = 1xxxx Channel 3 = 2xxxx etc.

With 2Mb operation it is necessary to include the half full flag to see whether the pointer is addressing lower or upper memory space.

E.g:- Channel 1 = xxxx Channel 2 = 1xxxx Channel 3 = 2xxxx when HF=0 for lower memory
Channel 1 = 8xxxx Channel 2 = 9xxxx Channel 3 = Axxxx when HF=1 for upper memory

7. Module Temperate Monitoring

The 8414 is fitted with a TC1047A which is a linear output temperature sensor whose output voltage is directly proportional to measured temperature. The TC1047A can accurately measure temperature from -40C to +125C. For the TC1047A, the output voltage range is typically 100mV at -40C, 500mV at 0C, 750mV at +25C, and 1.75V at +125C. A 10mV/°C voltage slope allows for the wide temperature range.

8. ID PROM

The word addresses are as below:-

Base+80	ASCII 'VI'	5649h	
Base+82	ASCII 'TA'	5441h	
Base+84	ASCII '4 '	3420h	
Base+86	Hytec ID high byte	0080h	
Base+88	Hytec ID low word	0300h	
Base+8A	Model number	8414h	
Base+8C	Revision	2201h	This shows PCB Iss 2 Xilinx V201
Base+8E	Reserved	0000h	
Base+90	Driver ID	0000h	
Base+92	Driver ID	0000h	
Base+94	Flags	0006h	This shows 8MHz and 32MHz operation
Base+96	No of bytes used	001Ah	
Base+98	Cal Type	0000h	0 = No software Calibration factors stored
Base+9A	Serial Number	xxxxdec	
Base+9C	Not used	0000h	
Base+9E	WLO	0000h	

9. SELECTION OF THE +/-12 VOLT POWER SUPPLY

The ADC 8414 +/-12 volt power supply can be derived either internally from the carrier card or from an external source via a transition card. The source is selected using jumpers J1, J2 and the GND AGND link where:

J1 External +12V connect 1 & 2, Internal +12V connect 2 & 3
J2 External -12V connect 1 & 2, Internal -12V connect 2 & 3

GND AGND Link
IN for internal +/-12V
OUT for external +/-12V (supplied from transition card DC DC converter).

IMPORTANT NOTE

The 8414 ADC should not be operated with only one of the 12Volt power rail connected as this may cause damage to the unit. This situation can be caused by incorrect setting of the jumpers J1 or J2 which set the source of the +/-12Volt supplies to the 8414 ADC card.

Power supply in balance will occur if:

1. **one of the jumpers is set to select the 12Volt from an isolated power supply which is not fitted and the other being set for internal 12Volt supply.**
2. **one of the jumpers is not fitted.**

10. EPICS Software Driver

EPICS and ASYN software drivers are in development for the ADC8414 16 channel ADC Industry Pack. For downloads go to:
www.hytec-electronics.co.uk/Download.aspx

APPENDIX A

PCB JUMPERS

Issue 1 PCB
J1 External +12V connect 1 & 2, Internal +12V connect 2 & 3
J2 External -12V connect 1 & 2, Internal -12V connect 2 & 3
J3 Not used.
J4 Not used.

LNK1 Factory set IN links VME GND and AGND **IMPORTANT DO NOT REMOVE**

APPENDIX B

I/O Connector – PL2 (50 way) on 8414 ADC Board

Pin	Signal	Pin	Signal
1	Input 1 +ve	26	Input 13 -ve
2	Input 1 -ve	27	Input 14 +ve
3	Input 2 +ve	28	Input 14 -ve
4	Input 2 -ve	29	Input 15 +ve
5	Input 3 +ve	30	Input 15 -ve
6	Input 3 -ve	31	Input 16 +ve
7	Input 4 +ve	32	Input 16 -ve
8	Input 4 -ve	33	N.C.
9	Input 5 +ve	34	AGND
10	Input 5 -ve	35	ExtTrig Pos
11	Input 6 +ve	36	ExtTrig Neg
12	Input 6 -ve	37	N.C.
13	Input 7 +ve	38	AGND
14	Input 7 -ve	39	XClk
15	Input 8 +ve	40	/XClk
16	Input 8 -ve	41	+12VX
17	Input 9 +ve	42	AGND
18	Input 9 -ve	43	+12VX
19	Input 10 +ve	44	AGND
20	Input 10 -ve	45	-12VX
21	Input 11 +ve	46	AGND
22	Input 11 -ve	47	-12VX
23	Input 12 +ve	48	AGND
24	Input 12 -ve	49	N.C.
25	Input 13 +ve	50	AGND

APPENDIX C

HYTEC TRANSITION CARD CONNECTIONS FOR THE ADC8414

I/O Connector – 50 way on transition
Pin Assignments

Pin	Signal	Pin	Signal
1	Chan 1 -	26	Chan 1 +
2	Chan 2 -	27	Chan 2 +
3	Chan 3 -	28	Chan 3 +
4	Chan 4 -	29	Chan 4 +
5	Chan 5 -	30	Chan 5 +
6	Chan 6 -	31	Chan 6 +
7	Chan 7 -	32	Chan 7 +
8	Chan 8 -	33	Chan 8 +
9	Chan 9 -	34	Chan 9 +
10	Chan 10 -	35	Chan 10 +
11	Chan 11 -	36	Chan 11 +
12	Chan 12 -	37	Chan 12 +
13	Chan 13 -	38	Chan 13 +
14	Chan 14 -	39	Chan 14 +
15	Chan 15 -	40	Chan 15 +
16	Chan 16 -	41	Chan 16 +
17		42	
18	ExtTrig Neg	43	ExtTrig Pos
19		44	
20	ExtCLK Neg	45	ExtCLK Pos
21	AGND	46	+12V *
22	AGND	47	+12V *
23	AGND	48	-12V *
24	AGND	49	-12V *
25	AGND	50	AGND

* Supplied when DC/DC converters to be fitted

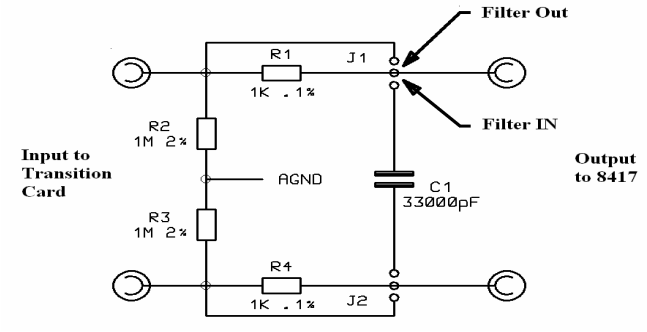
The Hytec TB8210/8211 Analogue I/O transition card

The Hytec TB8210/8211 is a single-width VME64X Transition Board which routes 64 channels of analogue I/O in 4 groups of 16 analogue channel pairs. Noise filters are provided for all 16 channels of each group which are jumper selectable on the 8210.

It has the option to fit on-board DC-DC converter for plant isolation.

This is the preferred card to use as it ties the inputs of the 8414 to AGND via 1Mohm resistors. It also has a low pass filter which can be switched in by jumpers (denoted by affixed label) on the card. The filter value should be determined before delivery. For the 8414 the C1 should be 1nF max to give 160KHz band width approx.

The 8211 does not have jumpers and it maybe supplied with out the capacitor C1 fitted but still ties the grounds.



8210 and 8211 signal conditioning card

Card 8308 and 8307

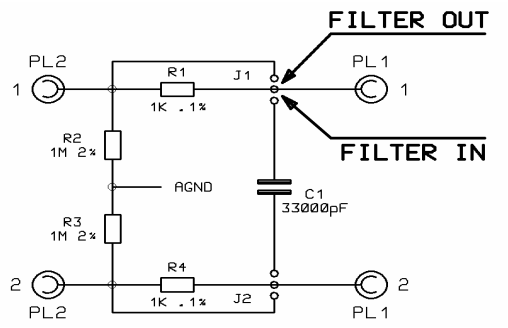
The 8308 allows for plug in signal card as used by the IOC to be plugged in to a single-width VME64X Transition Board.

The 8308 has four sites equating to IP positions A, B, C and D.

The 8307 has straight-through connections for 8002/4 carrier board sites A and B. Signal conditioning in-line with connections to sites C and D by means of plug-in signal conditioning board (SCBs).

There are two types of plug-in card that can be used:-

- 9304 straight through card. This can be used as the ADC8414 has its own active filter set to 100KHz. **NOTE** This card should be used with caution as the fully differential inputs of the 8414 may float if not correctly tied to AGND.
- 9202 signal conditioning card. This is the preferred card to use as it ties the inputs of the 8414 to AGND via 1Mohm resistors. It also has a low pass filter which can be switched in by jumpers (denoted by affixed label) on the card. The filter value should be determined before delivery. The filter should be set to give 170KHz (C1=1nF max) when used with the ADC8414 (denoted by affixed label). This card can be used to further reduce input noise especially sharp noise. When using this filter the overall bandwidth of the ADC8414 is reduced to approx 90KHz. The 9202 can also be setup to be a straight through card by setting the jumpers to link the filter out.



9202 signal conditioning card

The Hytec 8304 Straight-through transition card

Straight-through connections for 8002/4 carrier board sites A, B, C and D.

NOTE This card should be used with caution as the fully differential inputs of the 8414 may float if not correctly tied to AGND.

APPENDIX D

VME64X PIN ASSIGNMENT ON HYTEC 8002 IP CARRIER BOARD FOR ADC8414

ROW A	SIG	ROW B	SIG	ROW C	SIG	ROW D	SIG	ROW E	SIG	ROW F	SIG
P0.A01	D Chan 1+	P0.B01	D Chan 1-	P0.C01	D Chan 2+	P0.DO1	D Chan 2 -	P0.E01	D Chan 3+	P0.F01	GND
P0.A02	D Chan 3 -	P0.B02	D Chan 4+	P0.C02	D Chan 4 -	P0.D02	D Chan 5+	P0.E02	D Chan 5 -	P0.F02	GND
P0.A03	D Chan 6+	P0.B03	D Chan 6 -	P0.C03	D Chan 7+	P0.D03	D Chan 7 -	P0.E03	D Chan 8+	P0.F03	GND
P0.A04	D Chan 8 -	P0.B04	D Chan 9+	P0.C04	D Chan 9 -	P0.D04	D Chan 10 +	P0.E04	D Chan 10 -	P0.F04	GND
P0.A05	D Chan 11+	P0.B05	D Chan 11 -	P0.C05	D Chan 12 +	P0.D05	D Chan 12 -	P0.E05	D Chan 13 +	P0.F05	GND
P0.A06	D Chan 13 -	P0.B06	D Chan 14 +	P0.C06	D Chan 14 -	P0.D06	D Chan 15 +	P0.E06	D Chan 15 -	P0.F06	GND
P0.A07	D Chan 16+	P0.B07	D Chan 16 -	P0.C07	N/C	P0.D07	N/C	P0.E07	D XTrigger	P0.F07	GND
P0.A08	D/XTrigger	P0.B08	N/C	P0.C08	N/C	P0.D08	D XCLK	P0.E08	D /XCLK	P0.F08	GND
P0.A09	D +12V	P0.B09	D AGND	P0.C09	D +12V	P0.D09	D AGND	P0.E09	D -12V	P0.F09	GND
P0.A10	D AGND	P0.B10	D -12V	P0.C10	D AGND	P0.D10	N/C	P0.E10	D AGND	P0.F10	GND
P0.A11	C Chan 1+	P0 B11	C Chan 1 -	P0.C11	C Chan 2+	P0.D11	C Chan 2 -	P0 E11	C Chan 3+	P0.F11	GND
P0.A12	C Chan 3 -	P0.B12	C Chan 4+	P0.C12	C Chan 4 -	P0.D12	C Chan 5+	P0.E12	C Chan 5 -	P0.F12	GND
P0.A13	C Chan 6+	P0.B13	C Chan 6-	P0.C13	C Chan 7+	P0.D13	C Chan 7 -	P0.E13	C Chan 8+	P0.F13	GND
P0.A14	C Chan 8-	P0.B14	C Chan 9+	P0.C14	C Chan 9-	P0.D14	C Chan 10+	P0.E14	C Chan 11+	P0.F14	GND
P0.A15	C Chan 11+	P0.B15	C Chan 11-	P0.C15	C Chan 12+	P0.D15	C Chan 12-	P0.E15	C Chan 13+	P0.F15	GND
P0.A16	C Chan 13-	P0.B16	C Chan 14+	P0.C16	C Chan 14-	P0.D16	C Chan 15+	P0.E16	C Chan 15-	P0.F16	GND
P0.A17	C Chan 16+	P0.B17	C Chan 16-	P0.C17	N/C	P0.D17	N/C	P0.E17	C XTrigger	P0.F17	GND
P0.A18	C/XTrigger	P0.B18	N/C	P0.C18	N/C	P0.D18	C XCLK	P0.E18	C /XCLK	P0.F18	GND
P0.A19	C +12V	P0.B19	C AGND	P0.C19	C +12V	P0.D19	C AGND	P0.E19	C -12V	P0.F19	GND

P0 pin assignment

P1 ROW A	SIGNAL	P1 ROW B	SIGNAL	P1 ROW C	SIGNAL	P1 ROW D	SIGNAL	P1 ROW Z	SIGNAL
P1.A01	D00	P1.B01	N/C	P1.C01	D08	P1.D01	N/C	P1.Z01	N/C
P1.A02	D01	P1.B02	N/C	P1.C02	D09	P1.D02	N/C	P1.Z02	GND
P1.A03	D02	P1.B03	N/C	P1.C03	D10	P1.D03	N/C	P1.Z03	N/C
P1.A04	D03	P1.B04	BG0IN*	P1.C04	D11	P1.D04	N/C	P1.Z04	GND
P1.A05	D04	P1.B05	BG0OUT*	P1.C05	D12	P1.D05	N/C	P1.Z05	N/C
P1.A06	D05	P1.B06	BG1IN*	P1.C06	D13	P1.D06	N/C	P1.Z06	GND
P1.A07	D06	P1.B07	BG1OUT*	P1.C07	D14	P1.D07	N/C	P1.Z07	N/C
P1.A08	D07	P1.B08	BG2IN*	P1.C08	D15	P1.D08	N/C	P1.Z08	GND
P1.A09	GND	P1.B09	BG2OUT*	P1.C09	GND	P1.D09	N/C	P1.Z09	N/C
P1.A10	N/C	P1.B10	BG3IN*	P1.C10	N/C	P1.D10	N/C	P1.Z10	GND
P1.A11	GND	P1.B11	BG3OUT*	P1.C11	BERR*	P1.D11	N/C	P1.Z11	N/C
P1.A12	DS1*	P1.B12	N/C	P1.C12	RESET	P1.D12	+3.3V	P1.Z12	GND
P1.A13	DS0*	P1.B13	N/C	P1.C13	LWORD*	P1.D13	N/C	P1.Z13	N/C
P1.A14	WRITE	P1.B14	N/C	P1.C14	AM5	P1.D14	+3.3V	P1.Z14	GND
P1.A15	GND	P1.B15	N/C	P1.C15	A23	P1.D15	N/C	P1.Z15	N/C
P1.A16	DTACK*	P1.B16	AM0	P1.C16	A22	P1.D16	+3.3V	P1.Z16	GND
P1.A17	GND	P1.B17	AM1	P1.C17	A21	P1.D17	N/C	P1.Z17	N/C
P1.A18	AS	P1.B18	AM2	P1.C18	A20	P1.D18	+3.3V	P1.Z18	GND
P1.A19	GND	P1.B19	AM3	P1.C19	A19	P1.D19	N/C	P1.Z19	N/C
P1.A20	IACK	P1.B20	GND	P1.C20	A18	P1.D20	+3.3V	P1.Z20	GND
P1.A21	IACKIN*	P1.B21	N/C	P1.C21	A17	P1.D21	N/C	P1.Z21	N/C
P1.A22	IACKOUT	P1.B22	N/C	P1.C22	A16	P1.D22	+3.3V	P1.Z22	GND
P1.A23	AM4	P1.B23	GND	P1.C23	A15	P1.D23	N/C	P1.Z23	N/C
P1.A24	A07	P1.B24	IRQ7*	P1.C24	A14	P1.D24	+3.3V	P1.Z24	GND
P1.A25	A06	P1.B25	IRQ6*	P1.C25	A13	P1.D25	N/C	P1.Z25	N/C
P1.A26	A05	P1.B26	IRQ5*	P1.C26	A12	P1.D26	+3.3V	P1.Z26	GND
P1.A27	A04	P1.B27	IRQ4*	P1.C27	A11	P1.D27	N/C	P1.Z27	N/C
P1.A28	A03	P1.B28	IRQ3*	P1.C28	A10	P1.D28	+3.3V	P1.Z28	GND
P1.A29	A02	P1.B29	IRQ2*	P1.C29	A09	P1.D29	N/C	P1.Z29	N/C
P1.A30	A0l	P1.B30	IRQ1*	P1.C30	A08	P1.D30	+3.3V	P1.Z30	GND
P1.A31	-12V	P1.B31	N/C	P1.C31	+12V	P1.D31	N/C	P1.Z31	N/C
P1.A32	+5V	P1.B32	+5V	P1.C32	+5V	P1.D32	+5V	P1.Z32	GND

P1 Pin Assignment

ROWA	SIG	ROWB	SIG	ROWC	SIG	ROWD	SIG	ROWZ	SIG
P2.A01	B +12V	P2.B01	+5V	P2.C01	B AGND	P2.D01	C -12V	P2.Z01	C AGND
P2.A02	B +12V	P2.B02	GND	P2.C02	B AGND	P2.D02	C AGND	P2.Z02	GND
P2.A03	B -12V	P2.B03	N/C	P2.C03	B AGND	P2.D03	C AGND	P2.Z03	N/C
P2.A04	B -12V	P2.B04	A24	P2.C04	B AGND	P2.D04	B Chan 1 +	P2.Z04	GND
P2.A05	N/C	P2.B05	A25	P2.C05	B AGND	P2.D05	B Chan 2 +	P2.Z05	B Chan 1 -
P2.A06	A Chan 1 +	P2.B06	A26	P2.C06	A Chan 1 -	P2.D06	B Chan 2 -	P2.Z06	GND
P2.A07	A Chan 2 +	P2.B07	A27	P2.C07	A Chan 2 -	P2.D07	B Chan 3 -	P2.Z07	B Chan 3 +
P2.A08	A Chan 3 +	P2.B08	A28	P2.C08	A Chan 3 -	P2.D08	B Chan 4 +	P2.Z08	GND
P2.A09	A Chan 4 +	P2.B09	A29	P2.C09	A Chan 4 -	P2.D09	B Chan 5 +	P2.Z09	B Chan 4 -
P2.A10	A Chan 5 +	P2.B10	A30	P2.C10	A Chan 5 -	P2.D10	B Chan 5 -	P2.Z10	GND
P2.A11	A Chan 6 +	P2.B11	A31	P2.C11	A Chan 6 -	P2.D11	B Chan 6 -	P2.Z11	B Chan 6 +
P2.A12	A Chan 7 +	P2.B12	GND	P2.C12	A Chan 7 -	P2.D12	B Chan 7 +	P2.Z12	GND
P2.A13	A Chan 8 +	P2.B13	+5V	P2.C13	A Chan 8 -	P2.D13	B Chan 8 +	P2.Z13	B Chan 7 -
P2.A14	A Chan 9 +	P2.B14	N/C	P2.C14	A Chan 9 -	P2.D14	B Chan 8 -	P2.Z14	GND
P2.A15	A Chan 10 +	P2.B15	N/C	P2.C15	A Chan 10 -	P2.D15	B Chan 9 -	P2.Z15	B Chan 9 +
P2.A16	A Chan 11 +	P2.B16	N/C	P2.C16	A Chan 11 -	P2.D16	B Chan 10 +	P2.Z16	GND
P2.A17	A Chan 12 +	P2.B17	N/C	P2.C17	A Chan 12 -	P2.D17	B Chan 11 +	P2.Z17	B Chan 10 -
P2.A18	A Chan 13 +	P2.B18	N/C	P2.C18	A Chan 13 -	P2.D18	B Chan 11 -	P2.Z18	GND
P2.A19	A Chan 14 +	P2.B19	N/C	P2.C19	A Chan 14 -	P2.D19	B Chan 12 -	P2.Z19	B Chan 12+
P2.A20	A Chan 15 +	P2.B20	N/C	P2.C20	A Chan 15 -	P2.D20	B Chan 13 +	P2.Z20	GND
P2.A21	A Chan 16 +	P2.B21	N/C	P2.C21	A Chan 16 -	P2.D21	B Chan 14 +	P2.Z21	B Chan 13 -
P2.A22	N/C	P2.B22	GND	P2.C22	N/C	P2.D22	B Chan 14 -	P2.Z22	GND
P2.A23	A X Trigger	P2.B23	N/C	P2.C23	A /XTrigger	P2.D23	B Chan 15 -	P2.Z23	B Chan 15+
P2.A24	N/C	P2.B24	N/C	P2.C24	N/C	P2.D24	B Chan 16 +	P2.Z24	GND
P2.A25	A XCLK	P2.B25	N/C	P2.C25	A /XCLK	P2.D25	N/C	P2.Z25	B Chan 16 -
P2.A26	A +12V	P2.B26	N/C	P2.C26	A AGND	P2.D26	N/C	P2.Z26	GND
P2.A27	A +12V	P2.B27	N/C	P2.C27	A AGND	P2.D27	B /XTrigger	P2.Z27	B X Trigger
P2.A28	A -12V	P2.B28	N/C	P2.C28	A AGND	P2.D28	N/C	P2.Z28	GND
P2.A29	A -12V	P2.B29	N/C	P2.C29	A AGND	P2.D29	B XCLK	P2.Z29	N/C
P2.A30	N/C	P2.B30	N/C	P2.C30	A AGND	P2.D30	B /XCLK	P2.Z30	GND
P2.A31	Out+3.3V	P2.B31	GND	P2.C31	Out+3.3V	P2.D31	GND	P2.Z31	Out +3.3V
P2.A32	Out +5V	P2.B32	+5V	P2.C32	Out +5V	P2.D32	PC +5V	P2.Z32	GND

P2 pin assignment

Denotes pins with thickened tracks which can be used for power inputs