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ADC8417 8-CHANNEL 24-BIT ADC INDUSTRY PACK

USERS MANUAL

PCB Issue 3
FPGA Version 8417V302
8MHz or 32MHZ IP Clock

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/12/10	0.1	Preliminary
21/02/11	1.0	Initial release.
06/05/11	2.0	Change data storage format to same as DAC8415 (see CN310).
06/07/11	2.3	Endian bit in the CSR Ext so user can switch between Big and Little Endian for ADC data in memory and ADC data registers.
20/10/11	3.0	The unit has been redesigned as an 8 channel unit to reduce power consumption.
14/12/11	3.1	Product specifications updated and memory data table corrected for 8 channels.
16/12/11	3.2	Two extra registers added to allow full address counter to be read and the NOC register to be written in full.
19/04/12	3.3	The manual highlights the preferred type of Transition card to use and the need to use proper grounding techniques.

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CONTENTS

1. INTRODUCTION	4
2. PRODUCT SPECIFICATIONS	5
3. OPERATING MODES	6
3.1 REGISTER MODE	6
3.2 TRIGGERED SAMPLING.....	6
4. MEMORY MAP	7
5. APPLICATION REGISTERS	9
5.1 CONTROL & STATUS REGISTER (CSR).....	9
5.2 CONTROL	9
5.3 CONVERSION POINTER	10
5.4 NUMBER OF CONVERSIONS.....	10
5.5 ADC SAMPLE RATE.....	10
5.6 INTERRUPT VECTOR	10
5.7 EXTENDED CONTROL & STATUS REGISTER (CSR EXT).....	11
5.8 ADC REGISTERS.....	12
6. ADC OPERATION	13
6.1 MEMORY UPDATE INHIBIT AND INTERRUPT.....	13
6.2 SET NUMBER OF CONVERSIONS	13
6.3 TRIGGERING.....	13
6.3.1 <i>Software Trigger</i>	13
6.3.2 <i>Hardware Trigger</i>	13
6.4 MEMORY UPDATE	13
7. ID PROM	14
8. SELECTION OF THE +/-12 VOLT POWER SUPPLY	14
IMPORTANT NOTE	14
9. EPICS SOFTWARE DRIVER	14
APPENDIX A	15
APPENDIX B	16
APPENDIX C	17
APPENDIX D	19

1. INTRODUCTION

The Hytec IP-SSA-8417 is an Industry Pack that provides 8 channels of simultaneously sampled analogue digitisation with the following characteristics:-

- 8 simultaneously sampled channels.
- 8401 register superset and connector pin layout.
- 24-bit ADCs used on-board
- Programmable 16bits/24 bits resolution
- Programmable bi-polar full-scale resolution all inputs +/-10V or +/-5V bi-polar.
- Conversion method: Delta-sigma
- On-board calibration by FPGA firmware using stored offset and gain parameters.
- 16bits accuracy +/-10V on board calibration.
- 16bits accuracy +/-5V on board calibration.
- True full differential inputs.
- Input impedance - 10Mohms differential,
- CMRR - 100dB at +/-5V wrt plant CMV
- DC +/-25V overload for 1ms.
- On board RAM Memory up to 1M x 16 bits (128K samples per channel in 16 bit mode and 64K samples per channel in 24 bit mode.
- Offset drift: 4uV/degC typical
- Gain drift 2ppm/degC typical
- Up to 100kSPS sampling rate from an external clock
- Internal update clock rates programmable (100KHz,50KHz,20KHz,10KHz,5KHz,2KHz,1KHz,500Hz,200Hz,100Hz,50Hz,20Hz,10Hz,5Hz,2Hz and 1Hz)
- On-board sample clock: programmable to 100kHz
- ADC Noise 20uV rms
- Bandwidth 70kHz@100kSPS
- System to plant isolation to 100V when externally powered by DC/DC converter option.
- Ext sample clock up to 100kHz isolated input
- Ext trigger isolated input
- Two buffered reference voltage outputs for excitation.
- 8/32MHz IP system clock operation.
- Field upgradeable firmware (requires Xilinx/compatible device to program built in FPGA flash memory via the FPGA JTAG port).
- EPICS and ASYN driver support.

IMPORTANT NOTE

Please select the correct transition card or ensure that the input signals to the 8417 are correct grounded between the 8417 and source. This is to ensure that the inputs of the 8417 and the source are tied together and are not allowed to float.

2. PRODUCT SPECIFICATIONS

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of channels:	8
ADC resolution:	24 bits
Diff. Non-linearity:	+/-0.75 LSB TYP
Int. Non-linearity:	+/-1.5 LSB TYP
Offset error:	+/-10V offset error - +/-610uV with firmware calibration @ 25 deg C (+/- 2mV typical without calibration). +/-5V offset error - +/-305uV after firmware calibration @ 25 deg C (+/- 2mV typical without calibration).
Offset drift:	10uV/degC typical
Gain error:	+/-10V gain error - +/-610uV after firmware calibration @ 25 deg C (+/- 0.2% FS typical without calibration). +/-5V gain error - +/-305uV after firmware calibration @ 25 deg C (+/- 0.2% FS typical without calibration).
Gain drift:	5ppm/degC typical
Range:	+/-10V or +/-5V full scale (+ve input referred to -ve input)
Overvoltage:	+/-25V peak for 1ms and 20VDC
Bandwidth (-3dB):	170KHz
Throughput:	100KHz
ADC device:	TI ADS1274
Data format:	24 bits straight binary
SNR:	ADC Signal-to-Noise 110dB (typ)
Isolation:	System to plant isolation to 100V when externally powered by DC/DC converter option.
Memory:	1M x 16 bits .
Power:	+5V @ 50mA typical +12V @ 315mA typical when switched to internal -12V @ 110mA typical when switched to internal

The 8417 Module Response Time

At the point where the module is writing ADC data to memory during sampling and an IP memory read/write occurs the number of wait states introduced will vary.

In this case the module is guaranteed to respond with Ack* within 3.5us.

3. Operating Modes

3.1 Register mode

This mode is enabled by setting ARM = '0' (bit 15 of the CSR) and ET='0' (bit 14 of the CSR).

As soon as the ARM bit is set (no trigger required) the ADCs sample at the sample rate which is derived either from the internal clock whose rate is set by the Internal Sample Rate register or by the external sample clock supplied by the user via the rear transition card see .

The ADC data registers are updated at the conversion rate. These registers can be read in any order at any time.

The memory is also updated at the sample rate and is continuously updated rapping round on reaching the end of the memory until the ARM bit is cleared.

There are sixteen ADC buffer registers (addresses 10hex – 28hex) which store the last sampled conversions and may be read at any time.

3.2 Triggered sampling

This mode is enabled by setting ARM = '0' (bit 15 of the CSR) and ET='1' (bit 14 of the CSR). Then when a software or hardware trigger is detected conversions are stored in the RAM memory at the sample rate set.

The sample rate is derived either from the internal clock whose rate is set by the Internal Clock Rate register or by the external clock supplied by the user.

The value written to the memory pointer register gives the starting point in memory that the conversions are stored to.

The point at which conversions are stopped is set by the Number of Counts register.

The address the unit stops at is given by the Memory Conversion pointer register.

This mode also updates the ADC Data registers at the conversion rate. These registers can be read in any order at any time.

4. Memory Map

A bit in the control register of the 8417 allows selection of either 1Mb memory (16K samples/channel 24 bit) when set at logic 1 or 2Mb (32K samples/channel 24 bit) when set at logic 0.

24 Bit Mode

When set to 24 bit mode with 2Mb memory size the memory is split up in to two halves giving an upper and lower conversion memory.

These areas are further divided into sixteen segments allocated to conversions from ADC1 to ADC16 as shown in the table below.

When the lower buffer has been filled the Half Full Flag status is set and when the upper memory is full the Full Flag status is set.

24 bit Data in memory Little endian (Endian bit in CSR Ext='0')

Lower Conversion Memory ADC	Upper Conversion Memory ADC
ADC8 conversions	ADC8 conversions
ADC7 conversions	ADC7 conversions
ADC6 conversions	ADC6 conversions
ADC3 conversions	ADC3 conversions
ADC2 conversions	ADC2 conversions
ADC1 conversion 32k (bits 23-16)	ADC1 conversion 64k (bits 23-16)
ADC1 conversion 32k (bits 15-0)	ADC1 conversion 64k (bits 15-0)
ADC1 conversion 32k-1 (bits 23-16)	ADC1 conversion 64k-1 (bits 23-16)
ADC1 conversion 32k-1 (bits 15-0)	ADC1 conversion 64k-1 (bits 15-0)
ADC1 conversion 1 (bits 23-16)	ADC1 conversion 32k+1 (bits 23-16)
ADC1 conversion 1 (bits 15-0)	ADC1 conversion 32k+1 (bits 15-0)

24 bit Data in memory Big endian (Endian bit in CSR Ext='1')

Lower Conversion Memory ADC	Upper Conversion Memory ADC
ADC8 conversions	ADC8 conversions
ADC7 conversions	ADC7 conversions
ADC6 conversions	ADC6 conversions
ADC3 conversions	ADC3 conversions
ADC2 conversions	ADC2 conversions
ADC1 conversion 32k (bits 15-0)	ADC1 conversion 64k (bits 15-0)
ADC1 conversion 32k (bits 23-16)	ADC1 conversion 64k (bits 23-16)
ADC1 conversion 32k-1 (bits 15-0)	ADC1 conversion 64k-1 (bits 15-0)
ADC1 conversion 32k-1 (bits 23-16)	ADC1 conversion 64k-1 (bits 23-16)
ADC1 conversion 1 (bits 15-0)	ADC1 conversion 32k+1 (bits 15-0)
ADC1 conversion 1 (bits 23-16)	ADC1 conversion 32k+1 (bits 23-16)

16 Bit Mode

When set to 16 bit mode with 2Mb memory size the memory is split up in to two halves giving an upper and lower conversion memory.

These areas are further divided into eight segments allocated to conversions from ADC1 to ADC8 as shown in the table below.

When the lower buffer has been filled the Half Full Flag status is set and when the upper memory is full the Full Flag status is set.

Lower Conversion Memory	Upper Conversion Memory
ADC8 conversions	ADC8 conversions
ADC7 conversions	ADC7 conversions
ADC6 conversions	ADC6 conversions
ADC3 conversions	ADC3 conversions
ADC2 conversions	ADC2 conversions
ADC1 conversion 64k (bits 15-0) ADC1 conversion 64k-1 (bits 15-0)	ADC1 conversion 128k (bits 15-0) ADC1 conversion 128k-1 (bits 15-0)
ADC1 conversion 2 (bits 15-0) ADC1 conversion 1 (bits 15-0)	ADC1 conversion 64k+2 (bits 15-0) ADC1 conversion 64k+1 (bits 15-0)

5. Application Registers

There are eight application specific (I/O) registers and consists of the following the:

- CSR,
- number of samples per trigger (NCO),
- memory conversion pointer,
- clock rate,
- interrupt vector value
- Extended CSR.

There are also 16 ADC buffer registers.

5.1 Control & Status Register (CSR)

5.2 Control

Write Address: 0hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ARM	EX	ST	XC	ET	EE	FE	HE	1M	DA	EII	MII	x	CC	F	HF

Status

Read Address: 0hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ARM	EX	ST	XC	ET	EE	FE	HE	1M	DA	EII	MII	MIS	CC	F	HF

- ARM** Arm the ADCs. Allow conversions either continuous or triggered.
- EX** Enable trigger. If not set continuously sample at the clock rate. If set allows external trigger or software trigger
- ST** Software trigger. Triggers a programmed number of samples. ST is cleared on completion.
- XC** Enable the external clock. If 0 the internal clock is used for the sample rate. If set true the external clock is used for the sample clock without frequency division.
- ET** When logic '0' disable hardware memory inhibit input. When logic '1' enable hardware memory inhibit from IP **Strobe*** line (*on Hytec 800x IP carrier card, this signal is driven from the front panel INHIBIT lemo*).
- EE** Enables interrupt at end of sampling sequence.
- FE** Enables interrupt when the upper conversion memory has been filled. (Memory Full).
- HE** Enables interrupt when the lower conversion memory has been filled. (Memory Half Full).
- 1M** Enables 1Mb memory (64K samples/channel) when logic 1 and 2Mb (128K samples/channel) when logic 0.
- DA** Set to 1 allows the unit to disarm on completion of memory acquisition
- EII** This enables an interrupt to be generated when ever the memory inhibit bit (MIS) is set.
- MII** **(Write)** When set to logic '1' hardware memory inhibit interrupt is cleared but not disabled. **(Read)** Shows that an interrupt has been generated from hardware memory inhibit.
- MIS** **(Read Only)** this bit indicates that the hardware memory inhibited on the IP **Strobe*** line is asserted when at logic '1' (*driven from the front panel INHIBIT lemo on Hytec 800x IP carriers*).
- CC** Conversions complete. Status bit set when the number of programmed samples has been completed. Generates IRQ0* if set and EE is set to a logic 1.
- F** Full status. Set when the upper conversion memory has been filled. Generates IRQ0* if set and FE is set to a logic 1. To clear this flag write a '0' to this bit.
- HF** Half full status. Set when the lower conversion memory has been filled. Generates IRQ0* if set and HE is set to a logic 1. To clear this flag write a '0' to this bit.

5.3 Conversion Pointer LSW

Read/write Address: 2hex

The current conversion address is given by the conversion address offset by the ADC number. This register **can not be** written too when the unit is ARMED.

When in 24bit mode the address counter is incremented by 2.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

5.4 Number of conversions LSW

Read/write Address: 4hex

The number of conversions register allows the number of samples per trigger to be programmed.

If a number of triggers occur and the memory buffer size per channel is exceeded the conversions will wrap around from the upper memory to the base of the lower memory.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

5.5 ADC Sample Rate

Read/write Address: 6hex

The first five bits in the sample rate register are used to enable codes 0 – 16 to enable frequencies of 1 Hz to 100kHz in multiples of 1,2,5 or 10. (E.g. 0=1Hz, 1=2Hz, 2=5Hz, 3=10Hz and so on to 15=100KHz) Each clock pulse will initiate simultaneous ADC conversions and store them in memory.

If the external sample clock exceeds 50KHz the unit must be put in to High Speed Mode by selecting the Internal 100KHz sample rate.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	S3	S2	S1	S0

5.6 Interrupt Vector

Read/write Address: 8hex

The vector register is a 16 bit register which stores the interrupt vector value.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

5.7 Extended Control & Status Register (CSR Ext)

Read/write Address: Ahex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
EN16	CAL		Endian		E	EFW	IFW	HS	R			ISE	IS	SMI	TEN

- TEN** This shows the trigger status of the unit (Read only).
- SMI** This sets **Software Memory Inhibit** when at logic '1'. This does not generate an interrupt or set the MIS in the CSR.
- IS** ADC Register update status. Set high when the ADC Registers have been updated. Generates IRQ0* if set and ISE is set to a logic 1. To clear IS write '1' this also clears the IRQ.
- ISE** Enables interrupt when ADC Registers have been updated as indicated by **IS**.
- R** Set ADC range set to 0 = +/-10V and range set to 1 = +/-5V.
- HS** Indicates ADC in High Speed Mode when running at greater then 50KHz sample rate when using internal clock. When using external sample clock need to set this by setting the internal clock speed to 100kHz in the ADC Sample rate register.
- IFW** **Do not set this bit as setup and calibration data maybe lost.** This bit enables the FPGA flash write from buffer command
- EFW** **Do not set this bit as setup and calibration data maybe lost.** This bit enables the External flash write by writing to IP mem i.e. switches off RAM
- E** **Do not set this bit as setup and calibration data maybe lost.** This bit enables the External flash chip or sector erase when do a IP write to mem. If IP data is 0x10 then chip erase (64s time taken) if IP data is 0x30 then sector erase where the sector address is given in the IP memory address lines. If chip erase then IP mem address = 0x555 and data 0x10.
- Endian** '0'=Little Endian '1'= Big and Little for ADC data in memory and data ADC registers in 24 bit acquisition mode only.
- CAL** If set to '1' unit does not use on board flash calibration *for register updates only*. If EX=1 then this has no effect. Used for production test.
- EN16** Enable 16 bit mode when set to logic 1.

5.8 Conversion Pointer MSW

Read/write Address: Chex

This is the top two bits of the current conversion address is given by the conversion address offset by the ADC number. This register **can be** written too when the unit is ARMed.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	C17	C16

5.9 Number of conversions MSW

Read/write Address: Ehex

The number of conversions register allows the number of samples per trigger to be programmed.

If a number of triggers occur and the memory buffer size per channel is exceeded the conversions will wrap around from the upper memory to the base of the lower memory.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	N17	N16

5.10 ADC Registers

Read only Address: 10hex – 28hex

The sixteen ADC buffer registers store the last sample conversions and may be read at any time.

Data format 000F00h = -10v, 800000h = 0V and FFF100h = +10V.

Data format 000F00h = -5v, 800000h = 0V and FFF100h = +5V.

16 bit mode (as 8401) this uses address 10hex to 18hex (Word 8hex – Fhex) for channels 1 to 8.

The eight ADC buffer registers store the last sample conversions and may be read at any time.

Data format 000F00h = -10v, 800000h = 0V and FFF100h = +10V.

Data format 000F00h = -5v, 800000h = 0V and FFF100h = +5V.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C23	C22	C21	C20	C19	C18	C17	C16	C15	C14	C13	C12	C11	C10	C9	C8

In 16 bit acquisition mode the 'Endian' bit in the CSR Ext has no effect.

24 bit mode this uses address 10hex to 28hex (Word 8hex – 17hex)

The sixteen ADC buffer registers store the last sample conversions and may be read at any time.

Data format 000F00h = -10v, 800000h = 0V and FFF100h = +10V.

Data format 000F00h = -5v, 800000h = 0V and FFF100h = +5V.

Little endian (Endian bit in CSR Ext='0')

i.e. channel 1 address of low word is 10hex (Word 8hex)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

channel 1 address of high word is 12hex (Word 9hex)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	C23	C22	C21	C20	C19	C18	C17	C16

Big endian (Endian bit in CSR Ext='1')

i.e. channel 1 address of low word is 10hex (Word 8hex)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	C23	C22	C21	C20	C19	C18	C17	C16

channel 1 address of high word is 12hex (Word 9hex)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

6. ADC OPERATION

6.1 Memory Update Inhibit and Interrupt

The updating of the conversion memory can be stopped by controlling the external IP **Strobe*** line (*on the Hytec 8002 or 8004 IP carrier card, this signal is driven from the front panel INHIBIT lemo*).

When the STROBE line is taken low and the enable hardware memory inhibit bit (ET) is set in CSR the updating of the conversion memory is stopped. This is indicated by the MIS bit in the CSR going high.

On memory update inhibit an interrupt can be generated if the **Enable Memory Inhibit Interrupt** enable bit (EII) is set in the CSR. The **Memory Inhibit Interrupt** (MII) bit of the CSR flags an interrupt. This is cleared by either clearing the EII in the CSR or by writing a '1' to MII bit in the CSR which clears the Memory Inhibit Interrupt without the need to clear the EII in the CSR.

The IP **Strobe*** line needs to be taken high then low after interrupt cleared to generate a new interrupt.

6.2 Set Number of Conversions

The 'EX' bit in the CSR must be set, if not then the NOC is ignored and the CC flag will not be set.

The number of conversions register (NOC) at address 2hex allows the number of samples per trigger to be programmed. The maximum number of conversions is 32K of samples 1MB and 64K of samples for 2MB for each channel before the Conversion Complete (CC) flag is set in the CSR. An interrupt is generated if the **Enable Interrupt on Last Sample** (EE) bit is set in the CSR. To clear the interrupt write a '0' to the CC bit of the CSR.

If a number of triggers occur and the memory buffer size of 64K of conversions per channel is exceeded the conversions will wrap around from the upper memory to the base of the lower memory.

6.3 Triggering

The triggering of the ADC8417 is only used when the number of conversions has been set in the Number of Conversions register and the **Enable Trigger** (EX) bit has been set in the CSR.

6.3.1 Software Trigger

The unit can be triggered by a software trigger by writing a '1' to the **Software Trigger** (ST) bit of the CSR.

6.3.2 Hardware Trigger

The external trigger is passed to the ADC8417 via designated pins see Appendices B, C and D.

6.4 Memory Update

All ADC channels are updated simultaneously and the memory pointer incremented. Therefore the memory pointer indicates what memory location has been reached by all the ADCs by adding the channel number to the pointer value with the channel number as the most significant bit.

E.g:- Channel 1 = xxxx Channel 2 = 1xxxx Channel 3 = 2xxxx etc.

With 2Mb operation it is necessary to include the half full flag to see whether the pointer is addressing lower or upper memory space.

E.g:- Channel 1 = xxxx Channel 2 = 1xxxx Channel 3 = 2xxxx when HF=0 for lower memory
Channel 1 = 8xxxx Channel 2 = 9xxxx Channel 3 = Axxxx when HF=1 for upper memory

7. ID PROM

The word addresses are as below:-

Base+80	ASCII 'VI'	5649h	
Base+82	ASCII 'TA'	5441h	
Base+84	ASCII '4 '	3420h	
Base+86	Hytec ID high byte	0080h	
Base+88	Hytec ID low word	0300h	
Base+8A	Model number	8417h	
Base+8C	Revision	3302h	This shows PCB Iss 3 FPGA at Version 302
Base+8E	Reserved	0000h	
Base+90	Driver ID	0000h	
Base+92	Driver ID	0000h	
Base+94	Flags	0006h	This shows 8MHz and 32MHz operation
Base+96	No of bytes used	001Ah	
Base+98	Cal Type	0000h	0 = No software Calibration factors stored
Base+9A	Serial Number	xxxxdec	
Base+9C	Not used	0000h	
Base+9E	WLO	0000h	

8. SELECTION OF THE +/-12 VOLT POWER SUPPLY

The ADC 8417 +/-12 volt power supply can be derived either internally from the carrier card or from an external source via a transition card . The source is selected using jumpers J1, J2 and the GND AGND link where:

J1 External +12V connect 1 & 2, Internal +12V connect 2 & 3

J2 External -12V connect 1 & 2, Internal -12V connect 2 & 3

GND AGND Link

IN for internal +/-12V

OUT for external +/-12V (supplied from transition card DC DC converter this must be able to supply).

IMPORTANT NOTE

The 8417 ADC should not be operated with only one of the 12Volt power rail connected as this may cause damage to the unit. This situation can be caused by incorrect setting of the jumpers J1 or J2 which set the source of the +/-12Volt supplies to the 8417 ADC card.

Power supply in balance will occur if:

1. one of the jumpers is set to select the 12Volt from an isolated power supply which is not fitted and the other being set for internal 12Volt supply.
2. one of the jumpers is not fitted.

9. EPICS Software Driver

EPICS and ASYN software drivers are in development for the ADC8417 8 channel 24 bit ADC Industry Pack.

For downloads go to: www.hytec-electronics.co.uk/Download.aspx

APPENDIX A

PCB JUMPERS

Issue 1 PCB

J1 External +12V connect 1 & 2, Internal +12V connect 2 & 3

J2 External -12V connect 1 & 2, Internal -12V connect 2 & 3

J3, J4 and J5 Not used.

J6 Selects +2.5V or +5V output to transition card

J7 Selects -2.5V or -5V output to transition card

LNK1 Factory set IN links VME GND and AGND.

APPENDIX B

I/O Connector – PL2 (50 way) on 8417 ADC Board

Pin	Signal	Pin	Signal
1	Input 1 +ve	26	
2	Input 1 -ve	27	
3	Input 2 +ve	28	
4	Input 2 -ve	29	
5	Input 3 +ve	30	
6	Input 3 -ve	31	
7	Input 4 +ve	32	
8	Input 4 -ve	33	+2.5V or +5V (J6)
9	Input 5 +ve	34	-2.5V or -5V (J7)
10	Input 5 -ve	35	ExtTrig Pos
11	Input 6 +ve	36	ExtTrig Neg
12	Input 6 -ve	37	N.C.
13	Input 7 +ve	38	N.C.
14	Input 7 -ve	39	XClk
15	Input 8 +ve	40	/XClk
16	Input 8 -ve	41	+12VX Input
17		42	AGND
18		43	+12VX Input
19		44	AGND
20		45	-12VX Input
21		46	AGND
22		47	-12VX Input
23		48	AGND
24		49	N.C.
25		50	AGND

APPENDIX C

HYTEC TRANSITION CARD CONNECTIONS FOR THE ADC8417

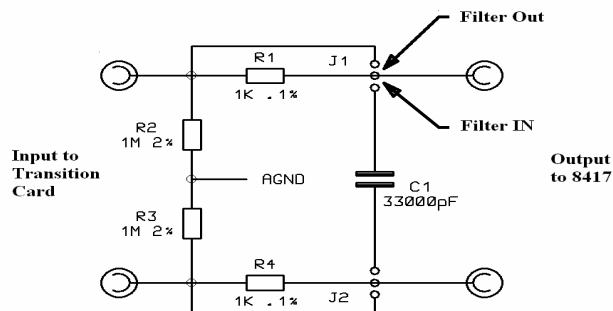
I/O Connector – 50 way on transition

Pin	Signal	Pin	Signal
1	Chan 1 -	26	Chan 1 +
2	Chan 2 -	27	Chan 2 +
3	Chan 3 -	28	Chan 3 +
4	Chan 4 -	29	Chan 4 +
5	Chan 5 -	30	Chan 5 +
6	Chan 6 -	31	Chan 6 +
7	Chan 7 -	32	Chan 7 +
8	Chan 8 -	33	Chan 8 +
9		34	
10		35	
11		36	
12		37	
13		38	
14		39	
15		40	
16		41	
17	-2.5 or -5V (J7)	42	2.5 or 5V (J6)
18	ExtTrig Neg	43	ExtTrig Pos
19		44	
20	ExtCLK Neg	45	ExtCLK Pos
21	AGND	46	
22	AGND	47	
23	AGND	48	
24	AGND	49	
25	AGND	50	

Card 8201 (32 differential Signals) and 8211 (64 differential Signals)

Filtered inputs (check correct filter values) for 32/64 differential analogue signals plus external clock and trigger inputs. It has the option to fit on-board DC-DC converter.

This is the preferred card to use as it ties the inputs of the 8417 to AGND via 1Mohm resistors. It also has a low pass filter which can be switched in by jumpers (denoted by affixed label) on the card. The filter value should be determined before delivery.



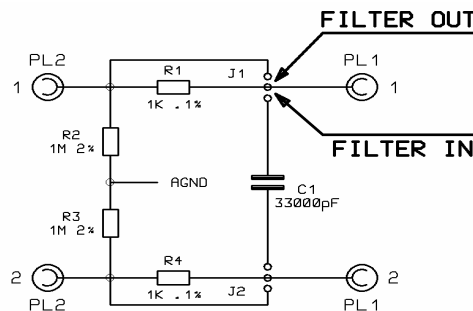
8201 and 8211 signal conditioning card

Card 8307

Straight-through connections for 8002/4 carrier board sites A and B. Signal conditioning in-line with connections to sites C and D by means of plug-in signal conditioning board (SCBs).

There are two types of plug-in card that can be used:-

- 9304 straight through card.
NOTE This card should be used with caution as the fully differential inputs of the 8417 may float if not correctly tied to AGND.
- 9202 signal conditioning card. This is the preferred card to use as it ties the inputs of the 8417 to AGND via 1Mohm resistors. It also has a low pass filter which can be switched in by jumpers (denoted by affixed label) on the card. The filter value should be determined before delivery.



9202 signal conditioning card

The Hytec 8304 Straight-through transition card

Straight-through connections for 8002/4 carrier board sites A, B, C and D.

NOTE This card should be used with caution as the fully differential inputs of the 8417 may float if not correctly tied to AGND.

APPENDIX D
VME64X PIN ASSIGNMENT ON HYTEC 8002 IP CARRIER BOARD FOR ADC8417

ROW A	SIG	ROW B	SIG	ROW C	SIG	ROW D	SIG	ROW E	SIG	ROW F	SIG
P0.A01	D Chan 1+	P0.B01	D Chan 1-	P0.C01	D Chan 2+	P0.D01	D Chan 2 -	P0.E01	D Chan 3+	P0.F01	GND
P0.A02	D Chan 3 -	P0.B02	D Chan 4+	P0.C02	D Chan 4 -	P0.D02	D Chan 5+	P0.E02	D Chan 5 -	P0.F02	GND
P0.A03	D Chan 6+	P0.B03	D Chan 6 -	P0.C03	D Chan 7+	P0.D03	D Chan 7 -	P0.E03	D Chan 8+	P0.F03	GND
P0.A04	D Chan 8 -	P0.B04	D Chan 9+	P0.C04	D Chan 9 -	P0.D04	D Chan 10 +	P0.E04	D Chan 10 -	P0.F04	GND
P0.A05	D Chan 11+	P0.B05	D Chan 11 -	P0.C05	D Chan 12 +	P0.D05	D Chan 12 -	P0.E05	D Chan 13 +	P0.F05	GND
P0.A06	D Chan 13 -	P0.B06	D Chan 14 +	P0.C06	D Chan 14 -	P0.D06	D Chan 15 +	P0.E06	D Chan 15 -	P0.F06	GND
P0.A07	D Chan 16+	P0.B07	D Chan 16 -	P0.C07	D+2V5 ROP	P0.D07	D-2V5 ROP	P0.E07	D XTrigger	P0.F07	GND
P0.A08	D/XTrigger	P0.B08	N/C	P0.C08	N/C	P0.D08	D XCLK	P0.E08	D /XCLK	P0.F08	GND
P0.A09	D +12V	P0.B09	D AGND	P0.C09	D +12V	P0.D09	D AGND	P0.E09	D -12V	P0.F09	GND
P0.A10	D AGND	P0.B10	D -12V	P0.C10	D AGND	P0.D10	N/C	P0.E10	D AGND	P0.F10	GND
P0.A11	C Chan 1+	P0.B11	C Chan 1 -	P0.C11	C Chan 2+	P0.D11	C Chan 2 -	P0.E11	C Chan 3+	P0.F11	GND
P0.A12	C Chan 3 -	P0.B12	C Chan 4+	P0.C12	C Chan 4 -	P0.D12	C Chan 5+	P0.E12	C Chan 5 -	P0.F12	GND
P0.A13	C Chan 6+	P0.B13	C Chan 6-	P0.C13	C Chan 7+	P0.D13	C Chan 7 -	P0.E13	C Chan 8+	P0.F13	GND
P0.A14	C Chan 8-	P0.B14	C Chan 9+	P0.C14	C Chan 9-	P0.D14	C Chan 10+	P0.E14	C Chan 11+	P0.F14	GND
P0.A15	C Chan 11+	P0.B15	C Chan 11-	P0.C15	C Chan 12+	P0.D15	C Chan 12-	P0.E15	C Chan 13+	P0.F15	GND
P0.A16	C Chan 13-	P0.B16	C Chan 14+	P0.C16	C Chan 14-	P0.D16	C Chan 15+	P0.E16	C Chan 15-	P0.F16	GND
P0.A17	C Chan 16+	P0.B17	C Chan 16-	P0.C17	C+2V5 ROP	P0.D17	C-2V5 ROP	P0.E17	C XTrigger	P0.F17	GND
P0.A18	C/XTrigger	P0.B18	N/C	P0.C18	N/C	P0.D18	C XCLK	P0.E18	C/XCLK	P0.F18	GND
P0.A19	C +12V	P0.B19	C AGND	P0.C19	C +12V	P0.D19	C AGND	P0.E19	C -12V	P0.F19	GND


P0 pin assignment

PI ROW A	SIGNAL	PI ROW B	SIGNAL	PI ROW C	SIGNAL	PI ROW D	SIGNAL	PI ROW Z	SIGNAL
P1.A01	D00	P1.B01	N/C	P1.C01	D08	P1.D01	N/C	P1.Z01	N/C
P1.A02	D01	P1.B02	N/C	P1.C02	D09	P1.D02	N/C	P1.Z02	GND
P1.A03	D02	P1.B03	N/C	P1.C03	D10	P1.D03	N/C	P1.Z03	N/C
P1.A04	D03	P1.B04	BG0IN*	P1.C04	D11	P1.D04	N/C	P1.Z04	GND
P1.A05	D04	P1.B05	BG0OUT*	P1.C05	D12	P1.D05	N/C	P1.Z05	N/C
P1.A06	D05	P1.B06	BG1IN*	P1.C06	D13	P1.D06	N/C	P1.Z06	GND
P1.A07	D06	P1.B07	BG1OUT*	P1.C07	D14	P1.D07	N/C	P1.Z07	N/C
P1.A08	D07	P1.B08	BG2IN*	P1.C08	D15	P1.D08	N/C	P1.Z08	GND
P1.A09	GND	P1.B09	BG2OUT*	P1.C09	GND	P1.D09	N/C	P1.Z09	N/C
P1.A10	N/C	P1.B10	BG3IN*	P1.C10	N/C	P1.D10	N/C	P1.Z10	GND
P1.A11	GND	P1.B11	BG3OUT*	P1.C11	BERR*	P1.D11	N/C	P1.Z11	N/C
P1.A12	DS1*	P1.B12	N/C	P1.C12	RESET	P1.D12	+3.3V	P1.Z12	GND
P1.A13	DS0*	P1.B13	N/C	P1.C13	LWORD*	P1.D13	N/C	P1.Z13	N/C
P1.A14	WRITE	P1.B14	N/C	P1.C14	AM5	P1.D14	+3.3V	P1.Z14	GND
P1.A15	GND	P1.B15	N/C	P1.C15	A23	P1.D15	N/C	P1.Z15	N/C
P1.A16	DTACK*	P1.B16	AM0	P1.C16	A22	P1.D16	+3.3V	P1.Z16	GND
P1.A17	GND	P1.B17	AM1	P1.C17	A21	P1.D17	N/C	P1.Z17	N/C
P1.A18	AS	P1.B18	AM2	P1.C18	A20	P1.D18	+3.3V	P1.Z18	GND
P1.A19	GND	P1.B19	AM3	P1.C19	A19	P1.D19	N/C	P1.Z19	N/C
P1.A20	IACK	P1.B20	GND	P1.C20	A18	P1.D20	+3.3V	P1.Z20	GND
P1.A21	IACKIN*	P1.B21	N/C	P1.C21	A17	P1.D21	N/C	P1.Z21	N/C
P1.A22	IACKOUT	P1.B22	N/C	P1.C22	A16	P1.D22	+3.3V	P1.Z22	GND
P1.A23	AM4	P1.B23	GND	P1.C23	A15	P1.D23	N/C	P1.Z23	N/C
P1.A24	A07	P1.B24	IRQ7*	P1.C24	A14	P1.D24	+3.3V	P1.Z24	GND
P1.A25	A06	P1.B25	IRQ6*	P1.C25	A13	P1.D25	N/C	P1.Z25	N/C
P1.A26	A05	P1.B26	IRQ5*	P1.C26	A12	P1.D26	+3.3V	P1.Z26	GND
P1.A27	A04	P1.B27	IRQ4*	P1.C27	A11	P1.D27	N/C	P1.Z27	N/C
P1.A28	A03	P1.B28	IRQ3*	P1.C28	A10	P1.D28	+3.3V	P1.Z28	GND
P1.A29	A02	P1.B29	IRQ2*	P1.C29	A09	P1.D29	N/C	P1.Z29	N/C
P1.A30	A01	P1.B30	IRQ1*	P1.C30	A08	P1.D30	+3.3V	P1.Z30	GND
P1.A31	-12V	P1.B31	N/C	P1.C31	+12V	P1.D31	N/C	P1.Z31	N/C
P1.A32	+5V	P1.B32	+5V	P1.C32	+5V	P1.D32	+5V	P1.Z32	GND

P1 Pin Assignment

ROWA	SIG	ROWB	SIG	ROWC	SIG	ROWD	SIG	ROWZ	SIG
P2.A01	B +12V	P2.B01	+5V	P2.C01	B AGND	P2.D01	C -12V	P2.Z01	C AGND
P2.A02	B +12V	P2.B02	GND	P2.C02	B AGND	P2.D02	C AGND	P2.Z02	GND
P2.A03	B -12V	P2.B03	N/C	P2.C03	B AGND	P2.D03	C AGND	P2.Z03	N/C
P2.A04	B -12V	P2.B04	A24	P2.C04	B AGND	P2.D04	B Chan 1 +	P2.Z04	GND
P2.A05	N/C	P2.B05	A25	P2.C05	B AGND	P2.D05	B Chan 2 +	P2.Z05	B Chan 1 -
P2.A06	A Chan 1 +	P2.B06	A26	P2.C06	A Chan 1 -	P2.D06	B Chan 2 -	P2.Z06	GND
P2.A07	A Chan 2 +	P2.B07	A27	P2.C07	A Chan 2 -	P2.D07	B Chan 3 -	P2.Z07	B Chan 3 +
P2.A08	A Chan 3 +	P2.B08	A28	P2.C08	A Chan 3 -	P2.D08	B Chan 4 +	P2.Z08	GND
P2.A09	A Chan 4 +	P2.B09	A29	P2.C09	A Chan 4 -	P2.D09	B Chan 5 +	P2.Z09	B Chan 4 -
P2.A10	A Chan 5 +	P2.B10	A30	P2.C10	A Chan 5 -	P2.D10	B Chan 5 -	P2.Z10	GND
P2.A11	A Chan 6 +	P2.B11	A31	P2.C11	A Chan 6 -	P2.D11	B Chan 6 -	P2.Z11	B Chan 6 +
P2.A12	A Chan 7 +	P2.B12	GND	P2.C12	A Chan 7 -	P2.D12	B Chan 7 +	P2.Z12	GND
P2.A13	A Chan 8 +	P2.B13	+5V	P2.C13	A Chan 8 -	P2.D13	B Chan 8 +	P2.Z13	B Chan 7 -
P2.A14	A Chan 9 +	P2.B14	N/C	P2.C14	A Chan 9 -	P2.D14	B Chan 8 -	P2.Z14	GND
P2.A15	A Chan 10 +	P2.B15	N/C	P2.C15	A Chan 10 -	P2.D15	B Chan 9 -	P2.Z15	B Chan 9 +
P2.A16	A Chan 11 +	P2.B16	N/C	P2.C16	A Chan 11 -	P2.D16	B Chan 10 +	P2.Z16	GND
P2.A17	A Chan 12 +	P2.B17	N/C	P2.C17	A Chan 12 -	P2.D17	B Chan 11 +	P2.Z17	B Chan 10 -
P2.A18	A Chan 13 +	P2.B18	N/C	P2.C18	A Chan 13 -	P2.D18	B Chan 11 -	P2.Z18	GND
P2.A19	A Chan 14 +	P2.B19	N/C	P2.C19	A Chan 14 -	P2.D19	B Chan 12 -	P2.Z19	B Chan 12+
P2.A20	A Chan 15 +	P2.B20	N/C	P2.C20	A Chan 15 -	P2.D20	B Chan 13 +	P2.Z20	GND
P2.A21	A Chan 16 +	P2.B21	N/C	P2.C21	A Chan 16 -	P2.D21	B Chan 14 +	P2.Z21	B Chan 13 -
P2.A22	A +2V5 ROP	P2.B22	GND	P2.C22	A -2V5 ROP	P2.D22	B Chan 14 -	P2.Z22	GND
P2.A23	A X Trigger	P2.B23	N/C	P2.C23	A /XTrigger	P2.D23	B Chan 15 -	P2.Z23	B Chan 15+
P2.A24	N/C	P2.B24	N/C	P2.C24	N/C	P2.D24	B Chan 16 +	P2.Z24	GND
P2.A25	A XCLK	P2.B25	N/C	P2.C25	A /XCLK	P2.D25	B +2V5 ROP	P2.Z25	B Chan 16 -
P2.A26	A +12V	P2.B26	N/C	P2.C26	A AGND	P2.D26	B -2V5 ROP	P2.Z26	GND
P2.A27	A +12V	P2.B27	N/C	P2.C27	A AGND	P2.D27	B /XTrigger	P2.Z27	B X Trigger
P2.A28	A -12V	P2.B28	N/C	P2.C28	A AGND	P2.D28	N/C	P2.Z28	GND
P2.A29	A -12V	P2.B29	N/C	P2.C29	A AGND	P2.D29	B XCLK	P2.Z29	N/C
P2.A30	N/C	P2.B30	N/C	P2.C30	A AGND	P2.D30	B /XCLK	P2.Z30	GND
P2.A31	Out+3.3V	P2.B31	GND	P2.C31	Out+3.3V	P2.D31	GND	P2.Z31	Out +3.3V
P2.A32	Out +5V	P2.B32	+5V	P2.C32	Out +5V	P2.D32	PC +5V	P2.Z32	GND

P2 pin assignment

 Denotes pins with thickened tracks which can be used for power inputs