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IP-DIO-8505
Digital I/O Board
INDUSTRY PACK

USERS MANUAL

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1 INTRODUCTION

This is a single-width IP module with sixteen channels of buffered digital input/output.
The I/O signals are accessed as the top and bottom halves of one 16-bit location. Each set of eight signals can be selected to be inputs or outputs. At power-up or after an IP reset, all signals default to the input state.
A control register associated with the I/O register determines whether each half will act as inputs or outputs and for input mode also controls the way that inputs are sampled.
When output mode is selected, the output data reflects the last data written to the corresponding I/O register. The buffered TTL outputs exactly mirror the logical state of the data written, thus writing a '1' to the register makes the TTL output signal go high.
When input mode is selected other control register bits come into play and determine the sampling mode of the register. One common sampling clock can be selected from a choice of four in the range 1KHz to 1MHz. Also, a common de-bounce clock can be chosen from the following choices: 100Hz, 200Hz, 500Hz and 1KHz or a divided down external clock source.
Writing to the port when input mode is selected has no effect.
Reading the port when output mode is selected will read back the last data written.
A pulse parameter register determines the duration of pulsed outputs up to 100 seconds.
A further register associated with each port controls which bits may generate an interrupt when in input mode. [Again, this function has no effect when in output mode.]
All the above registers occupy I/O space on the IP card, starting at offset zero as follows:

Offset	Name	Description
0	LKC	Last Known Change/Data Register
2	CSR	Control and Status Register
4	IMR	Mask Register
6	DBR	Debounce Register
8	PSR	Pulse Select Register
A	PPR	Pulse Parameter Register

2 PRODUCT SPECIFICATIONS

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of input/outputs:	16 (configurable as 16 in or 16 out or 8 in and 8 out)
Input level:	TTL
Output level	TTL high current
Input/output termination:	470 ohms to 0V or +3.3V by jumpered selection
Internal clock:	40MHz oscillator.
Clock accuracy:	+/-100ppm (0.01%)
External clock:	TTL input 1MHz typical.
Power:	+5V @ 180mA typical

3 OPERATING MODES

There are several basic operating modes set according to the CSR (see below):-

4 APPLICATION REGISTERS

There are 6 application specific (I/O) registers:-
[These registers are designed to 'mimic' those on the 8001 digital I/O Card].

4.1 Last Known Change/Data Register LKC IP Address 0 (Read/Write)

Address: Base + 0x0

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
LKC15	LKC14	LKC13	LKC12	LKC11	LKC10	LKC9	LKC8	LKC7	LKC6	LKC5	LKC4	LKC3	LKC2	LKC1	LKC0

This register shows the last known state of the I/O data. In the case of inputs it shows the input states conditioned by de-bounce and change-of-state detection. For outputs, the new data should be written here.

4.2 Control/Status Register CSR IP Address 1 (Read/Write)

Address: Base + 0x2

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
COS BIT	**IO INT EN**	NU	Ring Mode	OM1	OM0	MEM EN	SH1	SH0	SCAN T1	SCAN T0	COS T1	COS T0	SCLK SEL1	SCLK SEL0	SCAN EN

SCAN EN Start scanning digital inputs
SCLK SEL 0-1 Select source of scan and change-of-state clock: '00' = Internal 1MHz clock; '01' = Ext. clock from transition card.
COS T0-T1 Debounce clock frequency select:

CSR I/O		Debounce Scan rate	
Bit 4	**Bit 3**	**Internal Clock**	**Ext/Strobe clock**
0	0	100Hz	Div 10000
0	1	200Hz	Div 5000
1	0	500Hz	Div 2000
1	1	1KHz	Div 1000

SCAN T0-T1 Select scan rate of digital inputs:

CSR I/O		Scan Rate	
Bit 6	**Bit5**	**Internal Clock**	**Ext/Strobe clock**
0	0	1KHz	Div 1000
0	1	10KHz	Div 100
1	0	100KHz	Div 10
1	1	1MHz	Div 1

SH 0-1 Memory update inhibit source select: Not used.
MEM EN Enables memory update not used.
OM 0-1 Enable digital lines: '00' = all inputs; '11' = all outputs; '10' = half out (top 8 bits)/ half in (bottom 8 bits) '01' = half out (bottom 8 bits)/ half in (top 8 bits).
RING MODE Not used.
IO INT EN Enable interrupts to be generated by a change of state of the IO inputs.
COS BIT This bit signifies a change of state which causes an interrupt to be generated. A '0' needs to be written to this bit to clear the interrupt.

4.3 Digital Input Interrupt Mask Register IMR IP Address 2 (Read/Write)

Address: Base + 0x4

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0

The mask register only acts on input signals. Writing a '1' to a bit will allow a change-of-state on the corresponding input to generate an interrupt. Any output bits that have a corresponding '1' in this register will not generate interrupts.

4.4 Debounce RegisterDBR IP Address 3 (Read/Write)

Address: Base + 0x6

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

The de-bounce register only applies to bit selected as inputs. A '1' written to a bit position causes that input to be de-bounced at the selected common clock rate

4.5 Pulse Select Register PSR IP Address 4(Read/Write)

Address: Base + 0x8

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
PS15	PS14	PS13	PS12	PS11	PS10	PS9	PS8	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0

The Pulse Select register only applies to bit selected as outputs. Writing a '1' to a bit makes the corresponding output a pulsed type. In this case, writing a '1' to a bit in the LKC/Data register will cause the corresponding output to produce a pulse of a width controlled by the Pulse Parameter Register. At the end of the pulse, the corresponding bit in the LKC/Data register will be cleared.

4.6 Pulse Parameter Register PPR IP Address 5(Read/Write)

Address: Base + 0xA

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
PP15	PP14	PP13	PP12	PP11	PP10	PP9	PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0

The pulse parameter register controls the width of the output pulse produced when the corresponding bit is written as a '1' in the data register. The function of the bits is as follows:

Width	**PP4**	**PP3**	**PP2**	**PP1**	**PP0**
1 msec	0	0	0	0	0
10 msec	0	0	0	0	1
100 msec	0	0	0	1	0
1 second	0	0	0	1	1
2 seconds	0	0	1	0	0
5 seconds	0	0	1	0	1
10 seconds	0	0	1	1	0
20 seconds	0	0	1	1	1
50 seconds	0	1	0	0	0
100 secs	0	1	0	0	1

All other bits – no effect.

4.7 Vector IRV IP address 6 (Read/Write)

Address: Base + 0xC
Sets the interrupt request vector read by interrupt select.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

5 ID PROM

The ID configuration information held in the PROM is as detailed below.
The byte addresses of the ID PROM are as below:-

Base+80	ASCII 'VI'	5649h	
Base+82	ASCII 'TA'	5441h	
Base+84	ASCII '4 '	3420h	
Base+86	Hytec ID high byte	0080h	
Base+88	Hytec ID low word	0300h	
Base+8A	Model number	8505h	
Base+8C	Revision	3301h	(This shows PCB Issue 3 and Xilinx at issue 1)
Base+8E	Reserved	0000h	
Base+90	Driver ID	0000h	
Base+92	Driver ID	0000h	
Base+94	Flags	0002h	
Base+96	No of bytes used	001Ah	
Base+98	Not used	0000h	
Base+9A	Serial Number	xxxxd	

6 Jumpers

PCB JUMPER (settings for PCB Issues 3)

J1 Factory set

J2 Terminate data I/O lines via 470ohms to GND, 3.3Volts or 5Volts.
Terminate to GND = pins 2 & 4
Terminate to 3.3Volts = pins 2 & 1.
Terminate to 5Volts = pins 2 & 3.

J3 Terminate Ext Clk & spare I/O lines via 470ohms to GND, 3.3Volts or 5Volts.
Terminate to GND = pins 2 & 4
Terminate to 3.3Volts = pins 2 & 1.
Terminate to 5Volts = pins 2 & 3.

J5 Logic polarity of input low byte
J6 Logic polarity of input high byte
J7 Logic polarity of output low byte
J8 Logic polarity of output high byte

7 I/O Connector – 50 way on 8505 Board

Pin	Signal	Pin	Signal
1	I/O 1	26	GND
2	GND	27	I/O 14
3	I/O 2	28	GND
4	GND	29	I/O 15
5	I/O 3	30	GND
6	GND	31	I/O 16
7	I/O 4	32	GND
8	GND	33	Ext Clk
9	I/O5	34	GND
10	GND	35	Spare 2
11	I/O 6	36	GND
12	GND	37	Spare 3
13	I/O 7	38	GND
14	GND	39	Spare 4
15	I/O 8	40	GND
16	GND	41	N.C.
17	I/O 9	42	GND
18	GND	43	N.C.
19	I/O 10	44	GND
20	GND	45	N.C.
21	I/O 11	46	GND
22	GND	47	N.C.
23	I/O 12	48	GND
24	GND	49	N.C.
25	I/O 13	50	GND

8 8. HYTEC TRANSITION BOARD CONNECTIONS

TB 8304 I/O Connector – 50 way on transition board panel
Pin Assignments
Connectors 1-4

Pin	Signal	Pin	Signal
1	Gnd	26	I/O1 +
2	Gnd	27	I/O2 +
3	Gnd	28	I/O3 +
4	Gnd	29	I/O4 +
5	Gnd	30	I/O5 +
6	Gnd	31	I/O6 +
7	Gnd	32	I/O7 +
8	Gnd	33	I/O8 +
9	Gnd	34	I/O9 +
10	Gnd	35	I/O10 +
11	Gnd	36	I/O11 +
12	Gnd	37	I/O12 +
13	Gnd	38	I/O13 +
14	Gnd	39	I/O14 +
15	Gnd	40	I/O15 +
16	Gnd	41	I/O16 +
17	Gnd	42	Ext Clk
18	Gnd	43	Spare 2
19	Gnd	44	Spare 3
20	Gnd	45	Spare 4
21	Gnd	46	NC
22	Gnd	47	NC
23	Gnd	48	NC
24	Gnd	49	NC
25	Gnd	50	NC