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SC8512
16-CHANNEL 32-BIT SCALER INDUSTRY PACK

USERS MANUAL

PCB Issue 2.0
FPGAs Version 8512V204

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CONTENTS

1. INTRODUCTION

The Hytec IP-SC-8512 is a single-width Industry Pack that provides 16 pre-settable counting registers with the following characteristics:-

- 16 independent pre-settable counting channels
- Full 32 bits binary count capacity
- The ability to daisy-chain two counters for 64 bit binary counts.
- Each scaler channel can count up from a pre loaded value
- Count rates from D.C. to 10MHz
- An ARM register allows individual channels to be enabled or Inhibited
- Overflow register provides status of all counters
- Any counter can be programmed to disARM (Inhibit) all counters or block of counters on overflow.
- Block mode allows a group of counters to be defined and controlled by any one or all of the counters in the group.
- Maskable interrupt generated by each channel on overflow
- Programmable gate enable connects internal 10MHz clock to counter inputs
- Scaler external inputs via transition board
- Hardware Start/stop control via IP Strobe* signal (on the Hytec 800X series IP carrier cards this is generated from front panel inhibit Lemo).
- A common hardware ARM IN signal via the transition board, ARMs all counters.
- Programmable ARM OUT signal via transition board
- Counters can be read on the fly via a shadow register
- The ability to read the module identity, manufacturer, model, revisions and serial number from an onboard ID ROM.

2. PRODUCT SPECIFICATIONS

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of channels:	16
Max. count:	32 bits with IRQ on overflow. Overflow can clock next scaler using daisy-chain giving 64 bit count.
Data format:	Binary
Max count rate:	10MHz
Gate Input levels:	TTL compatible with jumper selectable 470Ω resistor pull-up or pull-down with positive edge clocking
Gate control:	Overall gate via Strobe* line on IP logic connector
Start/Stop levels:	TTL compatible with high value pull-up resistor (high level = Start)
ARM levels:	TTL compatible with jumper selectable 470Ω pull-up or pull-down resistor (high level = ARM all)
Internal clock:	10MHz oscillator with programmable connection to each counter gate.
Clock accuracy:	+/-100ppm (0.01%)
Power:	+5V @ 180mA typical

3. Operating Modes

There are three basic operating modes:-

1. **Basic Counter** - the counters are reset to zero either using reset or by write 0 to the counter or a pre-set value can be loaded in to the counter. The counter will count input pulses when enabled and armed until it overflows, generating an IRQ if enabled and inhibiting further counting.

2. **Interval Timer Block Mode** - a number of sequential counters can be defined as a block. Any or all counters in the block can then be set to control the Inhibit bit of all counters in the block i.e. any or all counters in the block can act as an interval timer.

3. **Daisy Chain** - two counters can be linked together to form a 64-bit counter by setting bits in the Daisy Chain register. Any bit, which is set in this register, allows an overflow on the respective channel to clock the next counter. The following counter pairs can be linked together:- 1 & 2, 3 & 4, 5 & 6, 7 & 8, 9 & 10, 11& 12, 13 & 14, 15 & 16.
   Interval Timer counters can also be daisy chained.

4. Application Registers

There are eleven application specific (I/O) registers; the CSR,

4.1 Control & Status Register (CSR)

Read/write register
Defines the interrupt vector V7-V0 reset control, start/stop and IRQ status.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V7	V6	V5	V4	V3	V2	V1	V0	T	x	x	x	EN	SS	R	IRQ

IRQ Any IRQ which is set and masked on sets this status bit (read only).
R Reset - writing a 1 to this bit resets all the counters and registers to zero apart from the Control & Status Register and ARM register (write only).
SS Start/stop – the overall enable (Strobe*) status (read only).
EN Hardware ARM IN from Transition board ARMs all counters (read only).
T Test. Writing a logic 1 increments all scalers by one (write only).

4.2 Arm Register (IP address 1)

Read/write register.
Any bit which is set arms the relevant counter.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

4.3 OVERFLOW Register (IP address 2)

Read/write register.
The overflow from each scaler is latched. When a bit is set it indicates overflow. If the interrupt enable for the channel is set then an interrupt will be generated, to clear the interrupt writing 0 to corresponding bit in the overflow register.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

4.4 IRQ Mask Register (IP address 3)

Read/write register.
Any bit which is set allows an overflow on the respective channel to generate IRQ.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0

4.5 Interval-enable Register (IP address 4)

Read/write register.
Any bit which is set defines that a counter is used as an interval timer. All counters or all counters defined in a block will be disarmed.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

4.6 Block Mode Register (IP address 5)

Read/write register.
Any bit which is set defines the end of a block and the start of the next block. Bit zero has no function.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	X

4.7 Daisy-chain Register (IP address 6)

Read/write register.
Any bit which is set allows an overflow on the respective channel to clock the next counter to give a 64 bit counter or interval timer.
The following counter pairs can be linked together:- 1 & 2, 3 & 4, 5 & 6, 7 & 8, 9 & 10, 11& 12, 13 & 14, 15 & 16.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
O15	O14	O13	O12	O11	O10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0

4.8 Gate-enable Register (IP address 7)

Read/write register.
Any bit which is set enables the internal 10MHz clock to gate a specific counter.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
G15	G14	G13	G12	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0

4.9 ARM ENABLE Register (IP address 8)

Write only register.
Allows individual bits in the ARM register to be set when a ‘1’ is written to them. Writing a ‘0’ will not change the value of the bit.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

4.10 CLEAR OVERFLOW Register (IP address 9)

Write only register.
Allows individual bits in the Overflow register to be cleared when a ‘1’ is written to them. Writing a ‘0’ will not change the value of the bit.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

4.11 CLEAR ARM Register (IP address A)

Write only register.
Allows individual bits in the ARM register to be cleared when a ‘1’ is written to them. Writing a ‘0’ will not change the value of the bit.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

5. Scaler Counter Registers

Counter Registers 0 to 15 are held in the memory space of the IP scaler card.

The counter registers may be read at memory addresses 00-1E(even) for the least significant words

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0

and 01-1F(odd) for the most significant words.

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16

The counter value can be set by writing to the appropriate address.

6. SCALER OPERATION

6.1 Scaler Inputs

The counters can be clocked either internally using the 10MHz clock or by writing to the test bit 'T' in the CSR or externally via the transition board see appendix B for connections.

6.2 Set number of counts to overflow.

The number of counts that are required before the counter overflows and cause an interrupt (if set) can be set by loading a value in to the counter registers located in memory or a reset can be issued which will clear all counters and registers.

Example calculation of preload value

The following calculation gives the value required for 100 counts:-

4294967295 – 100 = 4294967195 dec

FFFFFFFFh – 64h = FFFFFF9B hex

6.3 Set up and enable interrupts.

If interrupts are to be used then need to load the interrupt vector in to the top byte of the CSR register. Then enable the interrupt for the relevant counters by writing 1 to the respective bit in the IRQ Mask register.

6.4 Check Overflow Register is Zeroed

If a reset has not been issued since a pervious count the overflow register may have overflow bits already set. These bits will need to be cleared by writing a zero to them using the overflow register (address 0x2) or by writing a '1' to them using the Clear Overflow register (address 0x9).

6.5 ARMing the Counters

There are two ways to arm the counters:-

1. write a one in to the relevant bit of the ARM register, This can be done by writing to the ARM register at address 0x1 (this will over write the whole contents of the ARM register) or can write a '1' to the relevant bit in the ARM Enable register address 0x8.
2. use the ARM IN hardware signal from the transition board. When this is high all the counters are ARMed regardless of the bits set in the ARM register. When the ARM IN hardware signal is used the disarm on overflow is negated.

For the counters to be reARMed they must not be in an overflow state i.e. 0xFFFFFFFF as the ARM bit will not be set (even if the overflow bit is cleared).

6.6 Clear ARM

Write a zero in to the relevant bit of the ARM register. This can be done by writing to the ARM register at address 0x1 (this will over write the whole contents of the ARM register) or a '1' can be written to the relevant bit in the Clear ARM register address 0xA.

6.7 ARM Out

The ARM OUT hardware signal (see appendix C) is programmed by the first bit (A0) of the ARM register.

6.8 Start/stop (the overall enable)

The SC8512 can be Stopped and Started by taking the overall counter enable Low (Stop) or High (Start).
This input is pulled high on the SC8512 scaler so if not driven then the scaler will be constantly enabled.
The overall enable (Start/stop) of the scaler can be controlled via the IP card Stobe input. On the Hytec 800X series IP carrier cards this is generated from front panel inhibit Lemo, or the rear RST-TRIG lemo of the Hytec IOC 9010

6.9 Reading Counters on The Fly

All counters have their current count stored in a shadow register, this allows readouts to be taken in parallel to the acquisition of new data.

6.10 Overflow Set

When the counter reaches its terminal count the relevant bit is set in the Overflow register. If the interrupt enable has been set for the counter via the IRQ mask register then an interrupt will be generated. Also at this point the counter will be automatically stopped by clearing its arm bit in the ARM register.

6.11 Interrupt Handling

The interrupt handling routine should clear the interrupt line as soon as possible, this is achieved by reading the Overflow register and interrupt mask register to see which counter/s have caused the interrupt and then zero these bits in the Overflow register.

7. DAISY CHAIN OPERATION

Two counters can be linked together to form a 64-bit counter by setting bits in the Daisy Chain register. Any bit, which is set in this register, allows an overflow on the respective channel to clock the next scaler. The following counter pairs can be linked together:- 1 & 2, 3 & 4, 5 & 6, 7 & 8, 9 & 10, 11& 12, 13 & 14, 15 & 16.

Example

To set up counters 1 and 2 as a daisy chain pair set bit 0 to 1 in the Daisy Chain register.
Load the counters 1 and 2 to give the correct number of count before an interrupt is generated.
If an interrupt is to be generated then enable interrupts using the IRQ mask register on counter 1 only (counter 2 does not need to have its interrupts enabled).
To start the 64 bit scaler write a 1 to bit 0 of the ARM register only or use the hardware ARM IN signal. If hardware ARM IN is used make sure that counter 2 does not have any clocks on to its inputs as these will clock counter 2 causing an error.
The interrupt cleared by reading the Overflow register to see which counter/s have caused the interrupt and then zero these bit in the Overflow register.

8. INTERVAL TIMER BLOCK MODE OPERATION

Any counter or counters can be used to inhibit other counters (Interval Timers) by setting the corresponding bit/s to a one in the interval timer enable register. When these counters overflow they will clear all the ARM bits of the counters defined in a block.

8.1.1 Defining a Block

Any bit which is set to a '1' in the block mode register defines the end of a block and the start of the next block. A block is defined as all counters up to counter defined as the end of block x and the start of block y. i.e. 0x0480 written to the block mode register will define three blocks the first block starts at counter 0 and includes all counters up to counter 6. Counter 7 is the start of the next block which consist of counters 7 to 9 and the last block is defined from counters 10 to 15.

8.1.2 Selecting and Setting an Interval Timer

Any counters in a block can be defined as interval timer by writing a '1' to the corresponding bit in the interval enable register. A counter defined as an interval timer controls the ARM bits of all the counters in a group even other interval timers defined in the block. The first interval time in a block to overflow clears the ARM bits for all counters in the block and will generate an interrupt if enabled. Any counter in the block is able to count during this period if armed up to its overflow where it will clear it own ARM bit in the ARM register and generate an interrupt if enabled.
An interval timer can be loaded with a preset value and then clocked by either the internal or external clock. When an interval timer reaching its terminal count an overflow is generated along with an IRQ if enabled.

8.1.3 64 bit Interval Timer

A 64bit counter can also be defined as an interval timer, here the 64bit counter is set up as above, and the first 32bit counter is defined as an interval timer only.

9. ID PROM

The 8512 IP module includes a configuration ID PROM. The ID information held in the PROM is as detailed below.

The byte addresses of the ID PROM are as below:-

Base+80	ASCII 'VI'	5649h	
Base+82	ASCII 'TA'	5441h	
Base+84	ASCII '4 '	3420h	
Base+86	Hytec ID high byte	0080h	
Base+88	Hytec ID low word	0300h	
Base+8A	Model number	8512h	
Base+8C	Revision	2204h	This shows PCB Issue 2 and Xilinx V204 means FPGA at issue 4 for PCB issue 2.
Base+8E	Reserved	0000h	
Base+90	Driver ID	0000h	
Base+92	Driver ID	0000h	
Base+94	Flags	0002h	
Base+96	No of bytes used	001Ah	
Base+98	Not used	xxxxh	
Base+9A	Serial Number	xxxxdec	

APPENDIX A

PCB JUMPER (settings for PCB Issues 1 and 2)

J1 Factory set

J2 Terminate external scaler clocks to GND or 3Volts.
Terminate to GND = pins 1 & 2 Terminate to 3Volts = pins2 & 3.

J3 Terminate external control lines ARM IN and ARM OUT to GND or 3Volts
Terminate to GND = pins 1 & 2 Terminate to 3Volts = pins2 & 3.

J4 to J10 not used

APPENDIX B

I/O Connector – 50 way on 8512 Scaler Board

Pin	Signal	Pin	Signal
1	Count IN 1	26	GND
2	GND	27	Count IN 14
3	Count IN 2	28	GND
4	GND	29	Count IN 15
5	Count IN 3	30	GND
6	GND	31	Count IN 16
7	Count IN 4	32	GND
8	GND	33	Spare 1
9	Count IN 5	34	GND
10	GND	35	ARM Out
11	Count IN 6	36	GND
12	GND	37	Spare 2
13	Count IN 7	38	GND
14	GND	39	ARM In
15	Count IN 8	40	GND
16	GND	41	N.C.
17	Count IN 9	42	GND
18	GND	43	N.C.
19	Count IN 10	44	GND
20	GND	45	N.C.
21	Count IN 11	46	GND
22	GND	47	N.C.
23	Count IN 12	48	GND
24	GND	49	N.C.
25	Count IN 13	50	GND

APPENDIX C
HYTEC TRANSITION CARD CONNECTIONS

I/O Connector – 50 way on transition

Card 8202 Where this feeds ONE IP sites

Pin	Signal	Pin	Signal
1	GND	26	Count IN 1
2	GND	27	Count IN 2
3	GND	28	Count IN 3
4	GND	29	Count IN 4
5	GND	30	Count IN 5
6	GND	31	Count IN 6
7	GND	32	Count IN 7
8	GND	33	Count IN 8
9	GND	34	Count IN 9
10	GND	35	Count IN 10
11	GND	36	Count IN 11
12	GND	37	Count IN 12
13	GND	38	Count IN 13
14	GND	39	Count IN 14
15	GND	40	Count IN 15
16	GND	41	Count IN 16
17	N.C.	42	N.C.
18	GND	43	ARM Out
19	N.C.	44	N.C.
20	GND	45	ARM In
21	N.C.	46	N.C.
22	N.C.	47	N.C.
23	N.C.	48	N.C.
24	N.C.	49	N.C.
25	N.C.	50	N.C.

APPENDIX D
SAMPLE SOFTWARE FOR BASIC OPERATION

- Set up carrier card
- Scaler_OI-> Status = 0x0002; //Reset all register and counter on 8512
- Scaler_OI-> Status = INT_VECT<<8; // Load interrupt vector register top byte of CSR reg
- Scaler_OI-> IRQ_Mask = 0x0001; //Enable interrupts on scaler 0
- Scaler_OI-> DisARM = 0x0000; //No scalers set as interval timers
- Scaler_OI-> BLOCK_SEL = 0x0000; //No blocks defined
- Scaler_OI-> Gate_EN = 0x0001; //Scaler 0 set to use 10MHz internal clock
- Scaler_OI-> Daisy_Chain = 0x0000; //No scalers daisy chained
- Scaler_MEM->SC_LS0 = 0xyyyy; //Write to least significant word of scaler 0
- Scaler_MEM->SC_MS0 = 0xyyyy; //Write to most significant word of scaler 0
- Scaler_OI-> ARM = 0x0001; //Arm scaler 0 only or could use hardware ARM