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SI8516
Octal RS-485
INDUSTRY PACK

USERS MANUAL

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CONTENTS

1. Product Description

The Hytec IP-SI-8516 is a single-width Industry Pack that provides 8 serial interface lines with the following characteristics:-

- 8 independent RS-485 UART channels
- 64 byte Transmit and Receive FIFOs
- Transmit and Receive FIFO level counters
- Programmable Tx and Rx FIFO Trigger Levels
- Automatic Xon/Xoff Software Flow Control with Status Indication
- Programmable Data Rate with Prescaler
- Up to 6.25 Mbps Serial Data Rate
- Single Interrupt Output for all 8 UARTs
- Global Interrupt Source for all 8 UARTs
- Simultaneous UART channel initialisation
- Auto RS485 Half-duplex Control with Programmable Turn-around Delay
- Programmable Full/Half-duplex line control

2. Specifications

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of channels:	8
Max. baud rate:	921.6kbps with internal clock.
Data format:	Binary/ASCII
Input/Output levels:	RS-485 differential
Internal clock:	14.7456MHz oscillator
Clock accuracy:	+/-100ppm (0.01%)
Power:	+5V @ 400mA typical
Fuses:	F1 1A Connects +5V to I/O connector pin.
Jumpers:	J1 Boot jumper – inserted to allow FPGA to load. J2,J3 not used.

3. Application Registers

There are a number of application specific (I/O) registers.

Interrupt Register (IP address 0)

Read/write register defines the vector V7-V0, Read only interrupt source U7-U0

D15	D14	D13	D12	D11	D10	D9	D8	D7	D	D5	D4	D3	D2	D1	D0
V7	V6	V5	V4	V3	V2	V1	V0	U7	U6	U5	U4	U3	U2	U1	U0

V0-7 Interrupt vector to be used during IACK
U0-7 Any bit which is set indicates the interrupting UART

Interrupt Source Registers 1-3 (IP address 1-3)

Indicate the source of each interrupt from UART0 to 7 . Bits 8-15 are 0.
Read only register.

D07	D06	D05	D04	D03	D02	D01	D00	D07	D06	D05	D04	D03	D02	D01	D00
U50	U42	U41	U40	U32	U31	U30	U22	U21	U20	U12	U11	U10	U02	U01	U00
								D07	D06	D05	D04	D03	D02	D01	D00
								U72	U71	U70	U62	U61	U60	U52	U51

Timer Control Register (IP address 4&5)

Read/write register.
CS-Clock Select S/R-Single/Retrigger SS-Start/Stop IE-Timer Interrupt Enable

D07	D06	D05	D04	D03	D02	D01	D00	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	0	0	0	0	CS	S/R	SS	IE

Timer Counter Register (IP address 6&7)

Read/write register.
Timer counter data register.

D07	D06	D05	D04	D03	D02	D01	D00	D07	D06	D05	D04	D03	D02	D01	D00
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

8x Mode Register (IP address 8)

Read/write register.
Logic 0 sets 16x sampling. Logic 1 sets 8x sampling

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	U7	U6	U5	U4	U3	U2	U1	U0

Full/Half-duplex Register (IP address 9)

Read/write register.
Logic 0 sets Half-duplex. Logic 1 sets Full-duplex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	F7	F6	F5	F4	F3	F2	F1	F0

Reset Register (IP address A).
Resets are write only
R0-7 reset UART0-7

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	R7	R6	R5	R4	R3	R2	R1	R0

Sleep Register (IP address B)
S0-7 set UART0-7 into sleep mode Read/write register.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	S7	S6	S5	S4	S3	S2	S1	S0

Device Revision Register (IP address C) (UART device revision – read only)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	R7	R6	R5	R4	R3	R2	R1	R0

Device ID Registers (IP address D) (UART device ID – read only)

D07	D06	D05	D04	D03	D02	D01	D00	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	I7	I6	I5	I4	I3	I2	I1	I0

Control Register (IP address E). (Read/write)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
IRQ	IE	0	0	0	0	ENI	Rst	0	0	0	0	0	0	0	WA

IRQ Any IRQ which is set and masked on sets this status bit. Read only
IE Interrupt Enable
WA Setting this to a 1 enables writing to all UARTs in parallel. Read/write
ENI Enable Infra-red mode. Read/write
Rst Writing a 1 generates a reset to the UART device.

4. UART Channel Configuration Registers (Memory addresses 00-7F)

Each UART has a set of 16 configuration registers at addresses 0x,1x,2x….7x as follows:

Address	Reg	R/W	D07	D06	D05	D04	D03	D02	D01	D00
0 (LCR7=0)	RHR	R	R7	R6	R5	R4	R3	R2	R1	R0
0 (LCR7=0)	THR	W	T7	T6	T5	T4	T3	T2	T1	T0
0 (LCR7=1)	DLL	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1 (LCR7=1)	DLH	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	IER	R/W	CTS	RTS	Xon	0	MSIE	RSIE	TEIE	RDIE
2	ISR	R	FE	FE	FC	Xoff	IS3	IS2	IS1	IS0
2	FCR	W	RFT	RFT	TFT	TFT	DMA	TFR	RFR	FE
3	LCR	R/W	DE	STB	SP	EP	PE	SB	WL1	WL0
4	MCR	R/W	BP	IRE	XA	ILE	OP22	OP12	RTS	DTR
5	LSR	R/W	RFE	TSRE	THE	RxB	RxFE	RxPE	RxO	RDR
6	MSR	R	CD	RI	DSR	CTS	DCD	DRI	DDS	DCT
6	MSR	W	DL3	DL2	DL1	DL0				
7	SPR	R/W	D7	D6	D5	D4	D3	D2	D1	D0
8	FCTR	R/W	TR1	TR0	AE	IIR	H3	H2	H1	H0
9	EFR	R/W	ACE	ARE	SCS	EN	SF3	SF2	SF1	SF0
A	TFCNT	R	D7	D6	D5	D4	D3	D2	D1	D0
A	TFTRG	W	D7	D6	D5	D4	D3	D2	D1	D0
B	RFCNT	R	D7	D6	D5	D4	D3	D2	D1	D0
B	RFTRG	W	D7	D6	D5	D4	D3	D2	D1	D0
C	XCHAR	R							XOnI	XOfI
C	XOFF1	W	D7	D6	D5	D4	D3	D2	D1	D0
D	XOFF2	W	D7	D6	D5	D4	D3	D2	D1	D0
E	XON1	W	D7	D6	D5	D4	D3	D2	D1	D0
F	XON2	W	D7	D6	D5	D4	D3	D2	D1	D0

RHR – Receive Holding Register THR – Transmit Holding Register
DLL – Div Latch Low DLH – Div Latch High
IER - Interrupt Enable Register ISR - Interrupt Status Register FCR – FIFO Control Register
LCR – Line Control Register MCR – Modem Control Register LSR – Line Status Register
MSR – Modem Status Register SPR - Scratch Pad Register
FCTR EFR - Enhanced Function Register
TFCNT- Transmit FIFO Counter TFTRG – Transmit FIFO Trigger Level
RFCNT – Receive FIFO Counter RFTRG – Receive FIFO Trigger Level
XOFF1 – Xoff Character 1 XOFF2 – Xoff Character 2
XON1 – Xon Character 1 XON2 – Xon Character 2

5. ID PROM

The ID data byte addresses are as below:-

00 ASCII 'VI'	02 ASCII 'TA'
04 ASCII '4 '	06 Hytec ID high byte
08 Hytec ID low word	0a Model number
0c Revision	0e UART
10 Driver ID	12 Driver ID
14 Flags (8MHz)	16 No of bytes used
18 Not used	20 Not used
22 Serial no. high word	24 Serial no. low word

6. IP-SI 8516 I/O Connector

Connector: 50 way

Pin	Signal	Pin	Signal
1	GND	26	GND
2	Tx0- (Full or half Dx)	27	Tx5- (Full or half Dx)
3	Tx0+ (Full or half Dx)	28	Tx5+ (Full or half Dx)
4	Rx0- (Full Dx only)	29	Rx5- (Full Dx only)
5	Rx0+ (Full Dx only)	30	Rx5+ (Full Dx only)
6	GND	31	GND
7	Tx1- (Full or half Dx)	32	Tx6- (Full or half Dx)
8	Tx1+ (Full or half Dx)	33	Tx6+ (Full or half Dx)
9	Rx1- (Full Dx only)	34	Rx6- (Full Dx only)
10	Rx1+ (Full Dx only)	35	Rx6+ (Full Dx only)
11	GND	36	GND
12	Tx2- (Full or half Dx)	37	Tx7- (Full or half Dx)
13	Tx2+ (Full or half Dx)	38	Tx7+ (Full or half Dx)
14	Rx2- (Full Dx only)	39	Rx7- (Full Dx only)
15	Rx2+ (Full Dx only)	40	Rx7+ (Full Dx only)
16	GND	41	GND
17	Tx3- (Full or half Dx)	42	+5V Fused
18	Tx3+ (Full or half Dx)	43	N/C
19	Rx3- (Full Dx only)	44	N/C
20	Rx3+ (Full Dx only)	45	N/C
21	GND	46	N/C
22	Tx4- (Full or half Dx)	47	N/C
23	Tx4+ (Full or half Dx)	48	N/C
24	Rx4- (Full Dx only)	49	N/C
25	Rx4+ (Full Dx only)	50	N/C

7. Connections to IP-SI-8516 using the TB8304 Straight-through Transition Board

SCSI Pin	RS-485	SCSI Pin	RS-485
1	TX0-	26	GND
2	RX0-	27	TX0+
3	GND	28	RX0+
4	TX1+	29	TX1-
5	RX1+	30	RX1-
6	TX2-	31	GND
7	RX2-	32	TX2+
8	GND	33	RX2+
9	TX3+	34	TX3-
10	RX3+	35	RX3-
11	TX4-	36	GND
12	RX4-	37	TX4+
13	GND	38	RX4+
14	TX5+	39	TX5-
15	RX5+	40	RX5-
16	TX6-	41	GND
17	RX6-	42	TX6+
18	GND	43	RX6+
19	TX7+	44	TX7-
20	RX7+	45	RX7-
21	+5V	46	GND
22	-	47	-
23	-	48	-
24	-	49	-
25	-	50	-

NOTES

1. /CD0-7 ARE TTL CARRIER DETECT OR GENERAL PURPOSE INPUTS
2. WHEN USING RS-485 HALF-DUPLEX CONNECT ONLY TX+ AND TX-