HYTEC ELECTRONICS LTD

VTD1612 TRANSIENT RECORDER
USER MANUAL
ISSUE 3

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CONTENTS

1. PRODUCT DESCRIPTION

1.1 DESCRIPTION

The 1612A Transient Digitiser is a dual height single width VME slave board which provides the digitisation and storage of analog waveforms present on up to sixteen differential input channels, it is an upgraded version of the 1612 with a 10MHz convertor in place of the original 2MHz part.. Each input is provided with a track/hold circuit so that all channels can be **simultaneously sampled**. The sampled voltages are multiplexed into a fast 12 bit ADC which has its own sample/hold amplifier. The ADC digitises the voltage and stores the resultant binary information in a 128K word RAM. A 512K version is available. Memory can be allocated according to the number of inputs selected, i.e. 1, 2, 4, 8 or 16 inputs use 128K, 64K, 32K, 16K or 8K words per input. The RAM is dual–ported and provides access for both the ADC and VME bus.

The board has programmable operating modes. Its main modes are:–

1.2 TRIGGERED BUFFER MODE

Three clock frequencies can be selected for pre–trigger, near post trigger and far post–trigger digitisation rates. Memory is equally divided between the pre–trigger and post–trigger buffers. When the module is armed by software command, clocking occurs at the pre–trigger frequency in the pre–trigger buffer. A trigger causes digitisation to occur at the near post–trigger frequency for a specified number of samples from the start of the post–trigger buffer followed by the far post–trigger frequency for a second specified number of samples. On completion, acquisition is halted.

1.3 CONTINUOUS MODE

Normally, when the 'full flag' interrupts digitisation is inhibited. However, it is possible to set up a continuous mode wherein digitisation occurs continuously. The 'half full' and 'full' flags can then be used as an indication of where in the memory digitisation has reached, so that alternate halves of memory can be read whilst still acquiring data. Samples are clocked at the pre–trigger clock frequency and the whole memory is used as a pre–trigger buffer.

1.4 SINGLE SCAN MODE

In this mode the pre–trigger clock is inhibited. When the VTD is triggered the input voltages are sampled and converted, the memory address pointer is incremented and the 'end of event' interrupt status bit is set. It is possible to trigger multiple scans using post–trigger counts of greater than one.

The board can interrupt for one or all of three states:–

(a) the memory is full (completion of post–trigger) or,
(b) the memory is half full or,
(c) the end of a triggered event record has been reached.

It is possible to read the contents of an addressed memory location via the VME bus whilst the board is digitising. This concurrent access mode is permitted once per ADC conversion, i.e. not exceeding a read rate of one megaword per second.

At the trigger point the current memory address will be recorded in a time–stamp buffer. Up to 8192 time stamps can be recorded.

The board can be triggered from an external analog source, from channel 1, by an external logic pulse, or by software command.

The clock frequency can be programmed from 1MHz down to 0.01Hz using either an internal or external clock source with a maximum frequency of 8MHz. The clock is buffered and is transmitted via a front panel connector. Provision is made for connecting Clock Out to Clock In of another module. Trigger is also buffered and transmitted as a logic pulse via a connector so that one module can trigger another.

2. SPECIFICATIONS

Operating temperature range: 0 to 45^{o}C ambient.

Power requirements: +5V at 2.5A from the VMEbus
+5V STDBY maintains the RAM in the event of .power failure.
(+/– 5V is generated on board).

FRONT PANEL CONNECTORS

ANALOG INPUTS:

Connector type:	37 way D type socket.
Pin allocation:	1–16 analog positive inputs, 20–35 analog negative inputs, 17 analog trigger positive input, 36 analog trigger negative input, 18, 19, 37 Gnd.
Signal:	+/– 10V. Gains 1–10 may be ordered on a channel by channel basis.
Input impedance:	40K ohms differential. 20K ohms common mode.
Input Protection:	+/– 300V overvoltage for 1 second.
Common mode:	+/– 100V for linear operation.
CMRR:	70db at 100KHz.
Amplifier bandwidth:	5MHz (small signal).
Trigger signal:	As for analog inputs.
Acquisition time:	1uS to $\pm$0.025% for a +/– 10V transition, in multichannel mode, single channel 625nS to $\pm$0.025%.
Aperture jitter:	1nS max.
Aperture delay:	70nS.
ADC resolution:	12 bits.
ADC conversion:	625nS max to hold, digitise and store. (Internal converter 100nS).
Linearity error:	+/– 1/2 LSB.
Channel error:	+/– 1/2 LSB.
ADC error:	+/– 1/2 LSB.
Drift:	+/–30 ppm per ^{o}C (max).

DIGITAL SIGNALS:

Trigger input:	Lemo 00250 socket. Negative going TTL pulse. 200nS min. width.
Trigger output:	Lemo 00250 socket. Negative going TTL signal.
Clock in:	Lemo 00250 socket. Negative going TTL signal. 10MHz frequency max.
Clock out:	Lemo 00250 socket. Negative going TTL signal generated by internal clock or Clock In.
Busy out:	Lemo 00250 socket. Negative going TTL signal generated when a trigger has occurred until the end of event.

FRONT PANEL INDICATORS:

Armed:	LED which illuminates when the input waveforms are being digitised commencing at the pre–trigger rate.
Continuous:	LED which illuminates when 'Continuous' mode is set.
Trigger:	LED which illuminates for 200mS when a trigger occurs.
Full:	LED which illuminates when the memory is full.
Half–full:	LED which illuminates when the memory is half full.
Module address:	LED which illuminates for 200mS when the module is accessed from the VMEbus.
Busy:	LED which indicates the status of the Busy status signal. (An event is being recorded).
Error:	LED which illuminates when the module is addressed and bus timeout occurs.

BACKPLANE CONNECTORS:

The board uses the J1/P1 connector of the VMEbus. It is equipped with a jumper selectable base address and interrupt priority level. It recognises standard (24 bit) addressing. The memory map of the module is shown below:

Reserved (two words)	)
Reset memory address	)
Board descriptor	)
Upper/lower trigger threshold	)
Far post–trigger frequency	)
Near post–trigger frequency	)
Far post–trigger clock count	)
Near post–trigger clock count	) 16 words
No. of channels/memory allocation	)
ADC memory address pointer MS	)
ADC memory address pointer LS	)
Interrupt status	)
Interrupt vector	)
Time stamp data memory	) 8K words
Conversion data memory	) 128K words
	Base address (jumper selectable)

3. INSTALLATION

3.1 JUMPER SETTINGS

3.1.1 GENERAL

Install the printed circuit board jumpers in accordance with Appendix A and the component layout diagram, Appendix C.

3.1.2 BASE ADDRESS

The word address can be selected from 080000 to F80000 (hex) defined by the five jumpers J12 – J16. Insertion of a jumper selects a logical 0 at that position. Thus if J12 – J15 are made and J16 is left open, base address 800000 is selected.

3.1.3 INTERRUPT ACKNOWLEDGE PRIORITY

Interrupt priority from 0 to 7 can be selected with J17 – J19. Insertion of a jumper selected a logical 0. If J18 – J19 are made and J17 is left open priority level 1 is selected. This priority corresponds to selection of IRQ1 in the following paragraph.

3.1.4 INTERRUPT REQUEST

The interrupt request line to be driven by the interrupt is selected by inserting one of jumpers J20 – J26. Insertion of J20 selects IRQ1*.

3.1.5 ANALOG INPUT VOLTAGE RANGE

The input voltage range is selected using jumpers J1 – J4. Jumper J5 selects straight binary conversion or two's complement (sign extended to sixteen bits).

3.1.6 INTERNAL CLOCK

Jumpers J6 and J7 select the internal clock frequency to be used. In current versions J7 (8MHz) is selected.

3.1.7 SEQUENCER CLOCK PHASE

The jumpers J8 and J9 select the phase relationship between the clock signals of the logic sequencers and their set–up buffer registers. The jumper is factory set and should be maintained at the current setting.

3.1.8 TRIGGER TIMING MONOSTABLE

In situations where only one channel is used at the highest clock rate to ensure greatest trigger accuracy the timing monostable can be enabled by making J10.

3.1.9 POST–TRIGGER MONOSTABLE

Jumper J11 is provided for test purposes. it is normally left open. When made, the jumper disables the TRIGSEQB monostable. This monostable resets the memory address counter when the board is triggered so that the post–trigger buffer commences at its zero address. Therefore when the jumper is made conversions are stored in the post–trigger buffer commencing at the current address plus the post–trigger offset.

3.2 LINK SETTINGS

3.2.1 GENERAL

The printed circuit board link settings are shown in Appendix B. They are generally factory set and need not be changed for normal operation.

3.2.2. DATA LOGIC

Link LK1 determines the sense of the ADC data. when pins 2 and 3 are linked, the ADC provided positive logic. Data is complemented when pins 1 and 2 are linked.

3.2.3 OFFSET ADJUSTMENT POTENTIOMETER VOLTAGE

Link LK2 allows either a positive or negative bias voltage to be connected to the front end amplifiers according to which type of amplifier is used. Normally, OP64 amplifiers are used which require a negative voltage and pins 2 and 3 are connected.

3.2.4 CHANNEL 1 AND 4 ISOLATION

Link LK3 isolates sample and hold channels 1 and 4 for test purposes. Opening the link across pins 1 and 2 isolates sample/hold channel 1. Opening the link across pins 3 and 4 isolates sample/hold channel 4.

3.2.5 MISSED TRIGGER

Hardware logic is included for detection of missed triggers. However, in current versions this has not been implemented in firmware and link LK4 is not used.

3.2.6 ADC AMPLIFIER

Link LK5 connects the output of the multiplexer to the input of the ADC non–inverting amplifier. It is normally made.

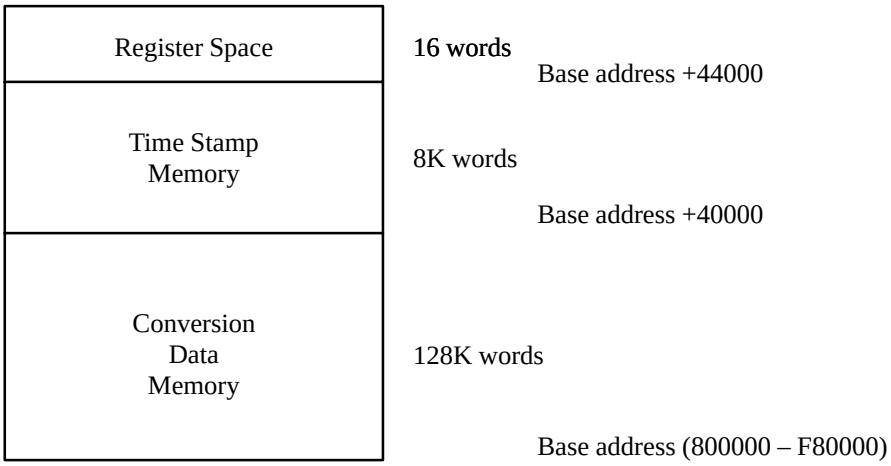
3.2.7 HOLD TIMING

Link LK6 is normally made by connecting pins 1 and 2.

4. OPERATION

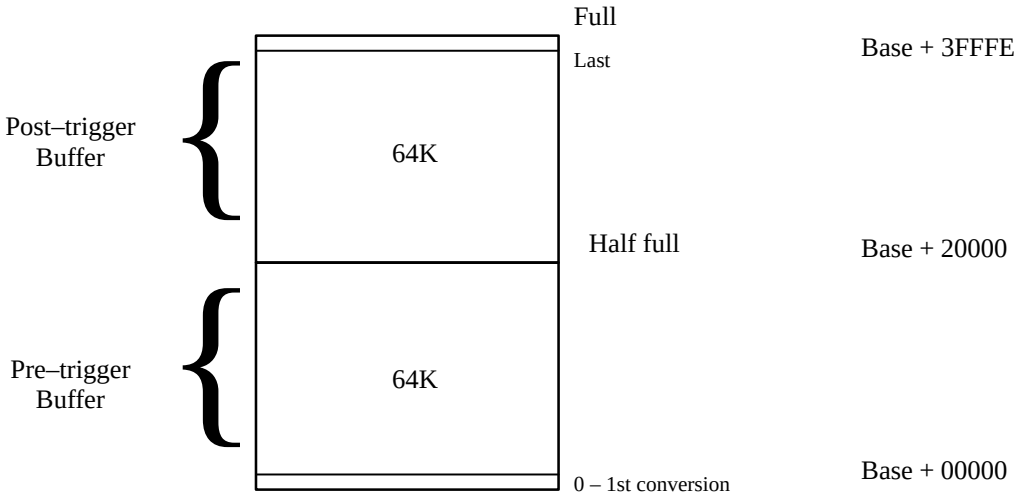
4.1 MEMORY MAP

The conversion data memory occupies a space of 128K words starting at the base address. A memory of 8K words resides above this followed by a further 16 words used for control and status registers. The memory map is shown below:

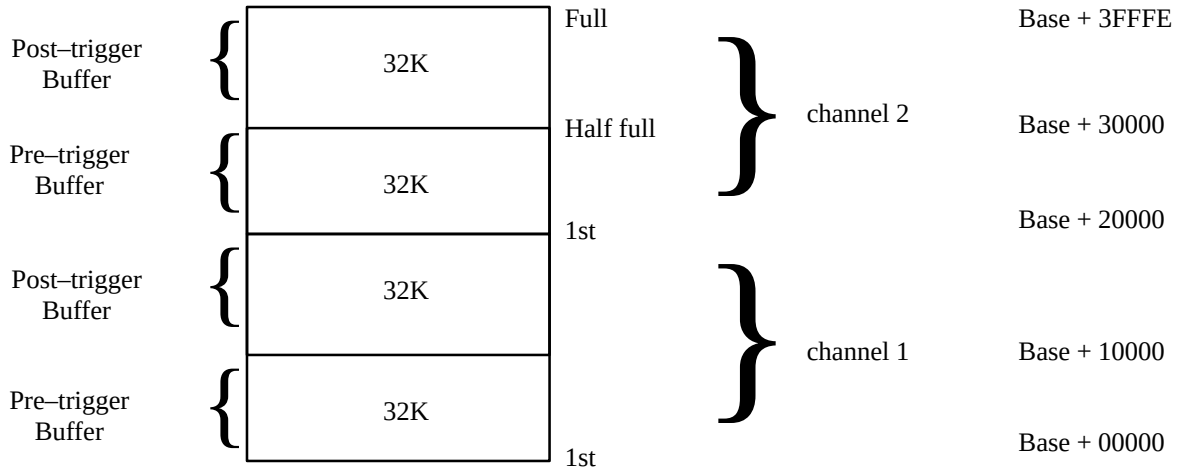


4.2 CONVERSION DATA MEMORY

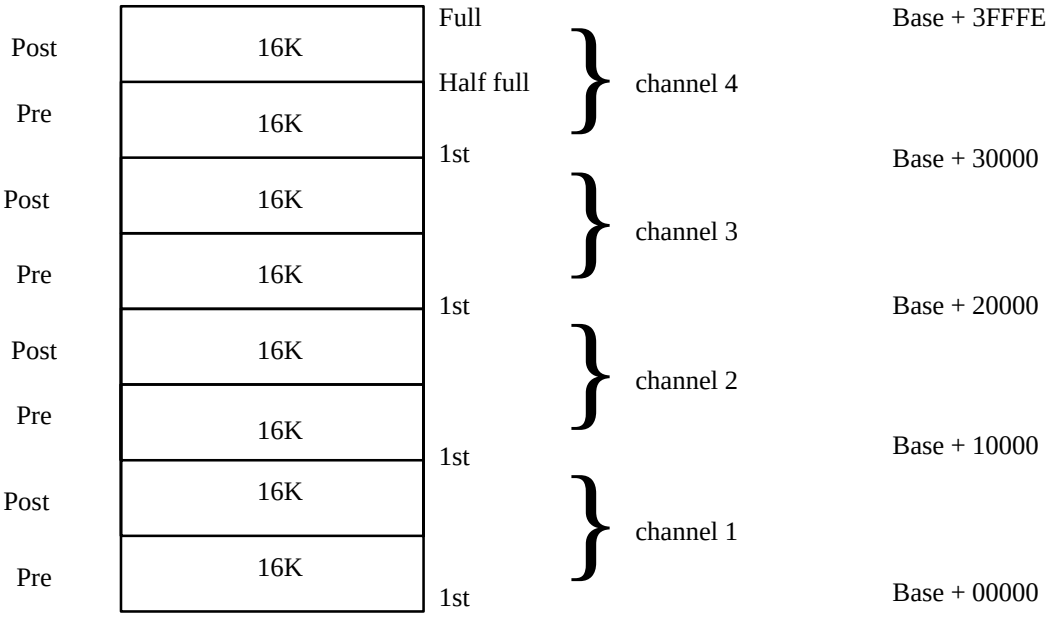
For a single channel (channel 1) the memory is totally allocated.



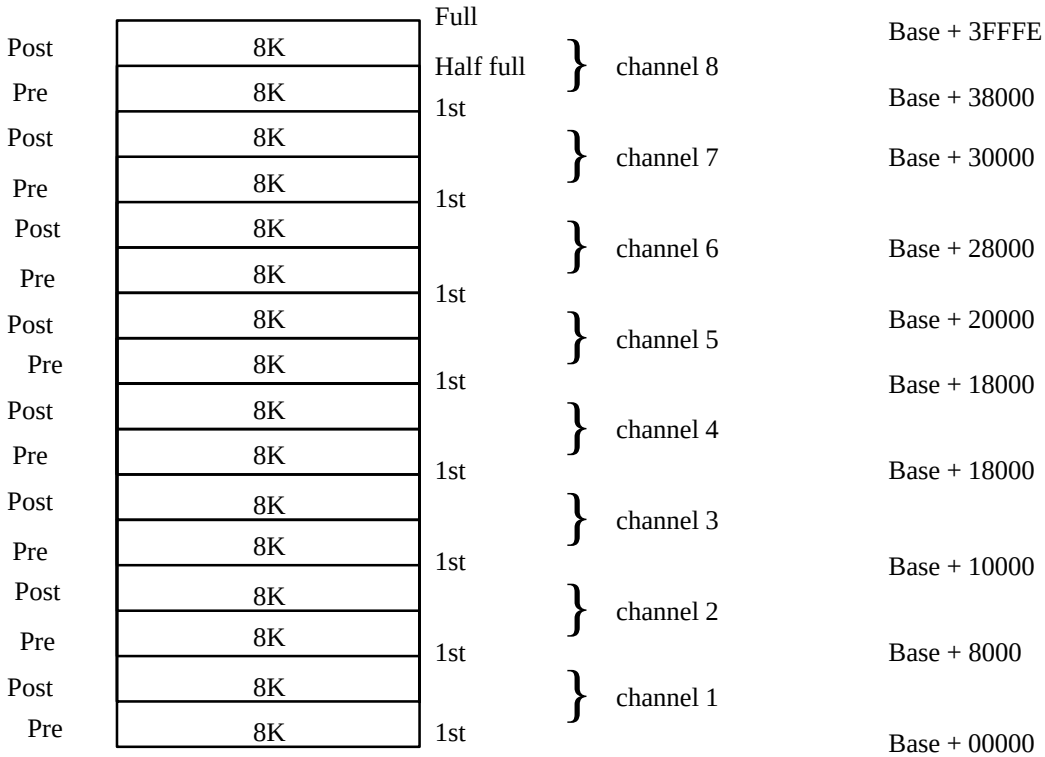
For two channels (channels 1 and 2) the memory is divided into two segments thus:



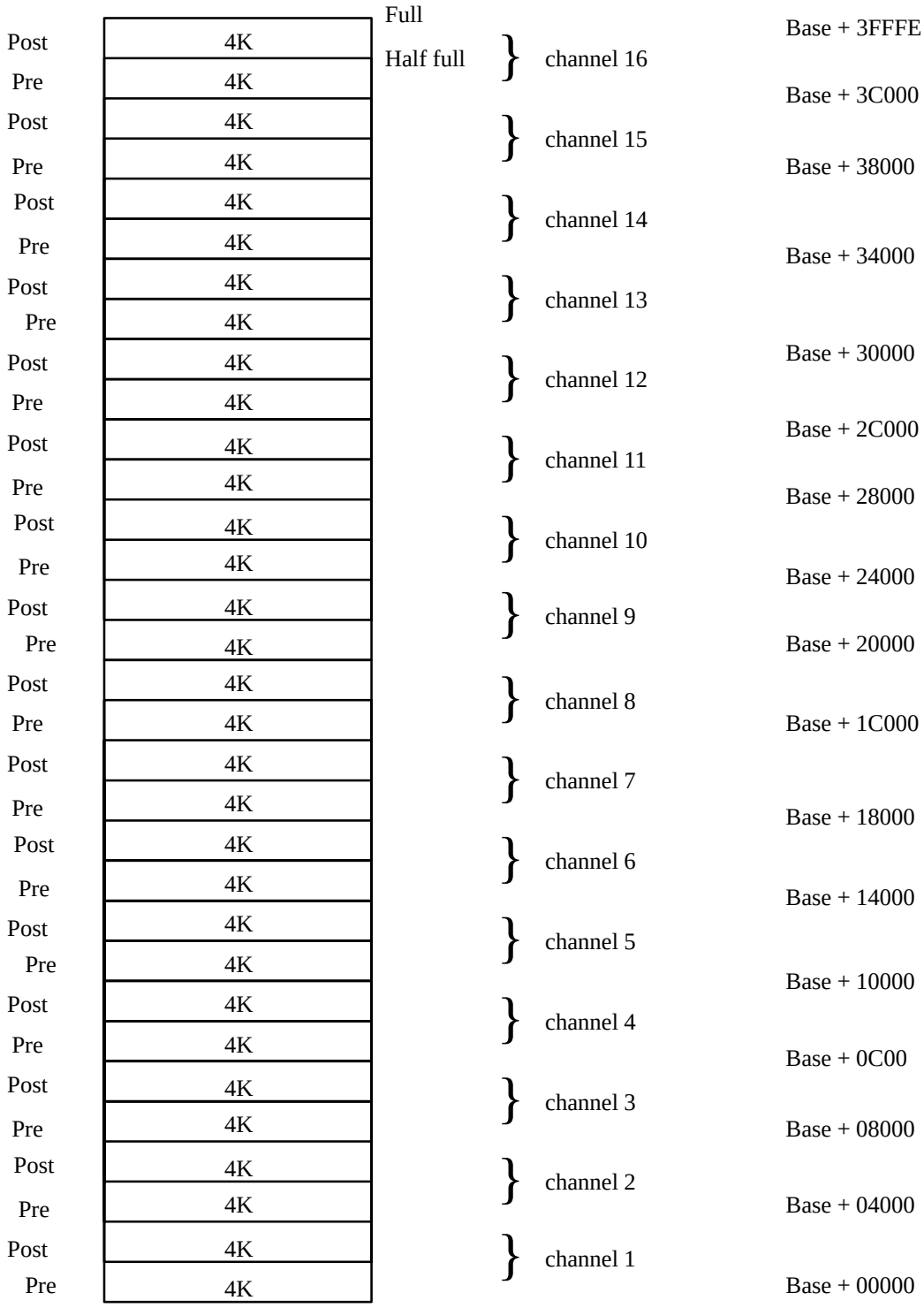
For four channels (channel 1 – 4) the memory is allocated as below:



For eight channels (channels 1 – 8) there are 8 segments:



For sixteen channels (channels 1 – 16):



4.3 TIME STAMP MEMORY

When the board is triggered the address of the next location in memory to be updated is stored in the time stamp memory pointed to by the Event Counter. thus after initialisation and start up the first recorded time stamp will be stored in location zero of the time stamp memory. The next will be stored in location 1 and so on up to a maximum of 8K values. If this is exceeded wrap–around will occur and the next time stamp will be stored in location zero.

Location zero resides at the Base Address (BA) plus 40000 bytes. The time stamp memory occupies from BA + 40000 to BA + 43FFE.

4.4 REGISTER SPACE

The control and status registers of the board occupy 16 words at the top of the memory area. These are allocated as follows:

BYTE ADDRESS	REGISTER	READ/WRITE
BA +4401E	Reserved	–
BA +4401C	Reserved	–
BA +4401A	Reset memory address pointer to zero	W
BA +44018	Module descriptor	R
BA +44016	Upper/lower trigger threshold	W
BA +44014	Far post–trigger frequency	W
BA +44012	Near post–trigger frequency	W
BA +44010	Pre–trigger frequency	W
BA +4400E	Far post–trigger clock count	W
BA +4400C	Near post–trigger clock count	W
BA +4400A	No. of channels/segment size	W
BA +44008	ADC memory address pointer MS	R
BA +44006	ADC memory address pointer LS	R
BA +44004	Mask and control	R/W
BA +44002	Interrupt status	R/W
BA +44000	Interrupt vector	* W

* Read during the IACK cycle.

4.5 DATA FORMATS

4.5.1 INTERRUPT VECTOR

Data Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Write D16	F								Vector							

Bits 00 – 07 – 8 bit vector.

Bits 08 – 15 – all 1s if 8 bit vector required.

4.5.2 INTERRUPT STATUS

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
B													EE	HF	F

Write D16 Bits 0–2

Read D16 bits 0–2, 15

B – Busy. Trigger has occurred and the board is in the post–trigger phase.

EE – End of event. Trigger has occurred and the board is in the post–trigger phase has been completed, i.e. both near post–trigger and fast post–trigger counts have finished.

HF – Half full. conversion data has been stored in the lower half of memory and the halfway boundary has been crossed.

F – Full. The memory has been completely filled. Unless continuous mode is set, conversions will be disabled.

Status bits 0–2 can be reset by writing 0s to each bit. The Busy bit can only be read. A logic 1 indicates that the condition read is true. Eg. if B=1 the triggered event is busy.

4.5.3 MASK AND CONTROL

Data Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Write/Read D16	ST	XMI	XMO	IP	XC	AT2	AT1	AT0	ARM		C	XT	TI	EE	EH	EF

EF – Enable ’Full’ interrupt. The top conversion data memory location has been overwritten by the ADC.

EH – Enable ’Half Full’ interrupt. The halfway point of the highest memory sector has been reached.

EE – Enable ’End of event’ interrupt. The near post–trigger and far post–trigger phase have been completed and the ADC is in the pre–trigger phase.

TI – Trigger Internal. Trigger from channel 1 amplifier.

XT – Enable external digital trigger via the front panel co–axial socket and enables software triggers.

C – Continuous mode. Digitisation continues regardless of the status of the ’Full’ flag. If ’Full’ is set memory storage ’wrap–around’ will occur.

ARM – Digitisation is enabled when set.

AT0 – 2; Three bit analog trigger code determines mode of trigger – see Appendix D for details of usage.

These codes are not implemented in early versions of the TRIGGER PLD.

XC – External clock. The basic clock rate is derived from the signal applied to the ’Clock In’ socket and the internal clock is inhibited. The settings of the trigger frequencies (4.5.6) define the frequency division.

IP – Inhibit pre–trigger clocking. Digitisation will not occur until the board is triggered.

XMO – 2 bit code reserved for memory paging on future versions of the VTD 1612.

ST – Software trigger. A write Mask and Control transfer with bit 15 will trigger an event. Busy will be set until the end of the end of the event.

4.5.4 ADC Memory Address Pointer

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LS Address Data																
Read Memory Address D16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MS Address Data	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Read Memory Address D16	X	X	X	X	X	X	X	X	23	22	21	20	19	18	17	16

The memory address counter is a 24 bit address counter. The 128K word memory is addressed by bits 00 to 16. If continuous is set bits 17 to 23 give an indication of how many times memory 'wrap–around' has occurred.

The address bits 00 – 16 are used according to the memory segment allocation:–

No. of channels	Sector size	Memory address bits	Segment address bits
16	8K	00–12	13–16
8	16K	00–13	14–16
4	32K	00–14	15–16
2	64K	00–15	16
1	128K	00–16	–

Note: bits 08–15 of the MS data will be set to all 1s.

The memory address read buffer has a latching arrangement such that data cannot change during a read. This has two side effects. After initialisation the memory address must be read twice to obtain the current zero value of the address counter.

After end of event when the address passes from post–trigger to the pre–trigger buffer the address must be read twice for the first read. This proves useful in that it can be checked that the end of post–trigger address is reached and then the corresponding address in the pre–trigger buffer is pointed to for the second read.

The memory address read buffer is updated at the end of a channel scan. Therefore, the appropriate segment address bits are zero and the address points to the next location to be updated.

4.5.5 NUMBER OF CHANNELS/SEGMENT SIZE

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Write D16	Not used								S3	S2	S1	S0	C3	C2	C1	C0

C0 Code 1 : Sample channel 1

C1 Code 2 : Sample channel 1 and 2

C2 Code 4 : Sample channel 1 – 4

C3 Code 8 : Sample channel 1 – 8

Code F : Sample all 16 channels

S0 Code 1 : 4K pre–trigger buffer

S1 Code 2 : 8K pre–trigger buffer

S2 Code 3 : 16K pre–trigger buffer

S3 Code 4 : 32K pre–trigger buffer

Code 5 : 64K pre–trigger buffer

8 – D : Disable the pre–trigger buffer limit – when armed digitisation will continue until 'Full' is set or until disarmed if 'Continuous' is set.

Valid combinations for no. of channels/segment size

1F 16 channels, 4K pre–trigger buffer, 4K post–trigger buffer

28 8 channels, 8K pre–trigger buffer, 8K post–trigger buffer

34 4 channels, 16K pre–trigger buffer, 16K post–trigger buffer

42 2 channel,s 32K pre–trigger buffer, 32K post–trigger buffer

51 1 channel, 64K pre–trigger buffer, 64K post–trigger buffer

8F,9F 16 channels, 8K per channel pre–trigger buffer

88,A8 8 channels, 16K per channel pre–trigger buffer

84,B4 4 channels, 32K per channel pre–trigger buffer

82,C2 2 channels, 64K per channel pre–trigger buffer

81,D1 1 channel, 128K per channel pre–trigger buffer

4.5.5 NEAR AND FAR POST–TRIGGER CLOCK COUNTS

	15	00
Write D16	Count Value	

Count value – ones complement binary value of clock count 0001 to FFFF FFFF (or ones complement of zero value) will set zero clock counts. Eg. if a near post trigger count of 1 and no far post–trigger count are required load FFFE and FFFF respectively.

4.5.6 PRE–TRIGGER, NEAR AND FAR POST–TRIGGER FREQUENCIES

		04	03	02	01	00
Write D16	Don't care	F4	F3	F2	F1	F0

F0 5 bit code which defines the frequency division.

F1 for the internal clock.

F2 Code 2 = 1MHz, Code 3 = 500KHz, Code 4 = 250KHz.

F3 etc. to Code 31 = 1.86 x 10^{-3} Hz.

F4 Code 0 and 1 provide the full or half clock frequencies when an external clock is used.

4.5.7 UPPER/LOWER TRIGGER THRESHOLD

L0 – L7 – 8 bit code determines lower trigger threshold 0 to –10V.

U0 – U7 – 8 bit code determines upper trigger threshold 0 to +10V.

When the analog trigger is implemented these two values determine the upper and lower voltage levels for the analog trigger criteria

eg. if L0 – L7 is set 7F the lower level would be –5V
if U0 – U7 is set 3F the upper level would be + 2.5V.

4.5.8 MODULE DESCRIPTOR

	15							08	07	06	05	04	03	02	01	00
Read D16	All 1's								D7							D0

D0 – D7 patched code which can be used as a board descriptor.

4.5.9 RESET MEMORY ADDRESS POINTER

A D16 write operation with any data clears the memory address pointer. This is particularly useful in Single Scan mode.

4.5.10 ADDRESS MODIFIER CODES

Codes 39 and 3D are used.

4.5.11 CONVERSION DATA FORMAT

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Read D16					D11											D0

Write D16 is available for testing the memory.

Unipolar

+10V	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
+5V	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bipolar

+10V	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
0V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
–0.005V	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
–10V	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

4.5.12 TIME STAMP DATA FORMAT

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Memory Address up to FFFF															

Read D16
Write D16 is available for testing the memory

4.6 MODES OF OPERATION

4.6.1 TRIGGERED BUFFER MODE

When armed the board scans the selected input channels, digitises the analog values and stores the data in the pre–trigger buffer continuously looping within the memory range of the pre–trigger buffer. A trigger causes the memory address to jump to the start of the post–trigger buffer. Converted values are then stored in this buffer until the near post and far post counts expire. The acquisition is halted with the address pointer set in the pre trigger buffer range.

An example of the set up for this is:–

1. Interrupt Vector		FFC9 (if used)
2. Mask and Control	(external clock 100KHz)	0810
3. No. of channels/segment size		0028 (8 channels)
4. Near post–trigger count	1s complement of:	0C00
5. Far post–trigger count	1s complement of:	0100
6. Pre trigger frequency		0000 (100KHz)
7. Near post–trigger frequency		0001 (50KHz)
8. Far post–trigger frequency		0002 (25KHz)
9. Upper and lower levels	(not used)	FFFF

The board is armed by adding 80 to mask and control. The board will accept an external trigger in the front panel coaxial socket or by software command (add 8000 to mask and control).

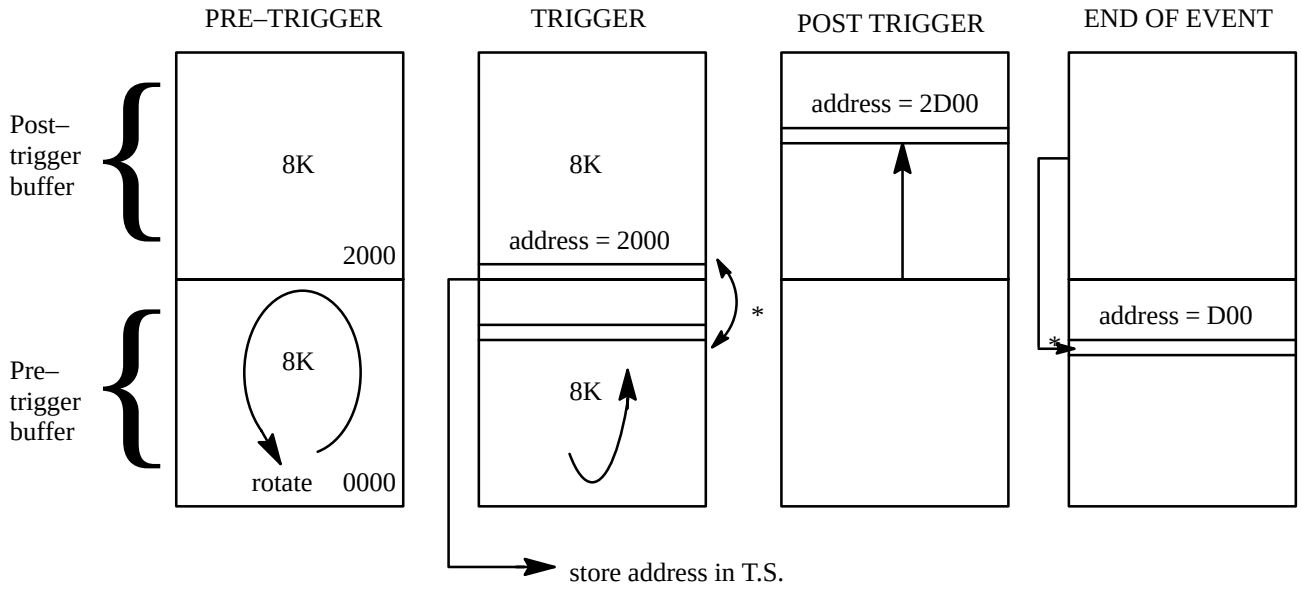
The pre–trigger clock frequency is that of the external clock. Near post frequency will be half of this and far post half again.

When the board is triggered, the Busy LED will be illuminated Half Full and then Full will be illuminated and Busy extinguished in that order.

If the memory address is read twice, the first read will give 2D00 and the second read D00 indicating that scanning has halted with the address set in the pre–trigger buffer.

The first location of the time–stamp memory will hold the memory address pointed to when trigger caused a jump to the post–trigger buffer. Shown diagramatically:–

For channel 1:–



* = jump

At the end of the event the post–trigger buffer will hold the data in sequence from the trigger point and the pre–trigger buffer will hold the pre–trigger data with the oldest recorded data starting at the location stored in location 0 of the time stamp memory, through 1FFF and back to 0000 and up to TS value –1. If pre–trigger clocking is enabled then, at the end of the event, the full flag is set in additin to the end–of–event flag to indicate that the upper half of the memory (above 2000) has been altered.

This example did not use interrupt. If interrupt is required at the end of the event the mask and control register should originally be set to 0814.

If it is required to use the internal clock the mask and control should be be set to 0010 instead of 0810. However the frequency division values should be increased to take into account the increased clock frequency. Typically:–

Pre–trigger frequency	0006 (65KHz)
Near post	0007
Far post	0008

4.6.2 CONTINUOUS MODE

In continuous mode the board continues to sample until disarmed. A typical set up is:–

1. Interrupt Vector	FFC9	
2. Mask and Control	0031	(interrupt full)
3. No. of channels	009F	(16 channels – no limit)
4. Near post–trigger count	XXXX	(don't care)
5. Far post–trigger count	XXXX	(don't care)
6. Pre trigger frequency	0007	(32KHz)
7. Near post frequency	0007	(32KHz)
8. Far post frequency	0007	(32KHz)
9. Upper and lower levels	FFFF (not used)	

The board will interrupt when the 'Full' flag is set but will continue to scan from zero address again.

Normally, in this mode the 'Half full' interrupt would first be enabled. When the board interrupts the 'Half full' status bit would be cleared and disabled and the 'Full' interrupt enabled.

When the board interrupts again the 'Full' status bit would be cleared and disabled and the 'Half full' interrupt re–enabled.

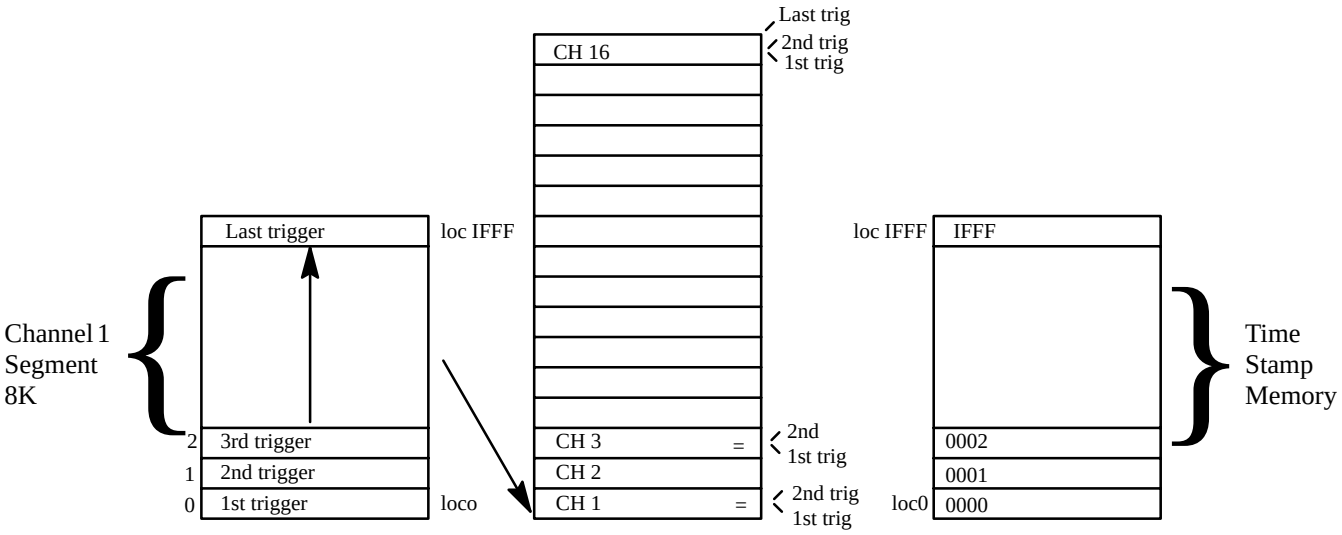
After the 'Half full' interrupt the lower buffer segment of memory would be read while accumulating data in the upper buffer segment. Similarly after 'Full' interrupt the upper buffer segment would be read.

4.6.3 SINGLE SCAN MODE

In this mode the board samples at the trigger rate. An example of a set up is:–

1.	Interrupt Vector	FFC9	
2.	Mask and Control	1014	(single mode)
3.	No. of channels	009F	
4.	Near post–trigger count	0001	(ones complement = FFFE)
5.	Far post–trigger count	0000	(ones complement = FFFF)
6.	Pre trigger frequency	0008	(don't care)
7.	Near post frequency	0008	(don't care)
8.	Far post frequency	0008	(don't care)
9.	Upper and lower levels	FFFF	(not used)

The board is armed by adding 80 to the mask and control register. Each trigger will causes values to be stored in successive locations of the memory until it is full.



Interrupt will occur at the end of each triggered event. The single scan operation can be checked by reading the time stamp memory which will indicate a sequence of incremented values. (From initial conditions 0 – 1FFF).

Variants of Single Scan mode can be achieved by increasing the Near and Far post–trigger count values.

5. CIRCUIT DESCRIPTION

5.1 GENERAL

The circuit is shown in block diagram form in diagram 5.1. The blocks and their related circuit references are shown in the following table.

Table 5.1 Circuit References

NAME OF BLOCK	IC REFERENCE	C.D. PAGE
Internal clock	XTI	2
Rate control	IC52	2
Trigger	IC58	2
Trig in	IC21	2
Trig sw	IC44	2
Dual comparator	IC47/48	2
ULDAC	IC36	2
LLDAC	IC37	2
Analog input amplifiers	ICI–IC16	1
S/H 1–16	IC17–IC20	1
MUX	IC22/24	1
MUX count	IC27	1
S/H bistable	IC21	1
Non–inverting amp	IC25	1
ADC	IC28	1
REG	IC33/34	1
Conversion control	IC26	1
Counter	IC29/31/32	1
Post Trigger Offset	IC122	3
Memory address read buffer	IC66–68	3
Conversion address buffer	IC62/63	3
Fullness detector	IC59	2
FPT freq	IC77	4
NPT freq	IC78	4
PT freq	IC79	4
FPT counter	IC80/81	4
NPT counter	IC84/85	4
Refresh clock	IC51/104	5
Conversion data memory	IC64/65	3
Memory address buffer	IC75/76	3
Event counter	IC69/70	3
Time stamp memory	IC71/72	3
TS address buffer	IC73/74	3
Patch	RN4	4
Module status buffer	IC82	4
Status register	IC53/89	4
Mask control reg	IC90/91	4
Int vector reg	IC96/97	4
VMEbus control	IC106	5
Selector switch	J20–26	5
Data buffers	IC113/114	6
Arbiter DPCON	IC110	5
Command decode	IC107–109	5
Address decode	IC86/101/103	5
Base address	IC102	5
Base address selector	J12–J16	5
Add buffer	IC98–100	5
Interrupt priority	IC105	5
Priority selector	J17–19	5
Power Supplies	IC116	6
Indicator driver	IC60	2
Front Panel skts	C01–05	2

5.2 OUTLINE

5.2.1 ANALOG SAMPLING

The outputs from the sixteen differential amplifiers are sampled and held when the S/H bistable is set by CLKHOLD and then multiplexed into the input of the non inverting amplifier which amplifies the signal to be compatible with the full–scale input of the ADC. (The analog signals are initially attennuated by 50% to be compatible with the 5V max signal capability of the sample and hold amplifiers).

Conversion is initiated by the START signal. At the end of conversion the ADC register is strobed to store the conversion data and the CLKCONV signal requests access to the internal tri–state data bus. When it is granted access, the conversion address buffer is gated to address the conversion data memory, the output of the ADC data register is enabled and the data gated onto the bus is written to the memory.

5.2.2 CONVERSION CONTROL

The ADC conversion timing, multiplexer scanning and memory addressing are controlled by the conversion control sequencer (CONBCON) and the conversion address counter. On receipt of STSCAN the sequencer initialises HOLD and provides a series of clock pulses which step the multiplexer counter, initiate conversion, clocking the data into the buffer register and incrementing the memory address once the data has been written to memory. The end of sequence is controlled by a status signal from the conversion address counter to the sequencer (SEG LIM) which is determined by the number of channels programmed to be scanned.

5.2.3 SAMPLING RATE CONTROL

There are three sampling phases pre–trigger, near post–trigger, far post–trigger. The sampling rate of each phase can be programmed by a five bit code which controls the division of the basic clock frequency. These codes are held in registers PT freq, NPT Freq, and FPT freq. Their outputs are gated to the frequency divider under control fo the RATECON sequencer. The number of post–trigger samples are controlled by the NPT Counter and FPT Counter. These contain buffer registers which hold the number of counts and transfer them to counters when the board is triggered. Each sample clocks the relevant counter until overflow occurs. The rate control circuit starts in pre–trigger mode. When triggered the near post–trigger frequency and counter are enabled. When overflow from the near post counter is received the sequencer commences the far post–trigger phase and enables the relevant frequency and counter registers. When overflow is received from the far post counter end of event is signalled back to the trigger circuit and the pre–trigger phase is entered once again. The sampling rate may be derived from an internal oscillator or from an externally supplied pulse train determined by MC11 and gate IC30.

5.2.4 ADDRESS COUNTER

The conversion address counter provides the scan number address and memory segment number address combined to address the conversion address memory and if continuous mode is programmed, counts the complete number of memory scans in bits 18 to 24. (Bits 1 to 17 address the memory).

When the board is triggered the post–trigger offset PAL circuit introduces an offset equal to half the address space into the memory address so that data is acquired into the upper half segment of the memory.

The fullness detector provides 'Half full' and 'Full' signals according to the state of the memory address. 'Half full' occurs when the half segment boundary is crossed and 'Full' is set when the top most location has been addressed in the continuous mode. The memory address is read out onto the internal bus and thence to the VMEbus by enabling the memory address read buffer.

5.2.5 TIME STAMP

Each time the board is triggered the current memory address is stored at the location in the time stamp memory addressed by the event counter. At the end of the event this counter is incremented to point at the next location. When a time stamp cycle is requested the arbiter grants control of the data bus the LS memory address is read onto the data bus and written to the time stamp memory. The time stamp memory can be read via the VMEbus using the relevant address gated via the VME address buffer.

5.2.6 INTERRUPTS

The interrupt status register comprises the Full, Half full and End of event flags. These are And gated with corresponding mask bits in the control and mask status register. The resultant signals are Or gated to form a single interrupt request. This is connected to one of the lines IRQ 1–7* as determined by the interrupt request selected switch. When the master responds with IACK at the correct priority level the interrupt vector enable signal gates the interrupt vector stored in the interrupt vector register onto the data bus. The interrupt is reset by clearing the appropriate interrupt status bit which can be determined by reading the status. Resetting the interrupt mask bits would also clear the interrupt request.

5.2.7 VMEBUS CONTROL

Access to/from the VMEbus is controlled by this sequencer. It requests access to the internal data bus by hand shaking with the arbiter sequencer. When the access is granted the appropriate VMEbus address is decoded and the selected register clocked or enabled onto the bus.

5.2.8 VMEBUS ADDRESS DECODE

The VME address is compared with the base address jumper setting. If there is a match the address and command decoders are enabled for the duration of the VME cycle.

5.2.9 ARBITRATION

The DPCON sequencer performs arbitration of the various requests for use of the internal data bus. It also controls the refresh of the conversion data memory.

Four requests are made:–

TS store – store the time stamp.

REFIN – refresh.

CCKCONV – store conversion data.

VMEREQ – VME cycle.

5.2.10 POWER SUPPLIES

The $\pm$ 15V supplies for the ADC and non–inverting amplifier are provided by a DC–DC converter supplied by +12V.

5.3 PROGRAMMED DEVICES

5.3.1 DEVICES USED

Two types of programmed device are used on the board. The first, a PAL 18P8 is a programmable array which provides combinatorial logic. The second a, PLS 159, is a programmed logic sequencer which is used as a state counter, control sequencer, and software programmed counter.

5.3.2 IC26 CONBCON – PLS159

PIN 1	INPUT	CLK8M	8MHz clock.
PIN 2	INPUT	/EOC	Goes low at the end of ADC conversion.
PIN 3	INPUT	/ENFPTF	Low during the far post–trigger phase.
PIN 4	INPUT	/ENNPTF	Low during the near post–trigger phase.
PIN 5	INPUT	/ENPTF	Low during the pre–trigger phase.
PIN 6	INPUT	/CLRCS	Low when conversion accepted by the memory.
PIN 7	INPUT	/STSCAN	Low initiates a scan and conversion sequence.
PIN 8	INPUT	MC12	Single scan mode, inhibits pre–trigger mode.
PIN 9	INPUT	/SEGLIM	Low indicates end of scan.

PIN 10	INPUT	GND	
PIN 11	INPUT	GND	Enable outputs.
PIN 12	OUTPUT	/CLMUX	Clears multiplexer address and SCANBUSY.
PIN 13	OUTPUT	/CLKCONV	Clocks ADC data into buffer and requests memory write cycle.
PIN 14	OUTPUT	/CLKCNVA	Clocks the memory counter.
PIN 15	OUTPUT	/TRISEQA	Allows memory address to increment.
PIN 16	OUTPUT	/TRISEQB	Low enables POSTOFFS and clears memory address.
PIN 17	OUTPUT	/CKMXSCN	Allows /CLKCNVA to increment channel address when low.
PIN 18	OUTPUT	/ENABLE	Enables ADC data output.
PIN 19	OUTPUT	/CLKMUX	Increments misc. counter and starts conversion.
PIN 20	INPUT	VCC	

5.3.3 IC29, 31, 32 MEMORY ADDRESS COUNTER PLS159s

CA00 – CA23 Outputs memory address.
CA13 – CA16 Outputs have special significance (channel number).

NOCH 1	INPUT)	
NOCH 2	INPUT)	No. of channels (F=16)
NOCH 4	INPUT)	
NOCH 8	INPUT)	
16WS	INPUT)	
32WS	INPUT)	Buffer size (4K – 64K)
64WS	INPUT)	
128WS	INPUT)	
/RESET	INPUT	Reset counter to 0 when low (all outputs high).

5.3.4 IC101 ADDRESS SELECT PAL18P8

/VALID = MESPACE + TSPACE + RGSPACE
/MESPACE = /A18
/TSPACE = A18*/A17*/A16*/A15*/A14
/RGSPACE = A18*/A17*/A16*A15*A14*/A13*/A12*/A11*/A10*/A09*/A08*/A07*/A06*/A05

5.3.5 IC103 AM PAL18P8

PIN 1	INPUT	/AS	Address strobe.
PINS 2–7	INPUTS	AM0–AM5	Address modifier code.
PIN 8	INPUT	/LWORD	Long word cycle.
PIN 9	INPUT	/VALID	Correct address selected.
PIN 11	INPUT	/BASEADDRESS	Boards address selected.
PIN 12	OUTPUT	ADDROK	Address is correct.

ADDROK = LWORD * VALID * BASE ADDRESS * AM5 * AM4 * AM3 * /AM1 * AM0

5.3.6 IC107 RDDEC PAL18P8

PIN 1–4	INPUTS	BUS ADDRESS A01–A04.	
PIN 5	INPUT	/RGSPACE	Register addressed.
PIN 6	INPUT	/ENEVA	
PIN 7	INPUT	VMECYCLE	VME cycle in progress.
PIN 8	INPUT	/ENAVME	VME cycle enabled.
PIN 9	INPUT	WRITE	VME write cycle.

PIN 11	INPUT	/SYSRST	System reset.
PIN 12	OUTPUT	/RESET	System or programmed reset.
PIN 13	OUTPUT	/WRVEC	Write vector register.
PIN 14	OUTPUT	/WRSTATS	Write status register.
PIN 15	OUTPUT	/RDMODS	Read module status.
PIN 16	OUTPUT	/RDMAMS	Read MS memory address register.
PIN 17	OUTPUT	/RDMALS	Read LS memory address register.
PIN 18	OUTPUT	/RDMASK	Read mask register.
PIN 19	OUTPUT	/RDSTATS	Read status register.

5.3.7 IC108 COMDEC PAL18P8

PIN 1	INPUT	/MESPACE	Memory addressed.
PIN 2	INPUT	/TSPACE	Time stamp memory addressed.
PIN 3	INPUT	/WRMEMO	Write to memory.
PIN 4	INPUT	/WRITS	Write to time stamp.
PIN 5	INPUT	/ENAVME	VME cycle enabled.
PIN 6	INPUT	VMEREQ	VME cycle requested.
PIN 7	INPUT	VME CYCLE	VME cycle granted.
PIN 8	INPUT	/RGSPACE	Register addressed.
PIN 9	INPUT	WRITE	VME write cycle.
PIN 11	INPUT	/SYSRST	System reset.
PIN 12	OUTPUT	/WRMEM	Write to memory (VME or ADC)
PIN 13	OUTPUT	/WRTS	Write time stamp (VME or ADC)
PIN 14	OUTPUT	/BTOA	Data buffer direction counted.
PIN 15	OUTPUT	/ENDATAB	Enable data onto bus.
PIN 16	OUTPUT	/VMEMEMA	Memory addressed by VME.
PIN 17	OUTPUT	/ENTSA	Enable time stamp address.
PIN 18	OUTPUT	/RDTS	Read time stamp.
PIN 19	OUTPUT	/RDMEM	Read memory.

5.3.8 IC109 WRDEC PAL18P8

PIN 1–4	INPUT	A01–A04	VME address bus.
PIN 5	INPUT	/RGSPACE	Register addressed.
PIN 6	INPUT	VMEREQ	VME cycle in requested.
PIN 7	INPUT	VMECYC	VME cycle in progress.
PIN 8	INPUT	/ENAVME	VME cycle enabled.
PIN 9	INPUT	WRITE	VME write cycle.
PIN 11	INPUT	/SYSRST	VME system reset.
PIN 12	INPUT	/WRFPTF	Write far post–trigger frequency.
PIN 13	OUTPUT	/WRNPTF	Write near post–trigger frequency.
PIN 14	OUTPUT	/WRPTF	Write pre–trigger frequency.
PIN 15	OUTPUT	/WRFPTC	Write far post–trigger count.
PIN 16	OUTPUT	/WRNPTC	Write near post –rigger count.
PIN 17	OUTPUT	/WRSEG	Write segment/channel register.
PIN 18	OUTPUT	/WRMASK	Write mask/control register.
PIN 19	OUTPUT	/WRTHRES	Write threshold register.

5.3.9 IC106 VME PLS159

PIN 1	INPUT	CLK8M	8MHz clock
PIN 2	INPUT	PRIORITY OK	Interrupt priority OK.
PIN 3	INPUT	IACKIN	VME interrupt acknowledge.
PIN 4	INPUT	DS1	Data strobe 1
PIN 5	INPUT	DS0	Data strobe 0.
PIN 6	INPUT	ADDRESS OK	Board addressed correctly.
PIN 7	INPUT	ENABLEVME	VME cycle granted.
PIN 8	INPUT	INTREQ	Interrupt request.
PIN 9	INPUT	SYSRST	VME system reset.

PIN 12	OUTPUT	WRISTB	Write strobe.
PIN 13	OUTPUT	INTVEN	Interrupt vector enable.
PIN 14	OUTPUT	VMEREQ	Request arbitration for internal bus.
PIN 15	OUTPUT	VMECYCLE	VME cycle in progress.
PIN 16	OUTPUT	IACKOUT	Daisy chain 1ACK to next device.
PIN 17	OUTPUT	DTACK	Generate DTACK.
PIN 18	OUTPUT	BERR	Not used.
PIN 19	OUTPUT	IRQ	Not used.

5.3.10 IC110 DPCON PLS159

PIN 1	INPUT	CLK8M	8MHz clock
PIN 2	INPUT	TSSTORE	Request for time stamp write cycle.
PIN 3	INPUT	CLKCONV	Request to write conversion to memory.
PIN 4	INPUT	RFRSH	Request for memory refresh cycle.
PIN 5	INPUT	VMEREQ	Request for VME cycle.
PIN 6	OUTPUT	CLTS	Clear time stamp request.
PIN 7	OUTPUT	CHIPEN	Memory access.
PIN 8	OUTPUT	ENEVA	
PIN 9	INPUT	VMECYCLE	VME cycle in progress.
PIN 12	OUTPUT	/ENABLEVME	Handshake back to VME request.
PIN 13	OUTPUT	/ENAVME	Enable VME access.
PIN 14	OUTPUT	/CLRCS	Acknowledge end of memory write.
PIN 15	OUTPUT	/CKCNVAD	Refresh cycle.
PIN 16	OUTPUT	/WRTS	Write time stamp.
PIN 17	OUTPUT	/ENCNVAD	Enable conversion address.
PIN 18	OUTPUT	/WRMEM	Write to memory
PIN 19	OUTPUT	/ENACONV	Enable conversion data to bus.

5.3.11 IC52 RATECON PLS159

PIN 1	INPUT	CLK8M	8MHz clock
PIN 2	INPUT	EVNTTRI	Trigger request.
PIN 3	INPUT	/FPTCOF	Far post trigger count overflow (0).
PIN 4	INPUT	/NPTCOF	Near post trigger count overflow (0).
PIN 5	INPUT	MC05	Continuous – full flag is ignored.
PIN 6	INPUT	MC07	Arm – clock in pre–trigger mode.
PIN 7	INPUT	/FULL	Full flag set.
PIN 8	INPUT	HICK	High frequency sample clock.
PIN 9	INPUT	LOCK	Low frequency sample clock.
PIN 12	OUTPUT	/CLRDIV	Clear frequency divider.
PIN 13	OUTPUT	/FLGSTR	Clock half full and full flags.
PIN 14	OUTPUT	/ENPTF	Enable pre–trigger frequency.
PIN 15	OUTPUT	/ENNPTF	Enable near post–trigger frequency.
PIN 16	OUTPUT	/ENFPTF	Enable far post–trigger frequency.
PIN 17	OUTPUT	/EOEVNT	End of triggered event handshake.
PIN 18	OUTPUT		Not used.
PIN 19	OUTPUT	/STSCAN	Start channel scan and conversion.

5.3.12 IC58 TRIGGER PLS159

PIN 1	INPUT	CLK8M	8MHz clock
PIN 2	INPUT	UTHRESH	Upper threshold level trigger.
PIN 3	INPUT	LTHRESH	Lower threshold level trigger
PIN 4	INPUT	LOGITRIG	Logic trigger.
PIN 5	INPUT	EOEVNT	End of event handshake returned from RATECON.
PIN 6	INPUT	ENEXTRIG	MC04 enables logic trigger.
PIN 7	INPUT	TRIMI	Trigger mode MC08.
PIN 8	INPUT	TRIM2	Trigger mode MC09.
PIN 9	INPUT	TRIM 4	Trigger mode MC10.

PIN 12	OUTPUT	/CLOG	Clear logic trigger.
PIN 13	OUTPUT	/EVNTCLK	Request time stamp cycle.
PIN 14	OUTPUT	/MISDTRI	Not used.
PIN 15	OUTPUT	/EVNTTRI	Event trigger. Starts post–trigger phase.
PIN 16	OUTPUT	/CLOW	Clear lower threshold level trigger.
PIN 17	OUTPUT	/CLUP	Clear upper threshold level trigger.
PIN 18	OUTPUT	/BUSY	Low when event is in progress (post–trigger).
PIN 19	OUTPUT	/TRIG	Trigger pulse.

5.3.13 IC59 FULLNESS DETECTOR 18P8

PIN 1	INPUT	CA17	Memory address counter bit 17.
PINS 2–7	INPUTS	/CA16M–/CA11M	Modified address count bits from POSTOFFS
PINS 8–9	INPUTS	CA10 CA09	Memory address counter bits 10 and 09.
PINS 11,12,13,18	INPUTS	NOCH8–NOCH1	Number of channels programmed.
PIN 19	INPUT	/FLGSTR	Clock flags signal from RATECON.
PIN 16	OUTPUT	/SETHF	Clock half full flag.
PIN 17	OUTPUT	/SETFF	Clock full flag.

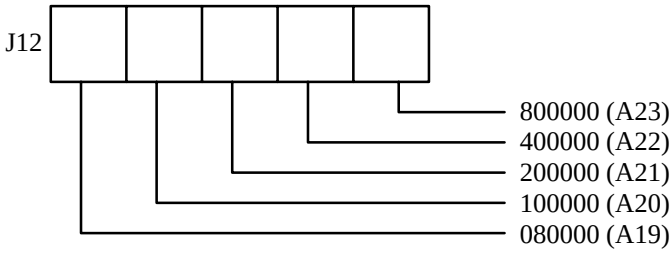
5.3.14 IC122 POSTOFFS 18P8

PINS 1–6	INPUTS	CA16–CA11	Memory address counter bits 11–16.
PINS 7–11	INPUTS	16WS–128WS	Sector size.
PIN 12	INPUT	/TRISEQB	Post trigger.
PIN 13	INPUT	MC12	Supplies pre–trigger operation.
PINS 14–19	OUTPUTS	/CA11M–/CA16M	Modified address counter bits (post–trigger offset).

APPENDIX – A

VTD 1612 – JUMPER SETTINGS

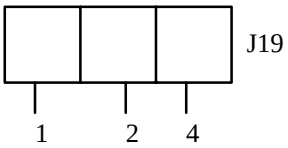
BASE ADDRESS J12 – J16



JUMPER OPEN = LOGIC 1.
JUMPER CLOSED = LOGIC 0.

e.g. for address 900000 insert J12, J14, J15

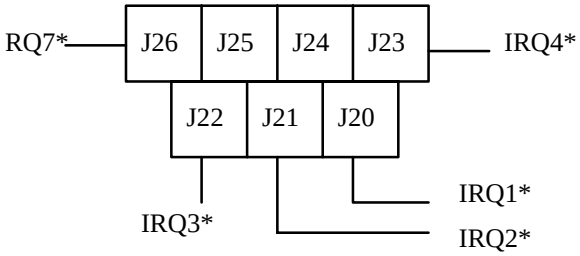
INTERRUPT ACKNOWLEDGE PRIORITY J17–J19



JUMPER OPEN = LOGIC 1.

e.g. for priority 1 insert J18, J19

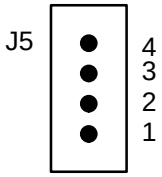
INTERRUPT REQUEST J20–J26



JUMPER CLOSED SELECTS IRQX*.
(insert only one at a time).

ANALOGUE INPUT VOLTAGE RANGE J1–J5

VOLTAGE RANGE	J1	J2	J3	J4	J5
0 to –5V		1		1	2 – 3
0 to –10V				1	2 – 3
0 to +10V	1			1	2 – 3
+/– 5V		1	1		1 – 2 3 – 4
+/– 10V			1		1 – 2 3 – 4



Notes: 1 = JUMPER INSERTED.
J5 1 – 4 left to right, J5 2 – 3 straight binary, J5 1 – 2, 3 – 4 2s complement.

INTERNAL CLOCK J6, J7

J6 closed 16MHz (for future use)) leave as set.
J7 closed 8MHz (normal connection))

SEQUENCER CLOCK PHASE J8, J9

J8 closed in phase (select on test)) leave as set.
J9 closed 180^{o} shift (select on test))

TRIGGER TIMING MONOSTABLE J10

Normally open.

POST TRIGGER MONOSTABLE J11

Normally open.

APPENDIX – B

VTD 1612– LINK SETTINGS

LINK	SETTING	
LK1	2 – 3	ADC data positive logic (1–2 complements).
LK2	2 – 3	Connects –12V to OP64 offset adjust wiper.
LK3	1 – 2	Normally made (isolates S/H 1).
	3 – 4	Normally made (isolates S/H 4).
LK4	1 – 2	Missed trigger not used.
LK5	made	Connects MUX to ADC amplifier.
LK6	1 – 2	Normally made (hold on CLKHOLD).

APPENDIX D

VTD 1612 – USE OF ANALOGUE TRIGGER

PRE–REQUISITES

1. IC58 should be 'TRIGA V2'.
2. Inverter IC51/1 should be by–passed.
3. Comparators IC47 and IC48 should have 68K resistors fitted between pins 2 and 7.
4. Issue 3 boards should be to modification status 4.

TRIGGER PHASE

The trigger amplifier IC40 is connected such that its positive input is connected to pin 36 and its negative input to pin 17. This is the opposite phase from channels 1 to 16 (+ odd pins – even pins)., Therefore, this phase difference exists between external trigger and channel 1 trigger if the connection sense is maintained.

The analogue trigger code of bits 8 – 10 of the mask and control register are then:–

Bit	10	9	8	Ext. Trigger	Ch. 1 Trigger
	0	0	0	No analogue trigger	No analogue trigger
	0	0	1	Positive slope	Negative slope
	0	1	0	Negative slope	Positive slope
	0	1	1	Pos. slope, neg. hysteresis	Neg. slope, pos. hysteresis
	1	0	0	Neg. slope, pos. hysteresis	Pos. slope, neg. hysteresis
	1	0	1	Window trigger	Window trigger

If pins 17 and 36 are reversed then external triggering and channel 1 triggering will have the same phase.

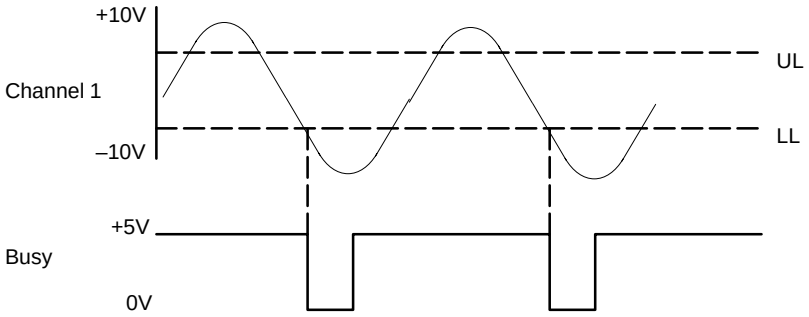
UPPER AND LOWER TRIGGER LEVELS

The positive level is controlled by bits 0 – 7.
The negative leve is controlled by bits 8 – 15.

EXAMPLES

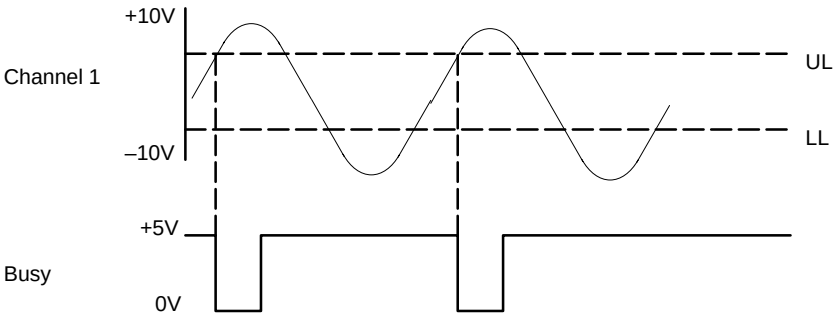
Threshold register set to 8080 (halfway levels).

Code 01



(eg: mask & control 1128)

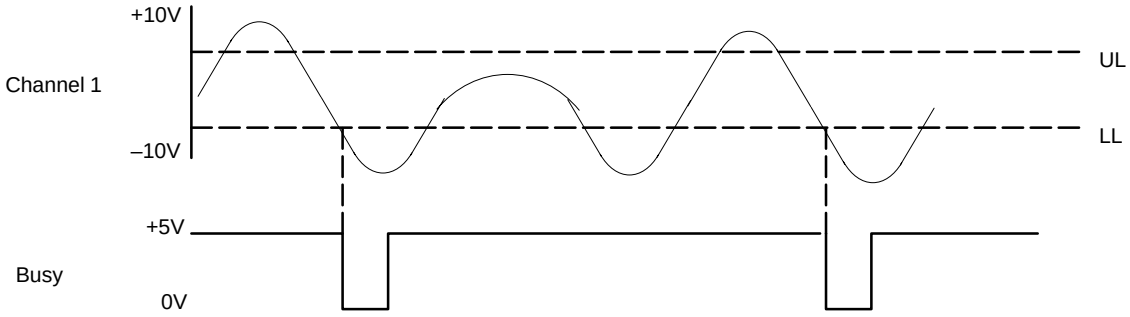
Code 02



(eg: mask & control 1228)

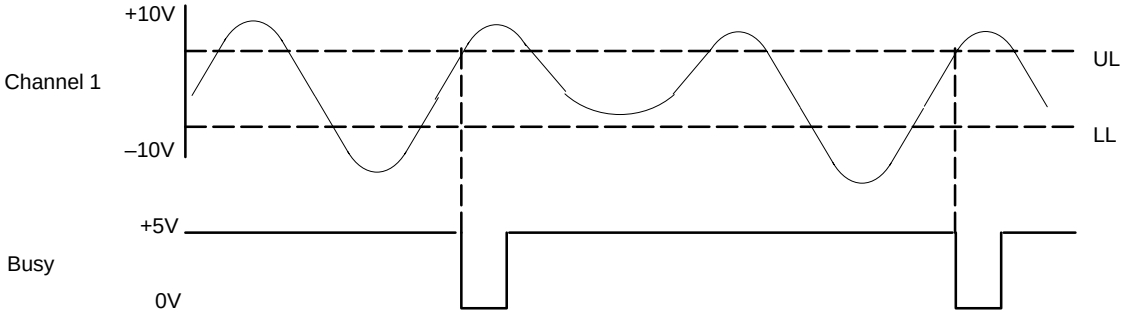
Code 03

(eg: mask & control 1328)



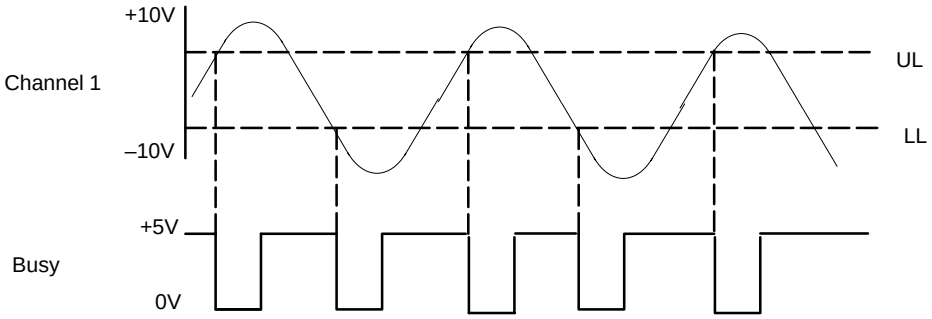
Code 04

(eg: mask & control 1428)



Code 05

(eg: mask & control 1528)



NB. Also set mask and control bit 7 to arm the module and commence triggering.