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DAC8415
16-CHANNEL 18-BIT DAC
INDUSTRY PACK

USERS MANUAL

PCB Issue 1.0
Firmware Version 8415V2201

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
21/10/10	1.0	Initial release.
09/02/12	1.1	Tidy up of manual.
08/01/15	2.0	Add ability to set offset on each channel
08/01/15	2.1	Change direction bit of Offset registers from bit 12 to bit 16.
28/11/17	2.2	Change from Hytec to Newwood Solutions for contact details
09/02/18	2.3	Change Firmware version and correct ID ROM content manual to show 8MHz only op and bit D12 is used for pos/neg control of DAC offset.

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CONTENTS

1. INTRODUCTION

The Hytec IP-DAC-8415 is a single-width Industry Pack that provides 16 channels of simultaneously updated digital to analogue conversion with the following characteristics:-

- 16 independently programmed channels
- 18 bits resolution – 18 bits monotonic.
- 16 or 18 bit operation selectable by hardware or software
- On board RAM Memory 1Meg x 16 bits (64K samples for 16bits) (32K samples for 18bits).
- ***+/-10V*** full scale output range *
- ***+/-5V*** full scale output range
- ***0 to 10V*** full scale output range
- ***0 to 5V*** full scale output range
- Ranges software selectable
- +/- 10mA current drive capability with continuous short-circuit protection
- Drives capacitive loads to 10000pF
- Straight binary or Two Complement input code
- Internal/External update clock rates
- Internal update clock rates programmable (50KHz,20KHz,10KHz,5KHz,2KHz,1KHz,500Hz,200Hz,100Hz,50Hz,20Hz,10Hz,5Hz,2Hz and 1Hz)
- Maximum 64KHz external clock rate
- Simultaneous up-date Power-on disable (outputs set to 0V on boot up)
- System to plant isolation to 100V when externally powered
- Board type, Board serial number, PCB issue and firmware version held on ROM.
- External Triggering
- Continuous function generation.
- Multi Trigger Mode.
- Repeat Multi Trigger Mode.
- Field upgradeable firmware (requires Xilinx/compatible device to program built in FPGA flash memory via the FPGA JTAG port).

* The units are factory set to have an output range of +/-10V on power up.

2. PRODUCT SPECIFICATIONS

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of channels:	16
DAC resolution:	18 bits
Data format ***+/-10V***:	18 bits straight binary Code format 20h = –10v, 20000h = 0V and 3FFE0h = +10V.
Data format ***+/-5V***:	18 bits straight binary Code format 40h = –5v, 20000h = 0V and 3FFC0h = +5V.
Data format ***0-10V***:	18 bits straight binary Code format 0000h = 0V and 3FFC0h = +10V.
Data format ***0-5V***:	18 bits straight binary Code format 0000h = 0V and 3FFC0h = +5V.
Output current:	+/-10mA @ FS
Capacitive load:	Stable up to 10000pF
Short circuit duration:	Continuous
OverV withstand:	No internal protection from external voltages provided
Update rate:	64KHz max
Power quiescent:	+5V @ 350mA typical +12V @ 150mA typical -12V @ 100mA typical
Isolation:	100V via opto-isolators (if externally powered by HYTEC 8912)
DAC device:	Texas Instruments DAC9881SB with serial interface
Integral non-linearity:	+/-1LSBs typ. +/-2LSBs max
Offset error:	+/- 32LSBs without calibration (+/-2LSBs after firmware calibration) at 25 deg C ambient. (Guaranteed for +/-10V range only).
Offset drift:	+/-0.8 ppm per deg C typical
Gain error:	+/- 32LSBs without calibration (+/-2LSBs after firmware calibration) at 25 deg C ambient. (Guaranteed for +/-10V range only).
Gain drift:	+/-10V range +/-2 ppm per deg C typical +/-5V range +/-4 ppm per deg C typical 0-10V range 2 ppm per deg C typical 0-5V range 0.8 ppm per deg C typical
Output slew rate:	1.6V/us typ.

3. Operating Modes

There are two operating modes:-

1. Registered – the DAC outputs are controlled by the contents of the DAC registers.
2. Memory – the DAC outputs are updated for the programmed number of samples at the programmed clock rate from the RAM memory.

All the outputs are updated serially but change together (there will be slight changes due to differences in the slew rate of the amplifiers (about +/-1uS) at the end of an internal update cycle.
The outputs may be updated at a rate of up to 64KHz. The two methods to update the 8415 DACs are detailed below.

3.1 USING REGISTER TO UPDATE DACs

For this mode set EX='0' and ARM='1' in the CSR.
In 18bit mode there are two registers per DAC channel giving a total of 32 registers. These can be loaded one at a time, the module can then be ARMed and the data from the registers will be serially loaded from one DAC to the next until all the data has been passed to the DACs. At this point the DAC outputs are automatically updated giving 16 simultaneous outputs. Then ARM bit is cleared.
In this mode the output sample clock is not used as the output is set when ARM is set.
All the outputs change together.

3.2 USING MEMORY TO UPDATE DACs

To select this mode set the following bits:-EX='1', ARM='1' in the CSR. Trigger using software trigger (ST) or external hardware trigger.
In this method the memory is first loaded with the required data and the number of memory locations used is entered in to the Number of Updates (NOC) register. The Control and Status Register (CSR) is then set to enable memory updates and ARM to unit with a software command. A trigger can then be issued either by a software command or by an external trigger to start down loading the data held in memory to the DACs via the registers as detail above. In this mode the registers are updated with new data from the memory at the update clock rate which is derived either internally or externally. The memory address is automatically incremented.

The unit can be programmed to generate an interrupt when memory is Half Full, Full or when the programmed number of outputs has occurred.
When the programmed number of output has occurred the unit will stop and ARM will be cleared.

In continuous mode, when the programmed number of output has occurred, the address counter will be zeroed and the output repeated until the ARM bit is cleared or the Cont bit in the CSR is cleared (no interrupt generated in continues mode). If the Cont bit is cleared, the unit will stop when the programmed number of output (NOC) has been reached.

The following should be loaded in to the NOC to output whole or half the memory in the following modes.

Memory Size (1MB in CSR)	Mode	NOC Values	
		Half memory	Full Memory
2Mb	18 Bit	0x4000	0x8000
2Mb	16 Bit	0x8000	0x0
1Mb	18 Bit	0x2000	0x4000
1Mb	16 Bit	0x4000	0x8000

When 1Mb is set the only change is when the Full and Half Full memory flags and interrupts occur as shown in the above table. The user must ensure that the correct NOC value is entered as the setting of the 1Mb in the CSR does not effect the NOC operation.

4. Memory Map

On board RAM Memory is 1M x 16 bits (64K samples per channel for 16bits) (32K for 18bits).
When used in the sixteen bit mode, there are two main buffer memories of 512k updates each (lower and upper buffers).
These are each divided into sixteen segments allocated to updates for DAC1 to DAC16.
When DAC16 has been updated from the top of the lower buffer, the Half memory Flag status is set and when it has been updated from the top of the upper memory buffer the Full Flag status is set.

Lower Conversion Memory	Upper Conversion Memory
DAC16 conversions	DAC16 conversions
DAC15 conversions	DAC15 conversions
DAC14 conversions	DAC14 conversions
DAC13 conversions	DAC13 conversions
DAC12 conversions	DAC12 conversions
DAC11 conversions	DAC11 conversions
DAC10 conversions	DAC10 conversions
DAC9 conversions	DAC9 conversions
DAC8 conversions	DAC8 conversions
DAC7 conversions	DAC7 conversions
DAC6 conversions	DAC6 conversions
DAC5 conversions	DAC5 conversions
DAC4 conversions	DAC4 conversions
DAC3 conversions	DAC3 conversions
DAC2 conversions	DAC2 conversions
DAC1 conversion 16k (bits16 - 17) DAC1 conversion 16k (bits 0 -15) DAC1 conversion 16k-1 (bits16 - 17) DAC1 conversion 16k-1 (bits 0 -15) DAC1 conversion 2 (bits16 - 17) DAC1 conversion 2 (bits 0 -15) DAC1 conversion 1 (bits16 - 17) DAC1 conversion 1 (bits 0 -15)	DAC1 conversion 32k (bits16 - 17) DAC1 conversion 32k (bits 0 -15) DAC1 conversion 32k-1 (bits16 - 17) DAC1 conversion 32k-1 (bits 0 -15) DAC1 conversion 16k+2 (bits16 - 17) DAC1 conversion 16k+2 (bits 0 -15) DAC1 conversion 16k+1 (bits16 - 17) DAC1 conversion 16k+1 (bits 0 -15)

18 Bit Mode

Lower Conversion Memory	Upper Conversion Memory
DAC16 conversions	DAC16 conversions
DAC15 conversions	DAC15 conversions
DAC14 conversions	DAC14 conversions
DAC13 conversions	DAC13 conversions
DAC12 conversions	DAC12 conversions
DAC11 conversions	DAC11 conversions
DAC10 conversions	DAC10 conversions
DAC9 conversions	DAC9 conversions
DAC8 conversions	DAC8 conversions
DAC7 conversions	DAC7 conversions
DAC6 conversions	DAC6 conversions
DAC5 conversions	DAC5 conversions
DAC4 conversions	DAC4 conversions
DAC3 conversions	DAC3 conversions
DAC2 conversions	DAC2 conversions
DAC1 conversion 32k DAC1 conversion 32k-1 DAC1 conversion 2 DAC1 conversion 1	DAC1 conversion 64k DAC1 conversion 64k-1 DAC1 conversion 32k+2 DAC1 conversion 32k+1

16 Bit Mode

5. Application Registers

There are a number of application and control registers as shown in the following table:

Application Register Table

Byte Addressing		**Word Addressing**		**16 Bit Application Registers**
Hex	***Dec***	***Hex***	***Dec***	
0	0	0	0	CSR
2	2	1	1	Conversion pointer
4	4	2	2	Number of Conversions
6	6	3	3	Sample Rate
8	8	4	4	Interrupt Vector
A	10	5	5	Extend Control & Status Register
C	12	6	6	Digital Potentiometer Data Register This allows the user to write to Digital Pot
E	14	7	7	Not used
10 - 4E	16 - 78	8-27	8-39	DAC Data register Channel 1
50 – 6E	80 - 110	28 - 37	40 - 55	**16 X DAC Offset registers Channels 1 to 16**
70	112	38	56	Not used
72	114	39	57	Not used
74	116	3A	58	Not used
76	118	3B	59	Not used
78	120	3C	60	Digital Potentiometer Calibration Register +/-10V (Read Only)
7A	122	3D	61	Digital Potentiometer Calibration Register +/-5V (Read Only)
7C	124	3E	62	Digital Potentiometer Calibration Register 0V – 10V (Read Only)
7E	126	3F	63	Digital Potentiometer Calibration Register 0V - 5V (Read Only)

5.1 Control & Status Register (CSR)

Read/Write Address: Byte 0hex (Word 0hex)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ARM	EX	ST	XC	ET	EE	FE	HE	BS	SSU	1MB	MH	CONT	CC	F	HF

ARM Writing a '1' to ARM bit causes the values loaded in to the DAC registers or the memory to be loaded in to the DACs.
When all the DACs have been updated from the registers (the EX bit set to '0') the ARM bit is cleared.
If the DACs are being updated from the memory (the EX bit set to '1') the ARM bit is not cleared.
In this mode if a number of triggers occur which cause the end of the memory to be reached, a subsequent trigger will cause the memory pointer to wrap around to the start of memory.

EX Enable trigger and memory update.
EX=0 The outputs will be loaded from the DAC registers.
EX=1 Allows external trigger or software trigger to initiate programmed updates from memory. In this mode the *Number Of Updates Register (NOC)* needs to be set between 0 to 64K updates.

ST Software trigger. Triggers the programmed number of updates from the memory as set by the Number of Updates register.

XC Enable the external clock. 0 = internal clock used for the sample rate. 1 = external clock used for the sample rate.

ET When set to '1' enables Inhibiting via the Lemo of the 8002 via the IP Strobe line. The Inhibit signal when set stops updating the DAC from memory.

EE Enables interrupt at end of programmed number of DAC updates from memory.

FE Enables interrupt when the upper conversion memory has been filled. (Memory Full).

HE Enables interrupt when the lower conversion memory has been filled. (Memory Half Full).

BS Busy status: Flag showing unit is busy shifting data to DAC's or in process of changing range.

SSU Writing a '1' will set all DAC outputs to zero (this bit is auto cleared on completion)

1MB Enable 1Mb memory (32K values/channel) when logic 1 and 2Mb (64K values/channel) when logic 0.

MH Set to '1' when the memory is inhibited from the IP Strobe line and ET is set.

CONT Sets continuous function generation

CC Conversions complete. Status bit set when the number of programmed updates has been completed. Generates IRQ0* if set and EE is set to a logic 1.

F Full status. Set when DAC16 has been updated from the top of memory. Generates IRQ0* if set and FE is set to a logic 1.

HF Half full status. Set when DAC16 has been updated from the top of the lower memory buffer. Generates IRQ0* if set and HE is set to a logic 1.

5.2 Memory Pointer

Read/write Address: Byte 2hex (Word 1hex)
The Memory pointer is the number of updates held in the memory.
The current conversion address is given by the Memory pointer address offset by the DAC number and the Full status.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

5.3 Number of updates (NOC)

Read/write Address: Byte 4hex (Word 2hex)
The number of updates register allows the number of updates per trigger to be programmed. If the memory buffer size is exceeded the update values will wrap around from the upper memory to the base of the lower memory.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

If the CONT bit ='1' set in CSR then the set number of outputs is output continuously.
If CONT not set then set nos bit output then the TRIGEN is cleared. CC in the CSR needs to be cleared before a further trigger is seen.

The following should be loaded in to the NOC to output whole or half the memory in the following modes.

Mode	NOC Values	
	Half Full	Full
18 Bit 2Mb	0x4000	0x8000
16 Bit 2Mb	0x8000	0x0
18 Bit 1Mb	0x2000	0x4000
16 Bit 1Mb	0x4000	0x8000

When 1Mb is set it only changes when the Full and Half Full flags and interrupts occur as shown in the above table. The user must ensure that the correct NOC value is entered as the setting of the 1Mb in the CSR does not effect the NOC operation.

5.4 Clock Rate

Read/write Address: Byte 6hex (Word 3hex)
The clock rate register is a four bit register (D00 to D03) which enables codes 0 – 13 to enable frequencies of 1 Hz to 50kHz in multiples of 1, 2, 5 or 10. (E.g. 0=1Hz, 1=2Hz, 2=5Hz, 3=10Hz and so on to 0xD=20KHz , 0xE=50KHz). Each clock pulse will initiate all 16 DAC updates from memory.

Clock rate Reg (D3 to D0)	Frequency Hz	Clock rate Reg (D3 to D0)	Frequency Hz
0000	1	1000	500
0001	2	1001	1MHz
0010	5	1010	2MHz
0011	10	1011	5MHz
0100	20	1100	10MHz
0101	50	1101	20MHz
0110	100	1110	50MHz
0111	200	1111	-

5.5 Interrupt Vector

Read/write Address: Byte 8hex (Word 4hex)
The vector register is a 16 bit register which stores the interrupt vector value.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

5.6 Extended Control & Status Register (CSR Ext)

Read/write Address: Byte Ahex (Word 5hex)
This gives added functionality over the 8402

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
EN16	CAL				E	EFW	IFW			RP	MT		BTC	R1	R0

R This sets range from "00"=+/-10V, "01"+/-5V, "10"=0-10V & "11"=0-5V.

BTC '0'= DAC input data straight binary '1'= DAC input data twos complement.

MT Multi trigger mode.

RP Cycle memory in Multi trigger mode

IFW **Do not set this bit as setup and calibration data maybe lost.** This bit enables the FPGA flash write from buffer command

EFW **Do not set this bit as setup and calibration data maybe lost.** This bit enables the External flash write by writing to IP mem i.e. switches off RAM

E **Do not set this bit as setup and calibration data maybe lost.** This bit enables the External flash chip or sector erase when do a IP write to mem. If IP data is 0x10 then chip erase (64s time taken) if IP data is 0x30 then sector erase where the sector address is given in the IP memory address lines. If chip erase then IP mem address = 0x555 and data 0x10.

CAL If set to '1' unit does not use on board flash calibration ***for register updates only.*** If EX=1 then this has no effect. Used for production test.

EN16 If set to '1' makes the unit same as the Hytec 8402 16 bit DAC. This bit can also be set by jumper J3 on PCB.

5.7 Digital Potentiometer Data Register

Read/write Address: Byte Chex (Word 6hex)

This is used for calibration only during production test on the units.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
EN	PD	CWR	X	X	X	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

The '**EN**' (bit 15) when set as a '1' will cause the current value of the register to be down loaded to the 10bit digital pot. On completion of the write the EN bit is cleared. The rest of the contents of the register remain unaltered.

PD bit when set to '1' loads the digital pot range data held in FPGA flash to registers in the FPGA. This is for production use only.

CWR bit copies wiper register in in digital pot to the non-volatile register in digital pot. This is for production use only.

The user can use this register to tweak the gain error of the unit if required. This maybe be used to compensate for ambient temperature.

5.8 DAC Registers

Read/write Address: Byte 10hex – 4Ehex (Word 8hex – 27hex)
The 16 DACs are updated from these registers when ARM is set EX bit is zero. On completion the ARM bit is cleared.
Straight binary data format or Twos Complement Code set by BTC bit of CSR Ext register.

16 bit code (as Hytec 8402) this uses address **10hex to 2Ehex (Word 8hex – 17hex) for channels 1 to 16.**

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C17	C16	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2

18 bit code this uses address **10hex to 4Ehex (Word 8hex – 27hex)**
i.e. channel 1 address of low word is 10hex (Word 8hex)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

i.e. channel 1 address of high word is 12hex (Word 9hex)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	C17	C16

5.9 DAC Offset Registers

Read Address: Byte 50hex – 6Ehex (Word 28hex – 37hex).

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	X	X	D	O11	O10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0

The 16 DACs can have there offset adjusted using these registers. If an overflow occurs the max\min output of the DAC will be set to max = 0x3FFFF and min = 0x00000.

O0-O11 This sets the offset value

D This is the sign bit 0 = Positive 1 = Negative.

5.10 Digital Potentiometer Calibration Registers

Read Address: Byte 60hex – 66hex (Word 30hex – 33hex)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	X	X	X	X	X	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

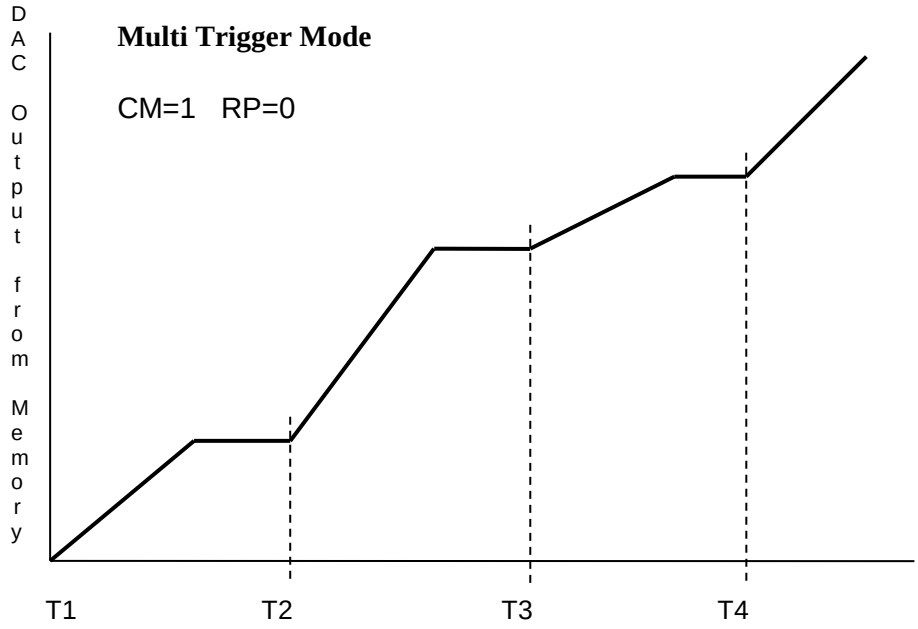
These four registers hold the digital pot calibration factor for each of the DACs voltage ranges. The values are loaded at power up from the FPGA flash or when 'PD' (bit 14) of the digital pot register is set to '1' this is cleared at the finish.
When the range is changed the data held in the associated register is loaded to the digital potentiometer.
The calibration values held in the FPGA flash are programmed in during production test.
The digital pot can still be changed using the Digital Potentiometer Register above but the digital pot will reload its self from the calibration registers on power up and on a range change.

6. MULTI TRIGGER AND REPEAT MULTI TRIGGER MODE

Multi trigger mode is set by bit 4 (MT) in the Ext CSR. This allows the user to repeatedly trigger the unit. The number of updates is set by the NOC register. When the unit is triggered and the required number of updates output the CC flag in the CSR is set and the unit stopped.

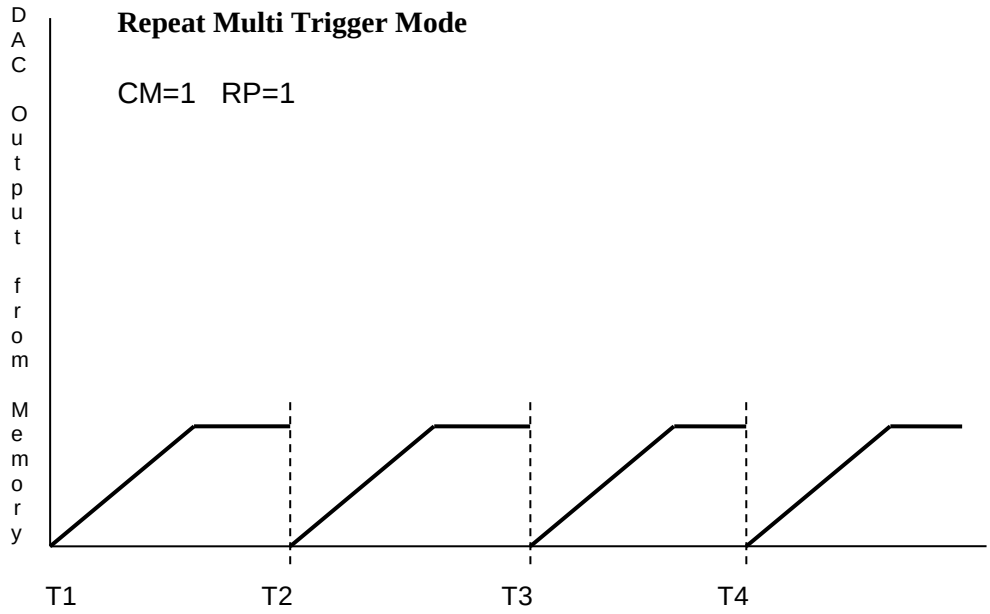
6.1 Multi Trigger Mode

In this mode the memory address pointer is **not** cleared. On the subsequent triggers the CC flag is cleared then at the end of the number of update is reset. If the half full or full points of the memory are reached then the half Full and Full Flags will be set. If memory reaches full it will wrap a round and repeat either with the next trigger or if number of updates take it over the memory full then it will wrap. Also the memory Half Full and Full flags will **NOT** be cleared once set.



6.2 Repeat Multi Trigger Mode

Repeat multi trigger mode is set by bit 5 (RP) in Ext CSR. In repeat multi trigger mode the address pointer is cleared on each trigger.



7. ID PROM

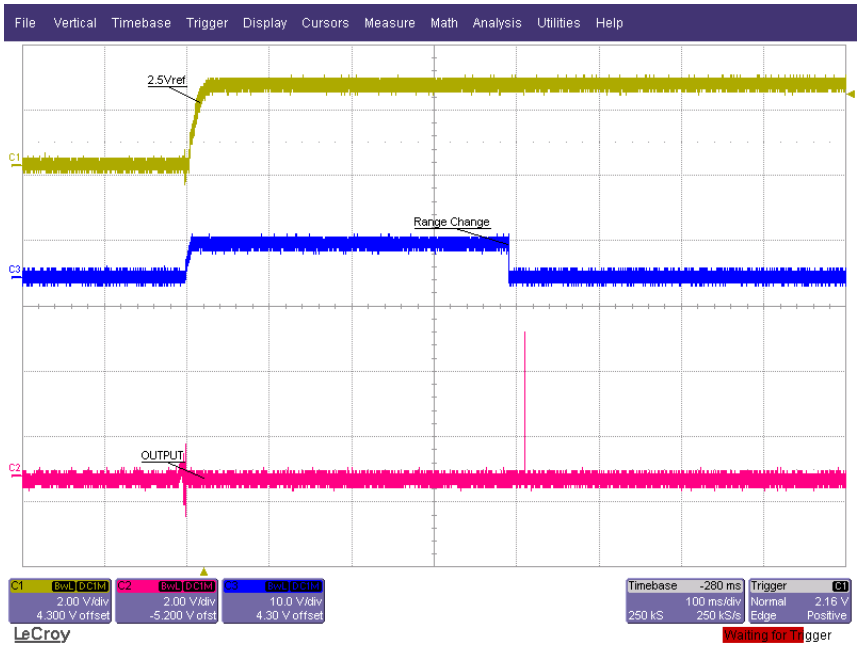
The ID data is stored in Flash memory. The word addresses are as below:-

Base+80	ASCII 'VI'	5649h	
Base+82	ASCII 'TA'	5441h	
Base+84	ASCII '4 '	3420h	
Base+86	Murf ID high byte	0080h	
Base+88	Murf ID low word	0300h	
Base+8A	Model number	8415h	
Base+8C	Revision	2201h	This shows PCB Iss 2 and FPGA firmware at Ver 201
Base+8E	Reserved	0000h	
Base+90	Driver ID	0000h	
Base+92	Driver ID	0000h	
Base+94	Flags	0002h	This shows 8MHz IP operation.
Base+96	No of bytes used	001Ah	
Base+98	Cal Type	0000h	0 = No Calibration factors.
Base+9A	Serial Number	xxxxdec	
Base+9C	Not used	0000h	
Base+9E	Not used	0000h	

8. POWER UP AND POWER DOWN AND RESET OF 8415 DAC

8.1 Power Up

During power up the 8415 outputs should remain approx zero volts with transients as shown below



8.2 Power Down

At power down the 8415 outputs are not guaranteed to remain steady.

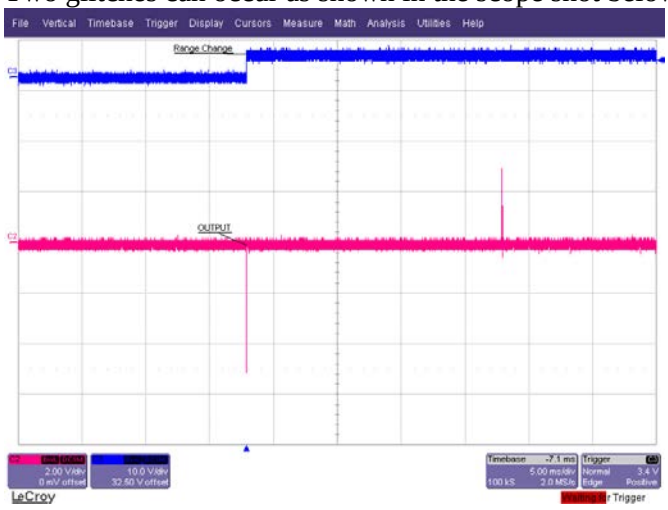
8.3 IP Reset

An IP reset will set the DAC output voltage to zero and set the range to +/-10V.
Reset clears the following registers:-
CSR.
NOC.
All DAC registers are zeroed.

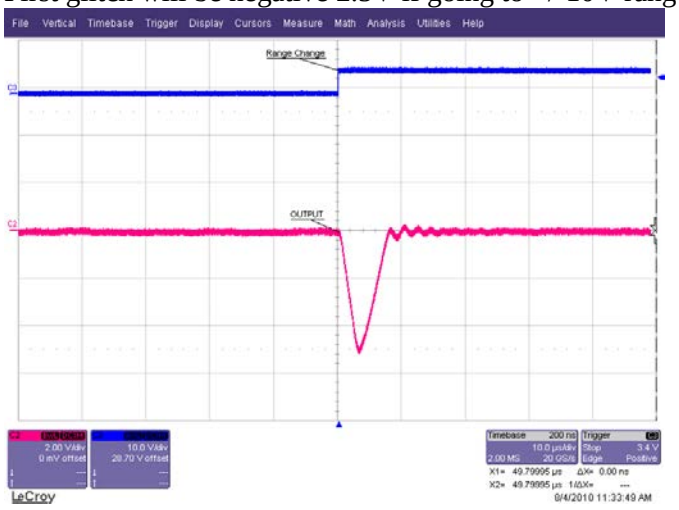
9. CHANGING RANGE OF 8415 DAC

The DAC 8415 powers on in the +/-10V range. When the range is change by writing to bits 0 and 1 of the ExtCSR the DAC will be offline for approx 20mS. During this time the DAC output will be zeroed and the new reference and offset voltages applied. During this process the output may glitch as shown in the following scope shots.

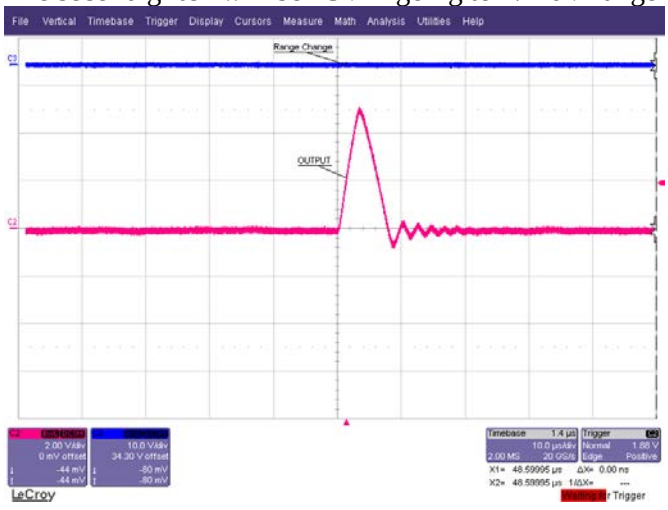
Two glitches can occur as shown in the scope shot below.



First glitch will be negative 2.5V if going to +/-10V range or negative 5V if going to +/-5V.



The second glitch will be +5V if going to +/-10V range or +2.5V if going from to +/-5V



When going from +/-5V to 0-10V then only first glitch to 2.5V.
When going from 0-10V to +/-5V only second glitch at 2.5V.

When going from +/-10V to 0-5V then only first glitch to 5V.
When going from 0-5V to +/-10V only second glitch at 5V.

When going from +/-10V to 0-10V then only first glitch to 5V.
When going from 0-10V to +/-10V only first glitch at 5V.

When going from +/-5V to 0-5V then only first glitch to 2.5V.
When going from 0-5V to +/-5V only first glitch at 2.5V.

When going between 0-5V and 0-10V no glitches occur

10.RANGE RESOLUTION AND INSTALLATION CONSIDERATIONS

The following table shows the resolution per range:

Range	Resolution
+/-10V	76.312576uV
+/-5V	38.165608uV
+10V	38.156288uV
+5V	19.078144uV

Due to the high resolution and linearity of the DAC, system design problems such as grounding and contact resistance become very important. For this 18bit converter with a 20V full-scale range , 1LSB is 76.312576uV. With a load current of 5mA, series wiring and connector resistance of only 60mohms will cause an output error of 2LSBs.
To put this in contexts the resistance of #23 wire is about 0.067ohms/meter. Neglecting contact resistance, less than 1 meter of wire will produce an error greater than 2LSBs in the analogue output voltage.

11.EPICS and ASYN Software Driver Plus Linux/Windows API

EPICS and ASYN software drivers are in avalable for the DAC8415 16 channel DAC Industry Pack.
For downloads go to: http://www.newwoodsolutions.co.uk

A Linux/Windowa API is available, consult Newwood Solutions Ltd for details.

12.SELECTION OF THE +/-12 VOLT POWER SUPPLY

The DAC 8415 +/-12 volt power supply can be derived either internally from the carrier card or from an external source via a transition card. The source is selected using jumpers J1, J2 and the GND AGND link LNK1 where:

J1 External +12V connect 1 & 2, Internal +12V connect 2 & 3
J2 External -12V connect 1 & 2, Internal -12V connect 2 & 3

LNK1 (GND AGND)
IN for internal +/-12V
OUT for external +/-12V (supplied from transition card DC DC converter).

APPENDIX A

PCB JUMPERS

Issue 1 PCB
J1 External +12V connect 1 & 2, Internal +12V connect 2 & 3
J2 External -12V connect 1 & 2, Internal -12V connect 2 & 3
J3 Sets 16bit mode when IN This overrides the EN16 bit in the CSR Ext(Factory set OUT)
J4 Not used. Jumper for J3 located here for shipment.

LNK1 Factory set IN links VME GND and AGND

APPENDIX B

I/O Connector – PL2 (50 way) on 8415 DAC PCB

Pin	Signal	Pin	Signal
1	Output 1	26	AGND
2	AGND	27	Output14
3	Output 2	28	AGND
4	AGND	29	Output15
5	Output 3	30	AGND
6	AGND	31	Output16
7	Output 4	32	AGND
8	AGND	33	N.C.
9	Output 5	34	N.C.
10	AGND	35	XTrigger
11	Output 6	36	/XTrigger
12	AGND	37	N.C.
13	Output 7	38	N.C.
14	AGND	39	XClk
15	Output 8	40	/XClk
16	AGND	41	+12VX
17	Output9	42	AGND
18	AGND	43	+12VX
19	Output10	44	AGND
20	AGND	45	-12VX
21	Output11	46	AGND
22	AGND	47	-12VX
23	Output12	48	AGND
24	AGND	49	N.C.
25	Output13	50	AGND

APPENDIX C

HYTEC TRANSITION CARD 8202 CONNECTIONS

I/O Connector – 50 way on transition panel

Pin	Signal	Pin	Signal
1	AGND	26	Output1
2	AGND	27	Output 2
3	AGND	28	Output 3
4	AGND	29	Output 4
5	AGND	30	Output 5
6	AGND	31	Output 6
7	AGND	32	Output 7
8	AGND	33	Output 8
9	AGND	34	Output 9
10	AGND	35	Output 10
11	AGND	36	Output 11
12	AGND	37	Output 12
13	AGND	38	Output 13
14	AGND	39	Output 14
15	AGND	40	Output 15
16	AGND	41	Output 16
17		42	
18	XTRIG N	43	XTRIG P
19		44	
20	XCLK N	45	XCLK P
21		46	
22		47	
23		48	
24	AGND	49	AGND
25	AGND	50	AGND

APPENDIX D

VME64X PIN ASSIGNMENT ON HYTEC 8002/4 IP CARRIER BOARD FOR DAC8415

ROW A	SIG	ROW B	SIG	ROW C	SIG	ROW D	SIG	ROW E	SIG	ROW F	SIG
P0.A01	D Chan 1+	P0.B01	D Chan 1-	P0.C01	D Chan 2+	P0.DO1	D Chan 2 -	P0.E01	D Chan 3+	P0.F01	GND
P0.A02	D Chan 3 -	P0.B02	D Chan 4+	P0.C02	D Chan 4 -	P0.D02	D Chan 5+	P0.E02	D Chan 5 -	P0.F02	GND
P0.A03	D Chan 6+	P0.B03	D Chan 6 -	P0.C03	D Chan 7+	P0.D03	D Chan 7 -	P0.E03	D Chan 8+	P0.F03	GND
P0.A04	D Chan 8 -	P0.B04	D Chan 9+	P0.C04	D Chan 9 -	P0.D04	D Chan 10 +	P0.E04	D Chan 10 -	P0.F04	GND
P0.A05	D Chan 11+	P0.B05	D Chan 11 -	P0.C05	D Chan 12 +	P0.D05	D Chan 12 -	P0.E05	D Chan 13 +	P0.F05	GND
P0.A06	D Chan 13 -	P0.B06	D Chan 14 +	P0.C06	D Chan 14 -	P0.D06	D Chan 15 +	P0.E06	D Chan 15 -	P0.F06	GND
P0.A07	D Chan 16+	P0.B07	D Chan 16 -	P0.C07	N/C	P0.D07	N/C	P0.E07	D XTrigger	P0.F07	GND
P0.A08	D/XTrigger	P0.B08	N/C	P0.C08	N/C	P0.D08	D XCLK	P0.E08	D /XCLK	P0.F08	GND
P0.A09	D +12V	P0.B09	D AGND	P0.C09	D +12V	P0.D09	D AGND	P0.E09	D -12V	P0.F09	GND
P0.A10	D AGND	P0.B10	D -12V	P0.C10	D AGND	P0.D10	N/C	P0.E10	D AGND	P0.F10	GND
P0.A11	C Chan 1+	P0 B11	C Chan 1 -	P0.C11	C Chan 2+	P0.D11	C Chan 2 -	P0 E11	C Chan 3+	P0.F11	GND
P0.A12	C Chan 3 -	P0.B12	C Chan 4+	P0.C12	C Chan 4 -	P0.D12	C Chan 5+	P0.E12	C Chan 5 -	P0.F12	GND
P0.A13	C Chan 6+	P0.B13	C Chan 6-	P0.C13	C Chan 7+	P0.D13	C Chan 7 -	P0.E13	C Chan 8+	P0.F13	GND
P0.A14	C Chan 8-	P0.B14	C Chan 9+	P0.C14	C Chan 9-	P0.D14	C Chan 10+	P0.E14	C Chan 11+	P0.F14	GND
P0.A15	C Chan 11+	P0.B15	C Chan 11-	P0.C15	C Chan 12+	P0.D15	C Chan 12-	P0.E15	C Chan 13+	P0.F15	GND
P0.A16	C Chan 13-	P0.B16	C Chan 14+	P0.C16	C Chan 14-	P0.D16	C Chan 15+	P0.E16	C Chan 15-	P0.F16	GND
P0.A17	C Chan 16+	P0.B17	C Chan 16-	P0.C17	N/C	P0.D17	N/C	P0.E17	C XTrigger	P0.F17	GND
P0.A18	C/XTrigger	P0.B18	N/C	P0.C18	N/C	P0.D18	C XCLK	P0.E18	C /XCLK	P0.F18	GND
P0.A19	C +12V	P0.B19	C AGND	P0.C19	C +12V	P0.D19	C AGND	P0.E19	C -12V	P0.F19	GND

P0 pin assignment

P1 ROW A	SIGNAL	P1 ROW B	SIGNAL	P1 ROW C	SIGNAL	P1 ROW D	SIGNAL	P1 ROW Z	SIGNAL
P1.A01	D00	P1.B01	N/C	P1.C01	D08	P1.D01	N/C	P1.Z01	N/C
P1.A02	D01	P1.B02	N/C	P1.C02	D09	P1.D02	N/C	P1.Z02	GND
P1.A03	D02	P1.B03	N/C	P1.C03	D10	P1.D03	N/C	P1.Z03	N/C
P1.A04	D03	P1.B04	BG0IN*	P1.C04	D11	P1.D04	N/C	P1.Z04	GND
P1.A05	D04	P1.B05	BG0OUT*	P1.C05	D12	P1.D05	N/C	P1.Z05	N/C
P1.A06	D05	P1.B06	BG1IN*	P1.C06	D13	P1.D06	N/C	P1.Z06	GND
P1.A07	D06	P1.B07	BG1OUT*	P1.C07	D14	P1.D07	N/C	P1.Z07	N/C
P1.A08	D07	P1.B08	BG2IN*	P1.C08	D15	P1.D08	N/C	P1.Z08	GND
P1.A09	GND	P1.B09	BG2OUT*	P1.C09	GND	P1.D09	N/C	P1.Z09	N/C
P1.A10	N/C	P1.B10	BG3IN*	P1.C10	N/C	P1.D10	N/C	P1.Z10	GND
P1.A11	GND	P1.B11	BG3OUT*	P1.C11	BERR*	P1.D11	N/C	P1.Z11	N/C
P1.A12	DS1*	P1.B12	N/C	P1.C12	RESET	P1.D12	+3.3V	P1.Z12	GND
P1.A13	DS0*	P1.B13	N/C	P1.C13	LWORD*	P1.D13	N/C	P1.Z13	N/C
P1.A14	WRITE	P1.B14	N/C	P1.C14	AM5	P1.D14	+3.3V	P1.Z14	GND
P1.A15	GND	P1.B15	N/C	P1.C15	A23	P1.D15	N/C	P1.Z15	N/C
P1.A16	DTACK*	P1.B16	AM0	P1.C16	A22	P1.D16	+3.3V	P1.Z16	GND
P1.A17	GND	P1.B17	AM1	P1.C17	A21	P1.D17	N/C	P1.Z17	N/C
P1.A18	AS	P1.B18	AM2	P1.C18	A20	P1.D18	+3.3V	P1.Z18	GND
P1.A19	GND	P1.B19	AM3	P1.C19	A19	P1.D19	N/C	P1.Z19	N/C
P1.A20	IACK	P1.B20	GND	P1.C20	A18	P1.D20	+3.3V	P1.Z20	GND
P1.A21	IACKIN*	P1.B21	N/C	P1.C21	A17	P1.D21	N/C	P1.Z21	N/C
P1.A22	IACKOUT	P1.B22	N/C	P1.C22	A16	P1.D22	+3.3V	P1.Z22	GND
P1.A23	AM4	P1.B23	GND	P1.C23	A15	P1.D23	N/C	P1.Z23	N/C
P1.A24	A07	P1.B24	IRQ7*	P1.C24	A14	P1.D24	+3.3V	P1.Z24	GND
P1.A25	A06	P1.B25	IRQ6*	P1.C25	A13	P1.D25	N/C	P1.Z25	N/C
P1.A26	A05	P1.B26	IRQ5*	P1.C26	A12	P1.D26	+3.3V	P1.Z26	GND
P1.A27	A04	P1.B27	IRQ4*	P1.C27	A11	P1.D27	N/C	P1.Z27	N/C
P1.A28	A03	P1.B28	IRQ3*	P1.C28	A10	P1.D28	+3.3V	P1.Z28	GND
P1.A29	A02	P1.B29	IRQ2*	P1.C29	A09	P1.D29	N/C	P1.Z29	N/C
P1.A30	A0l	P1.B30	IRQ1*	P1.C30	A08	P1.D30	+3.3V	P1.Z30	GND
P1.A31	-12V	P1.B31	N/C	P1.C31	+12V	P1.D31	N/C	P1.Z31	N/C
P1.A32	+5V	P1.B32	+5V	P1.C32	+5V	P1.D32	+5V	P1.Z32	GND

P1 Pin Assignment

ROWA	SIG	ROWB	SIG	ROWC	SIG	ROWD	SIG	ROWZ	SIG
P2.A01	B +12V	P2.B01	+5V	P2.C01	B AGND	P2.D01	C -12V	P2.Z01	C AGND
P2.A02	B +12V	P2.B02	GND	P2.C02	B AGND	P2.D02	C AGND	P2.Z02	GND
P2.A03	B -12V	P2.B03	N/C	P2.C03	B AGND	P2.D03	C AGND	P2.Z03	N/C
P2.A04	B -12V	P2.B04	A24	P2.C04	B AGND	P2.D04	B Chan 1 +	P2.Z04	GND
P2.A05	N/C	P2.B05	A25	P2.C05	B AGND	P2.D05	B Chan 2 +	P2.Z05	B Chan 1 -
P2.A06	A Chan 1 +	P2.B06	A26	P2.C06	A Chan 1 -	P2.D06	B Chan 2 -	P2.Z06	GND
P2.A07	A Chan 2 +	P2.B07	A27	P2.C07	A Chan 2 -	P2.D07	B Chan 3 -	P2.Z07	B Chan 3 +
P2.A08	A Chan 3 +	P2.B08	A28	P2.C08	A Chan 3 -	P2.D08	B Chan 4 +	P2.Z08	GND
P2.A09	A Chan 4 +	P2.B09	A29	P2.C09	A Chan 4 -	P2.D09	B Chan 5 +	P2.Z09	B Chan 4 -
P2.A10	A Chan 5 +	P2.B10	A30	P2.C10	A Chan 5 -	P2.D10	B Chan 5 -	P2.Z10	GND
P2.A11	A Chan 6 +	P2.B11	A31	P2.C11	A Chan 6 -	P2.D11	B Chan 6 -	P2.Z11	B Chan 6 +
P2.A12	A Chan 7 +	P2.B12	GND	P2.C12	A Chan 7 -	P2.D12	B Chan 7 +	P2.Z12	GND
P2.A13	A Chan 8 +	P2.B13	+5V	P2.C13	A Chan 8 -	P2.D13	B Chan 8 +	P2.Z13	B Chan 7 -
P2.A14	A Chan 9 +	P2.B14	N/C	P2.C14	A Chan 9 -	P2.D14	B Chan 8 -	P2.Z14	GND
P2.A15	A Chan 10 +	P2.B15	N/C	P2.C15	A Chan 10 -	P2.D15	B Chan 9 -	P2.Z15	B Chan 9 +
P2.A16	A Chan 11 +	P2.B16	N/C	P2.C16	A Chan 11 -	P2.D16	B Chan 10 +	P2.Z16	GND
P2.A17	A Chan 12 +	P2.B17	N/C	P2.C17	A Chan 12 -	P2.D17	B Chan 11 +	P2.Z17	B Chan 10 -
P2.A18	A Chan 13 +	P2.B18	N/C	P2.C18	A Chan 13 -	P2.D18	B Chan 11 -	P2.Z18	GND
P2.A19	A Chan 14 +	P2.B19	N/C	P2.C19	A Chan 14 -	P2.D19	B Chan 12 -	P2.Z19	B Chan 12+
P2.A20	A Chan 15 +	P2.B20	N/C	P2.C20	A Chan 15 -	P2.D20	B Chan 13 +	P2.Z20	GND
P2.A21	A Chan 16 +	P2.B21	N/C	P2.C21	A Chan 16 -	P2.D21	B Chan 14 +	P2.Z21	B Chan 13 -
P2.A22	N/C	P2.B22	GND	P2.C22	N/C	P2.D22	B Chan 14 -	P2.Z22	GND
P2.A23	A X Trigger	P2.B23	N/C	P2.C23	A /XTrigger	P2.D23	B Chan 15 -	P2.Z23	B Chan 15+
P2.A24	N/C	P2.B24	N/C	P2.C24	N/C	P2.D24	B Chan 16 +	P2.Z24	GND
P2.A25	A XCLK	P2.B25	N/C	P2.C25	A /XCLK	P2.D25	N/C	P2.Z25	B Chan 16 -
P2.A26	A +12V	P2.B26	N/C	P2.C26	A AGND	P2.D26	N/C	P2.Z26	GND
P2.A27	A +12V	P2.B27	N/C	P2.C27	A AGND	P2.D27	B /XTrigger	P2.Z27	B X Trigger
P2.A28	A -12V	P2.B28	N/C	P2.C28	A AGND	P2.D28	N/C	P2.Z28	GND
P2.A29	A -12V	P2.B29	N/C	P2.C29	A AGND	P2.D29	B XCLK	P2.Z29	N/C
P2.A30	N/C	P2.B30	N/C	P2.C30	A AGND	P2.D30	B /XCLK	P2.Z30	GND
P2.A31	Out+3.3V	P2.B31	GND	P2.C31	Out+3.3V	P2.D31	GND	P2.Z31	Out +3.3V
P2.A32	Out +5V	P2.B32	+5V	P2.C32	Out +5V	P2.D32	PC +5V	P2.Z32	GND

P2 pin assignment

	Denotes pins with thickened tracks which can be used for power inputs