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MCS8522
MULTI-CHANNEL SCALER INDUSTRY PACK

USERS MANUAL

PCB Issue 1.0
Firmware Versions:
Histogram Mode LVDS\TTL V103
Histogram Mode LVDS\TTL V104
Histogram Mode LVDS\TTL V105
Preset Scaler Mode LVDS\TTL V103

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
30/05/12	1.0	Initial release.
25/07/12	1.1	FF flag put in CSR. Unit does not start when nos cycles/triggers is set to zero. Unit does not start in Hist mode when Nos Gates per cycle is set to zero. Enter value required as opposed to not one less. Mem address reg in straight scaler mode shows next memory location to be written to.
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18/12/14	3.0	In Histogram Mode add External Enable function and amend TTL logic level register to include External Enable bit level.
28/11/17	3.1	Change from Hytec to Newwood Solutions for contact details
05/01/21	3.2	Some references to Hytec changed to Newwood Solutions in text

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1. INTRODUCTION

The Newwood Solutions IP-MSC-8522 is a single-width Industry Pack that provides 16 scalers channels with the following characteristics:-

- 16 independent counting channels.
- 32-bit counter depth.
- Shadow register to allow on-the-fly reading of scalers.
- Full 32 bits binary count capacity and 64 bit histogram capability.
- 2Mbytes SRAM.
- Gate/Bin advance by internal timer or programmable number of external pulses.
- 200MHz Count rates (LVDS, LVPECL and NIM), 100MHz for TTL.
- TTL, LVDS and LVPECL inputs (Input type must be specified when ordered).
- Input type can be reconfigured in the field via the JTAG port if requirements change.
- NIM input via dedicated terminal block.
- Each scaler has a 16 bit input coincidence pattern register.
- Interrupt on completion of programmed number of cycles/triggers/counts.
- External hardware trigger (software enable) or software trigger.
- Trigger output to allow Trigger In / Out daisy-chain connection for synchronisation.
- Software and external hardware reset of scalers and memory.
- Scaler external inputs via transition board.
- Trigger ignored if cycle has not completed.
- Channel masking.
- Counter Overflow register.
- Number of Cycle/Triggers Received register.
- The ability to read the module identity, manufacturer, model, revisions, input type and serial number from an onboard ID ROM.
- In the field firmware upgrade capability.

2. Modes of Operation

2.1 Histogramming Mode

In this mode a histogram is formed for each channel. This is achieved by acquiring and logging the data for each channel over a number of programmable time intervals (gates/bins) for a programmable number of cycles.

- Gate/Bin advance by internal timer or programmable number external pulses (1 to 65525).
- Internal Gate intervals may be programmed from 100usec to 65secs
- Output pulse on each Gate/Bin advance.
- Programmable memory depth (number of time intervals or Gate/Bins) per triggered cycle of gate intervals up to 16k per channel of 64bit data.
- 64 bit totalisers records each channels total counts for each Gate/Bin.
- 64 bit totalisers records each channels total count for all Gates/Bins in each cycle.
- Dwell time approx 10us.
- Coincidence mode allows counting for coincidence on multiple inputs.

2.2 Straight Scaler Mode

Straight scaler mode allows fixed or variable length counting time intervals. The interval length can be defined by an internal timer or by an external signal which can also be prescaled.
In this mode a time period or gate interval is set and when the unit is trigged the sixteen 32 bit counters will be enabled.
The gate interval can also be controlled externally by setting the EBA bit in the CSR. Here the timing pulses are user defined and received via the trigger input.
When the gate interval is finished the counter values are loaded in memory. The number of logged values is set in the Nos Cycles/Triggers register up to 32k per channel of 32bit data.
When the programmed number of triggers as set in the Number of Triggers register has occurred and the sequence completed, the Finished Flag (FF) in the CSR is set and an interrupt is generated if enabled.

- Gate/Bin advance by internal timer or programmable number external pulses (1 to 65525).
- Internal Gate (time) intervals may be programmed from 100usec to 65secs
- Number of cycles register determines number of add-to-memory cycles upto 32K per channel 32bit counter data.

2.3 Preset Scaler Mode

In this mode the counters are loaded with a preset count value. An arbitrary channel or a combination of channels can then be selected as the condition for the termination of the counting process for all counters. The selection of the channel(s) is done via the Count Termination Mask Register. The first selected channel that reaches its preset value will terminate the counting process and sets the FF flag in the CSR.
The individual counters can be driven from external inputs or from an internal pulse generator (selected by the Counter Source register). The internal pulse generator can be set to the following frequencies 25MHz, 50MHz, 100MHz or 200MHz.

3. Product Specifications

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of channels:	16
Max. count:	32 bits with IRQ at end of programmed number of cycles.
Data format:	Binary
Count rate TTL:	0 to 100Mpps
Count rate LVDS:	0 to 200Mpps
Coincidence:	2ns min. overlap for detection
Scaler Input levels:	TTL compatible with positive or negative edge clocking or LVDS 3.3V.
Trigger/Reset levels:	External Trigger Input. TTL compatible settable active low or active high options.
Trigger Delay:	the maximum Trigger delay due to internal logic is 25ns.
Trigger Output levels:	Trigger Output for synchronisation of modules. TTL compatible settable active low or active high options.
Clock accuracy:	+/-50ppm (0.005%)
Power:	+5V @ 250mA typical

4. Logic Signal levels

The configuration of the logic types are indicated in the 8522 ID ROM at Base+98.
Logic Type 0000h = Standard logic setup with LVDS.
Logic Type 0001h = Standard logic setup with LTTL.
Note: Other logic types may be possible, please consult Newwood Solutions ltd

Standard Configuration of Logic Level Signals for LVDS Inputs (Logic Type 0000h)
Scaler Input levels: LVDS 3.3V.
Trigger/Reset levels: LTTL
Trigger Output levels: LTTL
The jumper J1 (Pull up/pull down voltage select) should **not** have a jumper fitted. Pull up and Pull down resistors need to be implemented externally as required for the Trigger, Reset and Tigger Out.
Trigger IN and External Reset can be set via the TTL level register to accept active low LVTTL External pull up required or active high LVTTL External pull down required. Trigger Output driven from Trigger IN.

Standard Configuration of Logic Level Signals for LTTL Inputs (Logic Type 0001h)
Scaler Input levels: LTTL.
Trigger/Reset levels: LTTL
Trigger Output levels: LTTL
The Scaler Inputs, Trigger IN and External Reset can be set via the TTL level register to accept active low LVTTL (Jumper **J1** set in **pull up** position or External pull up required). Or active high LVTTL (Jumper **J1** set in **pull down** position or External pull down required).
Trigger Output driven from Trigger IN.

User Set TTL Logic Level
The user can set TTL logic levels as required by removing J1 and providing external pull up/down resisters. The TTL level register must be set accordingly.

The logic lines for the scaler inputs, external triggers, external trigger enable and reset logic signals can be:

- LTTL compatible with positive/negative edge clocking.
- LVDS 3.3V.
- A mixture of both as required.

Note: The required configuration standard needed or if different logic signal levels from standard configuration are required, must be specified when ordering. The unit can be reconfigured in the field via the JTAG port if requirements change.

5. Histogram and Straight Scaler Operating Modes

5.1 Histogram Mode (MD0='0' in CSR)

5.1.1 Basic Histogram Mode

The counters and memory can be reset to zero using the Reset bit (see CSR section) Then the memory depth and number of cycles need to be set as required.
The gate interval can be internally generated by writing to the Gate Interval register. Or can advance to the next time bin via the External Bin Advance (EBA) input. The external bin advance occurs on every N'th external pulse as set by the value set in the Gate Interval register.
When a trigger occurs the counters are automatically cleared to zero. The counters then count input pulses for an interval generated by the Gate Interval register. At the end of the interval all scaler contents are added to the first memory location for that channel and the gate interval restarted. The scalers count for the next interval and at the end of that interval the contents are added to the next memory location. This is repeated until the preset number of gates as set in the Number of Gates register has been reached. A new trigger will start the next cycle wherein the scaler contents are repeatedly added to memory at the end of each gate interval.
The memory pointer holds the start address for the next 16x64bit data address.
When the programmed number of cycles as set in the Number of Cycles register have been triggered and the sequence completed the Finished Flag (FF) in the CSR is set and an interrupt is generated if enabled.
There are sixteen 64 bit totalisers which record the total count for each channel.
A Trigger can be Hardware generated if 'ET' set in the CSR .

This diagram shows the memory lay out for one channel where the scaler registers are set as below:
Gate Interval: 16 Nos Cycles (Triggers): 10 Number of Gates: 7

This is memory layout for a single channel								
Number of Cyc/Trigs Hard/Soft	Gate Open Time set by Gate Interval Reg							Cycle/Trig Totaliser 64 bits (FPGA)
	1st 16ms gate open	2nd 16ms gate open	3rd 16ms gate open	4th 16ms gate open	5th 16ms gate open	6th 16ms gate open	7th 16ms gate open	
10th Trig Cyc 10	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	
9th Trig Cyc 9	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	
8th Trig Cyc 8	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	
7th Trig Cyc 7	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	
6th Trig Cyc 6	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	
5th Trig Cyc 5	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	
4th Trig Cyc 4	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	
3rd Trig Cyc 3	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	NC= Total=	
2nd Trig Cyc 2	NC=23 Total=75	NC=2 Total=55	NC=4 Total=46	NC=7 Total=46	NC=5 Total=25	NC=1 Total=81	NC=0 Total=95	424
1st Trig Cyc 1	NC=52 Total=52	NC=53 Total=53	NC=42 Total=42	NC=39 Total=39	NC=20 Total=20	NC=80 Total=80	NC=95 Total=95	381
Set by Nos Cycles Reg	Time Bin 1	Time Bin 2	Time Bin 3	Time Bin 4	Time Bin 5	Time Bin 6	Time Bin 7	
	External Memory Locations Nos Bins per trigger up to 16K 64bit words per channel Set by Nos Gates per Cycle Reg							

Each bin has a 32bit counter and a 64bit totaliser. The bin totaliser is stored in external RAM.
The maximum number of bins per channel is 16K.

5.1.2 Histogram Coincidence Mode

This is the same as histogram mode but where inputs which match the patterns set in the channel coincidence registers will increment the counters. Coincidence mode is enabled by setting the EC bit in the CSR, then inputs are AND gated with the Coincidence registers and if true increment the scaler for that channel. The minimum time of overlap required is 2ns min to ensure coincidence triggering. Note: If the pattern in the coincidence register is zero, then when the scaler inputs all go to zero, it does **not** give a count.
If a channel input is disabled then it will always read as zero in the pattern in the coincidence mode and the coincidence counter for that channel will always read zero.

5.1.3 Memory Layout for Histogram Mode

Time Bin Memory
The External 1M x 16 bit RAM memory contains the sixteen groups of time bins organised as up to 16K 64 bit time bins for each channel.
This memory is accessed when the ETM bit in the CSR is set to '0'.

Organisation of Time Bin Data in External RAM Memory

1M x 16 bits memory External RAM	
Memory allocation 16 Bit	**IP Card Address CSR 15='0'**
16K x64bit time bins for channel 16	Base + 960K
16K x64bit time bins for channel 15	Base + 896K
16K x64bit time bins for channel 14	Base + 832K
16K x64bit time bins for channel 13	Base + 768K
16K x64bit time bins for channel 12	Base + 704K
16K x64bit time bins for channel 11	Base + 640K
16K x64bit time bins for channel 10	Base + 576K
16K x64bit time bins for channel 9	Base + 512K
16K x64bit time bins for channel 8	Base + 448K
16K x64bit time bins for channel 7	Base + 384K
16Kx64bit time bins for channel 6	Base + 320K
16Kx64bit time bins for channel 5	Base + 256K
16Kx64bit time bins for channel 4	Base + 192K
16Kx64bit time bins for channel 3	Base + 128K
16Kx64bit time bins for channel 2	Base + 64K
16Kx64bit time bins for Channel 1 Time Bin 16K MSW 16 bit Time Bin 16K Third 16 bit word Time Bin 16K Second 16 bit word Time Bin 16K LSW 16 bit: : : : Time Bin 1 MSW 16 bit Time Bin 1 Third 16 bit word Time Bin 1 Second 16 bit word Time Bin 1 LSW 16 bit	Base + 0K

Totaliser Memory

Organisation of the sixteen 64 bit totaliser registers in FPGA RAM Memory
64 bit words for the totaliser values are read as four 16 bit words from the IP ram memory
This memory is accessed when the ETM bit in the CSR is set to '1'.

16 x 64 bits FPGA RAM memory	
Memory allocation	**IP Card Address CSR 15='1'**
Channel 16 Totaliser 64bits	Base + 60
Channel 15 Totaliser 64bits	Base + 56
Channel 14 Totaliser 64bits	Base + 52
Channel 13 Totaliser 64bits	Base + 48
Channel 12 Totaliser 64bits	Base + 44
Channel 11 Totaliser 64bits	Base + 40
Channel 10 Totaliser 64bits	Base + 36
Channel 9 Totaliser 64bits	Base + 32
Channel 8 Totaliser 64bits	Base + 28
Channel 7 Totaliser 64bits	Base + 24
Channel 6 Totaliser 64bits	Base + 20
Channel 5 Totaliser 64bits	Base + 16
Channel 4 Totaliser 64bits	Base + 12
Channel 3 Totaliser 64bits	Base + 8
Channel 2 Totaliser 64bits	Base + 4
Channel 1 Totaliser 64bits Most significant 16 bits of 64 bit word Third 16 bit word Second 16 bit word Least significant 16 bits of 64 bit word	Base + 0

5.2 Straight Scaler Mode (MD0='1' in CSR)

In this mode the time the gate is open is set using the gate Interval register. The period of the gate interval is controlled by the gate interval register setting the number of internally generated 100us or 1ms pulses.
The gate interval can also be controlled externally by setting the EBA bit in the CSR. Here the timing pulses are user defined and received via the trigger input.
When the gate interval is finished the counter values are loaded in memory. The number of logged values is set in the Nos Cycles/Triggers register.
When the programmed number of triggers as set in the Number of Triggers register has occurred and the sequence completed, the Finished Flag (FF) in the CSR is set and an interrupt is generated if enabled.
The current memory address is given by the Memory pointer registers LSW and MSW.
The memory pointer holds the start address for the next 16x32bit data address.

5.2.1 Memory Layout Straight Scaler Mode

512K x 32 bits memory External RAM		
Nos Triggers	**Memory allocation 32bits**	**IP Card Address CSR 15='0'**
32k	Chan 16	Base +
32k	Chan 15	Base +
32k	Chan 3	Base +
32k	Chan 2	Base +
32k	Chan 1	Base +
2	Chan 16	Base +60
2	Chan 15	Base +58
2	Chan 2	Base +34
2	Chan 1	Base +32
1	Chan 16	Base +30
1	Chan 15	Base +28
1	Chan 3	Base +4
1	Chan 2	Base +2
1	Chan 1	Base +0

5.3 Automated Memory Clear

Both internal FPGA RAM and external RAM are automatically cleared by issuing a Reset (R) in the CSR (bit 1). Or if the Enable External Reset bit (ER bit 4) is set and the External reset pin is taken high.
The CSR bit 1 indicates when clear memory routine has started='1' and finished='0' for both hardware and software resets clears.
It takes approx 80ms for the whole of the external ram memory to be cleared.

5.4 Application Registers Histogram and Straight Scaler

Application Register Table

Byte Addressing		Word Addressing		16 Bit Application Registers
Hex	***Dec***	***Hex***	***Dec***	
0 – 3E	0 – 62	28 – 1F	0 – 31	32 bit Shadow Counting registers chans 1 to 16
40 – 5E	64 – 94	20 – 2F	32 – 47	Coincidence Registers chans 1 to 16
60	96	30	48	CSR
62	98	31	49	Gate Interval Reg
64	100	32	50	Number of cycles
66	102	33	51	Nos Gates per cycle (memory depth)
68	104	34	52	Overflow register
6A	106	35	53	Nos “cycles” and/or triggers received
6C	108	36	54	Interrupt Vector register
6E	110	37	55	Interrupt Enable /disable
70	102	38	56	Memory pointer LSB
72	104	39	57	Memory pointer MSB
74	106	3A	58	Mask Channel Input
76	108	3B	59	Change of Function Register
78	110	3C	60	Select TTL level when card configured for TTL
7A	112	3D	61	NOT USED
7C	114	3E	62	Counter Source

5.4.1 Counting Registers (I/O Address 0-31)

Counter Shadow Registers 0 to 15 are held in the I/O space of the IP scaler card.
The counter registers may be read at addresses 00-1E (even) for the least significant words

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0

and 01-1F(odd) for the most significant words.

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16

Both these registers are cleared when a reset is issued.

5.4.2 Coincidence Registers (I/O Address 32-47)

Read/write register
Coincidence Registers 0 to 15 are held in the I/O space of the IP scaler card.
The coincidence registers may be read at addresses 20-2F

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

Each scaler has an AND coincidence pattern for the 16 inputs which operates when EC is a ‘1’.

5.4.3 Control & Status Register (CSR I/O Address 48)

Read/write register
Control and Status bits.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ETM	TS1	TS0	EBA	EXET	-	MD0	TM	FF	EC	ST	ER	ET	IE	R	IRQ

IRQ Interrupt Request, generated when the programmed number of cycles/triggers is reached. (Read only).
R Reset - writing a 1 to this bit resets all the counters and memory to zero. This bit also indicates when clear memory routine has started='1' and finished='0' for both hardware and software memory clears.
IE Interrupt enable enables IRQ to generate interrupt when set to a '1'.
ET Enable Hardware TRIGGER IN from Transition board to initiate each acquisition cycle.
ER Enable Reset . Enables external hardware reset to clear scalers and memory.
ST Software TRIGGER initiates a single acquisition cycle.
EC Enable coincidence. The coincidence patterns are AND gated to increment the appropriate scalers (Coincidence register 20 increments scaler 1 if the AND is true).
FF Finish flag set when the number of cycles/triggers reached. (read only).
TM Sets the interval timer multiples from 1ms to 100us in Gate Interval Register.
MD This bit set the mode of the unit.

MD 0	MODE TYPE
0	Histogram
1	Straight Scaler

EXET Enable External Trigger Enable
EBA Enable External time Bin Advance (EBA).
TSx Selects a "00"=25MHz, "01"=50MHz, "10"=100MHz or "11"=200MHz test input to counters.
ETM Enable Totaliser memory.

5.4.4 Gate Interval (Bin Advance) Register (I/O address 49)

Read/write register.
When EBA in the CSR set to '0' specifies the count for the gate interval timer in multiples of 1msec (1 to 65535ms) when TM='0' in CSR or in multiples of 100us (100us – 6553.5ms) when TM='1' in CSR.
When EBA in CSR set to '1' then the gate interval register sets then number of external pulses from the Trig/EBA input to set the gate interval (Bin advance).
The Trig/EBA input can be up to 20MHz, but with the restriction that the combination of the rate and the number of divides as set by the register is no shorter than the minimum allowed dwell time of the device (see relevant section on Dwell times).
If zero or one is entered will count for one gate interval.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

5.4.5 Number of Cycles\Triggers Register (I/O address 50)

Read/write register.
Specifies the number of cycles in Histogram mode (C) or the number triggers in straight scaler mode. In straight scaler mode (T) can have up to 32K of 32bit data for each channel. If zero is entered unit will not start in either mode.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
-	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

5.4.6 Number of Gates per cycle (memory depth) Register (I/O address 51)

Read/write register.
Specifies the number of time bins (gates) per cycle in Histogram mode. Each channel can have a maximum of 16k-1 64bit bins. In Scaler mode this register is not used.
If zero is entered in Histogram mode unit will not start.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
-	-	G13	G12	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0

5.4.7 Overflow Register (I/O address 52)

Read/write register.
The overflow from each scaler is latched. When a bit is set it indicates scaler overflow. Writing a ‘1 to a bit will clear the Overflow bit for that channel. Writing a zero changes nothing. Reset also clears this register.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
O15	O14	O13	O12	O11	O10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0

5.4.8 Nos "Cycles" and/or Triggers Received Register (IP address 53)

Read Only register.
Number of "cycles" and/or triggers received. This register is cleared when the number of cycles register (addr 50) is cleared. It is also cleared when an internal Reset (bit1 CSR) is set or an external reset is issued.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
TR15	TR14	TR13	TR12	TR11	TR10	TR9	TR8	TR7	TR6	TR5	TR4	TR3	TR2	TR1	TR0

5.4.9 Interrupt Vector Register (I/O address 54)

Read/write register.
Defines the interrupt vector.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

5.4.10 Interrupt Disable Register (I/O address 55)

Read/write register.
Writing a '1' to bit zero causes the Interrupt Enable bit 'IE' in the CSR to be cleared.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CIE

5.4.11 Memory pointer LSW Register (I/O address 56)

Read register.
LSW of memory pointer when in scaler mode.
In Histrgram mode the memory pointer holds the start address for the next 16x64bit data address.
In Straight and Prescler mode the memory pointer holds the start address for the next 16x32bit data address.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

5.4.12 Memory pointer MSW Register (I/O address 57)

Read register.
MSW of memory pointer when in scaler mode.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
-	-	-	-	-	-	-	-	-	-	-	-	A19	A18	A17	A16

5.4.13 Mask Channel Input (I/O address 58)

Write register.
Disable channels

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
DC15	DC14	DC13	DC12	DC11	DC10	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0

Write a ‘1’ to disable a channel i.e. DC=’1’ Channel 1 is disabled.

5.4.14 Change of Function Register (I/O address 59)

Read/Write register.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Do Not set	Do Note set					F1	F0	CH				L3	L2	L1	L0

L0 – L3 **This shows the** configuration of the logic types
00 = Standard logic setup with LVDS.
01 = Standard logic setup with LTTL.
Note: Other logic types may be possible, consult Newwood Solutions
CH Change function. This loads the **Preset Scaler** application into FPGA
F0 – F1 This shows which function is loaded in FPGA.
00=Histogram function.
01=Preset scaler function.

5.5 Select TTL level Register (I/O address 60) (Only in version V105 and above)

Read/write register.
This allows the TTL logic level of the unit to be set

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
												PS 3	PS 2	PS 1	PS0

PS0 This sets Trigger to accept active high LVTTL when ‘0’ or active Low LVTTL when ‘1’. **Important Note**: Trigger Output driven from Trigger IN.
PS1 This sets External Reset to accept active high LVTTL when ‘0’ or active Low LVTTL when ‘1’.
PS2 Sets Scaler Inputs to drive active high LVTTL when ‘0’ or active Low LVTTL when ‘1’. This is only applicable when unit is configured for TTL scaler in puts and has no effect when in LVDS mode.
PS3 This sets Trigger Enable to accept active high LVTTL when ‘0’ or active Low LVTTL when ‘1’.

5.5.1 Counter Source (I/O address 62)

Read/write register.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
CS 15	CS 14	CS 13	CS 12	CS 11	CS 10	CS 9	CS 8	CS 7	CS 6	CS 5	CS 4	CS 3	CS 2	CS 1	CS0

Write '1' to select internal counter clock or '0' to selects external input in to the counter for each channel.
The internal counter clock is set by bits 13 and 14 of the CSR:

CSR 14	CSR 13	Internal Counter Clock
0	0	25MHz
0	1	50MHz
1	0	100MHz
1	1	200MHz

5.6 Internal and External Reset

When an internal or external Reset is issued the follow registers and logic are reset.

Scan Enable lines cleared
Nos Cycles and or Triggers Received register is cleared
Memory Cleared both external RAM and FPGA RAM

5.7 External Time Bin Advance (EBA)

The next time bin can be advance to via the External Bin Advance (EBA) input (TRIG/EBA IN). The external bin advance occurs on every N'th external pulse as set by the value in the Gate Interval register.
When the EBA bit in CSR is set to '1' then the gate interval register sets then number of external pulses from the Trig/EBA input to set the gate interval (Bin advance).
The Trig/EBA input can be up to 20MHz, but with the restriction that the combination of the rate and the number of divides as set by the register is no shorter than the minimum allowed dwell time of the device (see relevant section on Dwell times).
The EBA signal comes in on the same pin as the External Trigger so if external trigger bit is set in the CSR then the unit will trigger on the first EBA signal. This first pulse will be counted as part of the EBA count interval.
The unit can alternatively be triggered via software.

5.8 External Trigger enable (version V104 and above)

Here an external line drives the external trigger enable need to set **ExET bit 11 in CSR**. If ET bit 3 is set it has no effect and if the nExtET line is de-asserted then an in put on the external trigger will not be seen.

To enable the unit using external trigger take the nExtET line pin 37 8522 (pin 44 transition card) **Low**. When this line is taken **High** the unit is disabled and an interrupt is generated on INTR0 if enabled.

When a trigger has occurred in this mode **need to clear the ExET bit 11 in CSR** to reset it before another trigger can be seen.

In this mode with the EBA set then the GIT reg holds the number of counts before advancing to the next bin. Important entering '0' will give a count of 1 and 1=2 etc this is same as before.

Example
If signal in to Ext Trig is 1MHz (1us period) and GIT set to 100 then each bin lasts for 100us

Beware minimum Gate interval time is approx 10us (no IP memory reads as this causes dwell time to increase).

The number of gates register still sets the max number of gates before stopping data acquisition and generating an interrupt. This should be set to 0x3FFF this allows the unit to acquire up to its maximum memory depth. Or it can be set to less to stop excessive time wastage if external ET is not de-asserted within a certain time as an interrupt will be generate.
In this mode the software trigger will be ignored and the number of cycles register

5.9 MINIMUM DWELL TIME

The minimum dwell time on the MSC8522 is defined as the time needed to take the data from the 16 counters and form a histogram which is saved in the external RAM memory.
The current design has a Dwell time of approx 10us. This means that if the EBA is 20MHz will need to put in the following calculated value to the EBA registers (GIT):

10us x 20MHz = 200counts min

This may be longer if the memory is being read at the same time see following scenario.

IP Clock 32MHz memory reads every 1200ns Dwell increased to approx !!!!
IP Clock 32MHz memory reads every 800ns Dwell increased to approx !!!!
IP Clock 32MHz memory reads every 500ns Dwell increased to approx !!!!

IP Clock 8MHz memory reads every 1300ns Dwell increased to approx !!!!

6. Preset Scaler

The 8522 can be operated as Preset Scaler. In this mode the counters are loaded with a preset count value. An arbitrary channel or a combination of channels can then be selected as the condition for the termination of the counting process for all counters. The selection of the channel(s) is done via the **Count Termination Mask Register**. The first selected channel that reaches its preset value will terminate the counting process and sets the FF flag in the CSR.
The preset values are defined by pre loading the counters.
If no counters are selected by the Count Termination on Preset Mask Register then the counters will all count to there preset value and stop.
All counters which have reached there preset count value will set the relevant bit in the Preset Hit register and stop.

The individual counters can be driven from external inputs or from an internal pulse generator (selected by the counter source register). The internal pulse generator can be set to the following frequencies (using bits D14 and D13 of the CSR) 25MHz, 50MHz, 100MHz or 200MHz.

It should be noted that the stopping of the counters will not be immediate on preset condition being detected but could take upto15ns. This means that the counters may not read zero when frequencies are above 60MHz.

6.1 Setting Value To Load in to Preset Scaler

The counters use the counter overflow to signal when the preset value is reached. Therefore the desired number of counts needs to be first inverted and incremented by 1.

E.g. require a count of 0x100 then 0xFFFFFF00 is loaded in to the counters.

6.2 Application Registers Preset Scaler

Application Register Table

Byte Addressing		**Word Addressing**		**16 Bit Application Registers**
Hex	***Dec***	***Hex***	***Dec***	
0 – 3E	0 – 62	28 – 1F	0 – 31	Write 32 bit preset scaler value chans 1 to 16 Read 32 bit scaler value chans 1 to 16
40 – 5E	64 – 94	20 – 2F	32 – 47	Not used
60	96	30	48	CSR
62	98	31	49	Not used
64	100	32	50	Not used
66	102	33	51	Not used
68	104	34	52	Preset Hit Register
6A	106	35	53	Count Termination Mask register
6C	108	36	54	Interrupt Vector register
6E	110	37	55	Interrupt Enable /disable
70	102	38	56	Not used
72	104	39	57	Not used
74	106	3A	58	ARM channel (enable)
76	108	3B	59	Change of Function Register
78	110	3C	60	Select TTL level when card configured for TTL
7A	112	3D	61	Not used
7C	114	3E	62	Counter Source 0=External 1=Internal

6.2.1 Preset Counting and Shadow Registers (I/O Address 0-31)

Counter Registers 0 to 15 are held in the I/O space of the IP scaler card.
The counter registers may be preloaded and read at addresses 00-1E (even) for the least significant words

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0

and 01-1F(odd) for the most significant words.

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16

Important Note When reading the counters with the Scalers **enable**, both the low and high word of the counter are latched in to the shadow register when the Least significant word is read and not when the most significant word read. This will ensure the correct 32 bit count word is read.

6.2.2 Control & Status Register (CSR I/O Address 48)

Read/write register
Control and Status bits.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
	TS1	TS0						FF	CT	ST	ER	ET	IE	R	IRQ

IRQ Interrupt Request. Ready, generated at the end of the programmed number of cycles or when preset value reached in preset Scaler mode. (Read only).
R Reset - writing a 1 to this bit resets all the counters and memory to zero. This bit also indicates when clear memory routine has started='1' and finished='0' for both hardware and software memory clears.
IE Interrupt enable enables IRQ to generate interrupt when set to a '1'.
ET Enable Hardware TRIGGER IN from Transition board to initiate each acquisition cycle.
ER Enable Reset . Enables external hardware reset to clear scalers and memory.
ST Software TRIGGER enables the counters.
CT This clears the trigger and stops the counters.
FF Finish flag set when a counter(s) (as shown in Preset Hit reg) reach its/there preset value. This flag is cleared when the Preset Hit registers is cleared. (read only).
TSx Selects a "00"=25MHz, "01"=50MHz, "10"=100MHz or "11"=200MHz test input to counters.

6.2.3 Preset Hit Register (I/O address 52)

Read/write register.
The Preset Hit from each scaler is latched. When a bit or bits are set it indicates scaler has reached its preset value.
Writing a '1 to a bit will clear the Preset Hit bit for that channel. Writing a zero changes nothing. This register is also cleared by a Reset.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
O15	O14	O13	O12	O11	O10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0

6.2.4 Count Termination Mask Register (IP address 53)

Read/Write register.
This register selects which channel(s) will terminate the counting process when the preset value is reached (the first selected counter to reach its preset value will terminate the counting process for all channels) and generate an interrupt.
Enable Interrupt on channel when it reaches its preset value.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
TR15	TR14	TR13	TR12	TR11	TR10	TR9	TR8	TR7	TR6	TR5	TR4	TR3	TR2	TR1	TR0

6.2.5 Interrupt Vector Register (I/O address 54)

Read/write register.
Defines the interrupt vector.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

6.2.6 Interrupt Disable Register (I/O address 55)

Read/write register.
Writing a '1' to bit zero causes the Interrupt Enable bit 'IE' in the CSR to be cleared.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CIE

6.2.7 ARM Channel Input (I/O address 58)

Write register.
Write a ‘1’ to ARM a channel.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
DC15	DC14	DC13	DC12	DC11	DC10	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0

6.2.8 Change of Function Register (I/O address 59)

Read/Write register.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Do Not set	Do Note set							CH						F1	F0

F0 – F1 This shows which function is loaded in FPGA.
00=Histogram function.
01=Preset scaler function.
CH Change function. This loads the **Histogram application** into FPGA

6.2.9 Select TTL level (I/O address 60)

Read/write register.
This allows the TTL logic level of the unit to be set

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
													PS2	PS1	PS0

PS0 This sets Trigger to accept active high LVTTL when ‘0’ or active Low LVTTL when ‘1’. Trigger Output driven from Trigger IN.
PS1 This sets External Reset to accept active high LVTTL when ‘0’ or active Low LVTTL when ‘1’.
PS2 Sets Scaler Inputs to drive active high LVTTL when ‘0’ or active Low LVTTL when ‘1’. This is only applicable when unit is configured for TTL scaler in puts and has no effect when in LVDS mode.

6.2.10 Counter Source (I/O address 62)

Read/write register.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
CS 15	CS 14	CS 13	CS 12	CS 11	CS 10	CS 9	CS 8	CS 7	CS 6	CS 5	CS 4	CS 3	CS 2	CS 1	CS0

Write '1' to select internal counter clock or '0' to selects external input in to the counter for each channel.
The internal counter clock is set by bits 13 and 14 of the CSR:

CSR 14	CSR 13	Internal Counter Clock
0	0	25MHz
0	1	50MHz
1	0	100MHz
1	1	200MHz

6.3 Internal and External Reset Preset Scaler Mode

When an internal or external Reset is issued the follow registers and logic are reset.

Scan Enable lines cleared and scanning stopped.
All counters and shadow registers are cleared to zero.
The Overflow register is cleared.
Finish flag **(**FF) in CSR cleared.

7. ID PROM

The 8522 IP module includes a configuration ID PROM. The ID information held in the PROM is as detailed below.

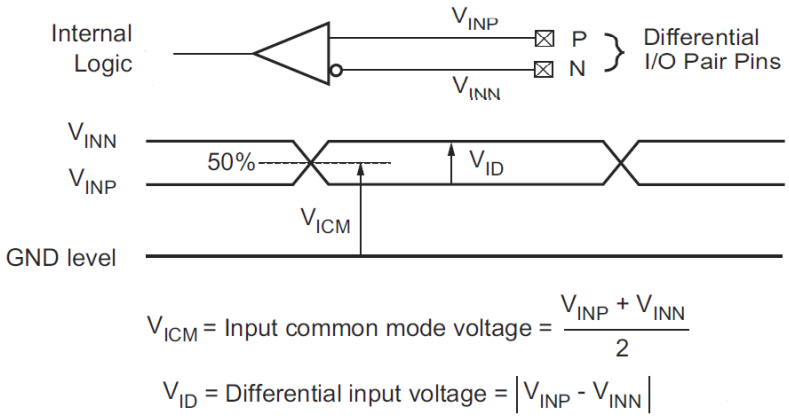
The byte addresses of the ID PROM are as below:-

Base+80	ASCII 'VI'	5649h	
Base+82	ASCII 'TA'	5441h	
Base+84	ASCII '4 '	3420h	
Base+86	Mfr ID high byte	0080h	
Base+88	Mfr ID low word	0300h	
Base+8A	Model number	8522h	
Base+8C	Revision	1101h	This shows PCB Issue 1 and Xilinx V103 means FPGA at issue 3 and PCB at issue 1.
Base+8E	Reserved	0000h	
Base+90	Driver ID	0000h	
Base+92	Driver ID	0000h	
Base+94	Flags	0002h	
Base+96	No of bytes used	001Ah	
Base+98	Funtion/Logic Type	Histogram 00xxh Preset Scaler 01xxh	
Base+9A	Serial Number	xxxxdec	

Logic Type xx00h = Standard logic setup with LVDS.
Logic Type xx01h = Standard logic setup with LTTL.
Note: Other logic setups may be defined later.

Logic Type x0xxh = Histogram.
Logic Type 01xxh = Scaler .
Note: Other setups may be defined later.

8. I/O Standards Input Configuration.



Differential Input Voltages

Recommended Operating Conditions for User I/Os Using Differential Signal Standards

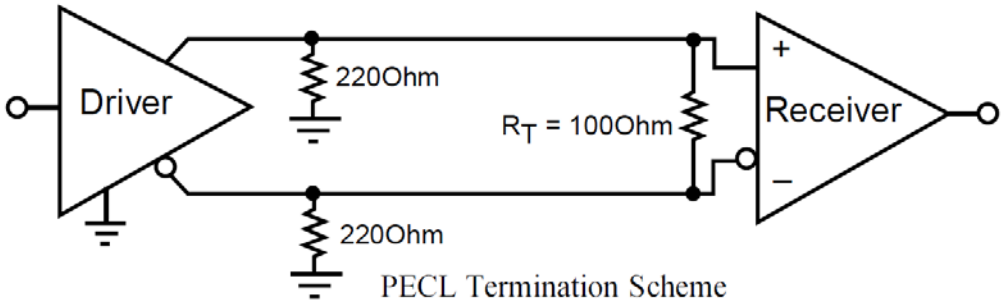
IOSTANDARD Attribute	VID			VICM		
	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_33	100	350	600	0.3	1.25	2.35
LVPECL	100	800	1000	0.3	1.2	1.5

8.1 LVPECL — Low Voltage Positive Emitter Coupled Logic

Differential I/O standard with a voltage swing between two signal lines of approximately 850 mV. The use of a reference voltage (VREF) or a board termination voltage (VTT) is not required.

Important Note

The LVPECL standard requires external 220Ohm resistor termination which is not implemented on the 8522 module.

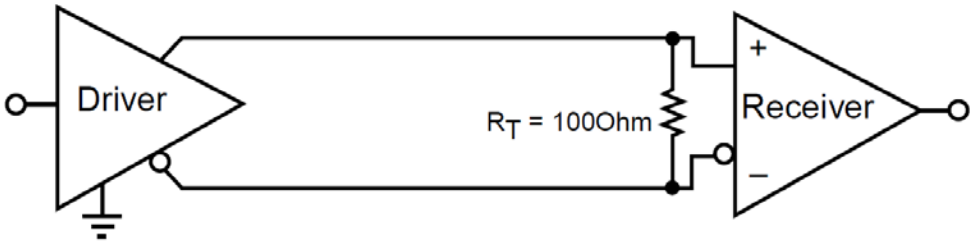


PECL Termination Scheme

The100ohm resistor termination is implemented on the unit.

8.2 LVDS — Low Voltage Differential Signal

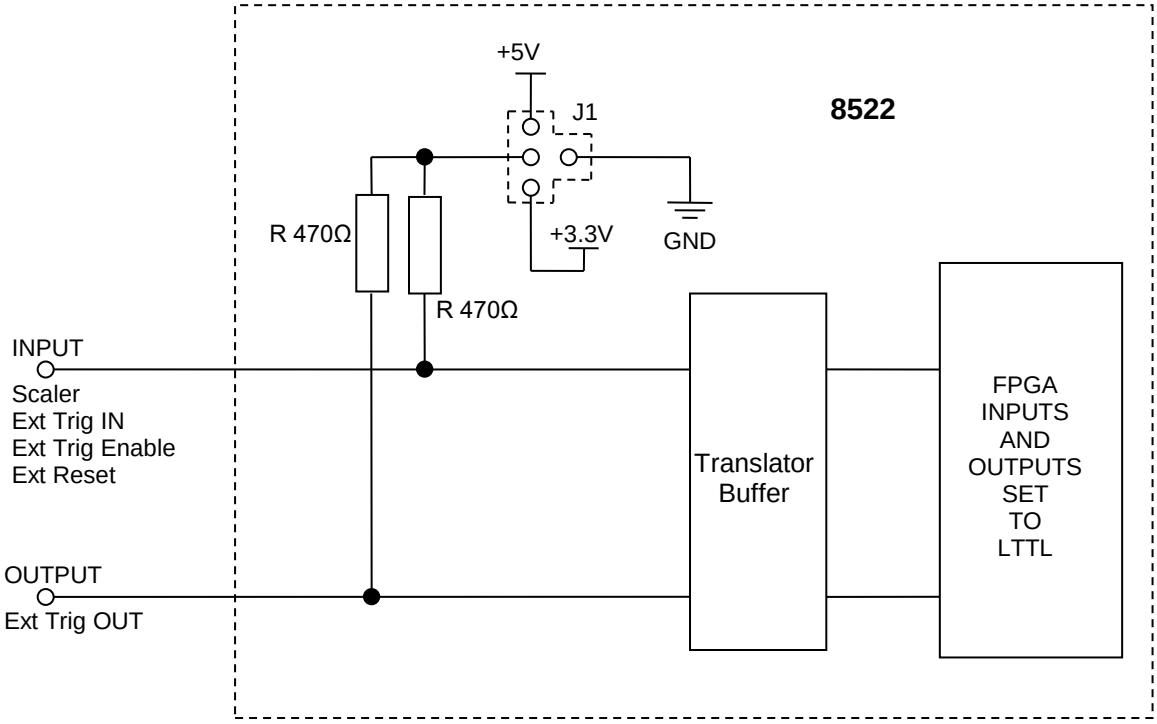
LVDS is a differential I/O standard. As with all differential signaling standards, LVDS requires that one data bit is carried through two signal lines, and it has an inherent noise immunity over single-ended I/O standards. The voltage swing between two signal lines is approximately 350 mV. The use of a reference voltage (VREF) or a board termination voltage (VTT) is not required. LVDS requires the use of two pins per input or output. LVDS has onboard 100ohm resistor termination implemented in FPGA on the unit.



LVDS Termination Scheme

8.3 J1 Pull-up or Pull-down For TTL Logic Signals

The jumper J1 allows the user to pull-up to 3.3V or 5V or pull-down to ground.



APPENDIX A

I/O Connector – 50 way on 8522 Scaler Board

Pin	Signal	Pin	Signal
1	IO1_P1	26	IO26_N13
2	IO2_N1	27	IO27_P14
3	IO3_P2	28	IO28_N14
4	IO4_N2	29	IO29_P15
5	IO5_P3	30	IO30_N15
6	IO6_N3	31	IO31_P16
7	IO7_P4	32	IO32_N16
8	IO8_N4	33	IO33_P17_ExtRST
9	IO9_P5	34	IO34_N17
10	IO10_N5	35	IO35_P18_TRIGOUT
11	IO11_P6	36	IO36_N18
12	IO12_N6	37	IO37_IP19_ExtTrigEnIN
13	IO13_P7	38	IO38_IN19
14	IO14_N7	39	IO39_IP20_TRIGIN
15	IO15_P8	40	IO40_IN20
16	IO16_N8	41	GND #
17	IO17_P9	42	IO41
18	IO18_N9	43	GND #
19	IO19_P10	44	IO42
20	IO20_N10	45	GND #
21	IO21_P11	46	IO43
22	IO22_N11	47	GND #
23	IO23_P12	48	IO44
24	IO24_N12	49	GND
25	IO25_P13	50	GND

Signal Naming Key:
IO5_P3 = can be single ended logic I/O chan 5 or positive of LVDS chan 3 I/O.
IO6_N3= can be single ended logic I/O chan 6 or negitive of LVDS chan 3 I/O.

.

Some channels have dedicated functionality and signal names i.e. IO35_P18_**TRIGOUT**.

APPENDIX B

NEWWOOD SOLUTIONS TRANSITION 8304 CARD CONNECTIONS FOR LVDS 3.3V INPUTS

I/O Connector – 50 way on transition

Card 8304 Where this feeds ONE IP sites

Pin Trans	Pin 8522	Signal	Pin Trans	Pin 8522	Signal
1	*2*	IO2_N1	26	*1*	IO1_P1
2	*4*	IO4_N2	27	*3*	IO3_P2
3	*6*	IO6_N3	28	*5*	IO5_P3
4	*8*	IO8_N4	29	*7*	IO7_P4
5	*10*	IO10_N5	30	*9*	IO9_P5
6	*12*	IO12_N6	31	*11*	IO11_P6
7	*14*	IO14_N7	32	*13*	IO13_P7
8	*16*	IO16_N8	33	*15*	IO15_P8
9	*18*	IO18_N9	34	*17*	IO17_P9
10	*20*	IO20_N10	35	*19*	IO19_P10
11	*22*	IO22_N11	36	*21*	IO21_P11
12	*24*	IO24_N12	37	*23*	IO23_P12
13	*26*	IO26_N13	38	*25*	IO25_P13
14	*28*	IO28_N14	39	*27*	IO27_P14
15	*30*	IO30_N15	40	*29*	IO29_P15
16	*32*	IO32_N16	41	*31*	IO31_P16
17	*34*	Not Used	42	*33*	Ext RST
18	*36*	Not Used	43	*35*	TRIG/EBA OUT
19	*38*	Not Used	44	*37*	Not Used
20	*40*	Not Used	45	*39*	TRIG/EBA IN
21	*42*	Not Used	46	*41*	GND
22	*44*	Not Used	47	*43*	GND
23	*46*	Not Used	48	*45*	GND
24	*48*	Not Used	49	*47*	GND
25	*50*	GND	50	*49*	GND

APPENDIX C

NEWWOOD SOLUTIONS TRANSITION 8304 CARD CONNECTIONS FOR TTL INPUTS

I/O Connector – 50 way on transition

Card 8304 Where this feeds ONE IP sites

Pin Trans	Pin 8522	Signal	Pin Trans	Pin 8522	Signal
1	*2*	Not Used	26	*1*	IO1_P1
2	*4*	Not Used	27	*3*	IO3_P2
3	*6*	Not Used	28	*5*	IO5_P3
4	*8*	Not Used	29	*7*	IO7_P4
5	*10*	Not Used	30	*9*	IO9_P5
6	*12*	Not Used	31	*11*	IO11_P6
7	*14*	Not Used	32	*13*	IO13_P7
8	*16*	Not Used	33	*15*	IO15_P8
9	*18*	Not Used	34	*17*	IO17_P9
10	*20*	Not Used	35	*19*	IO19_P10
11	*22*	Not Used	36	*21*	IO21_P11
12	*24*	Not Used	37	*23*	IO23_P12
13	*26*	Not Used	38	*25*	IO25_P13
14	*28*	Not Used	39	*27*	IO27_P14
15	*30*	Not Used	40	*29*	IO29_P15
16	*32*	Not Used	41	*31*	IO31_P16
17	*34*	Not Used	42	*33*	Ext RST
18	*36*	Not Used	43	*35*	TRIG/EBA OUT
19	*38*	Not Used	44	*37*	Ext Trig Enable IN *
20	*40*	Not Used	45	*39*	TRIG/EBA IN
21	*42*	Not Used	46	*41*	GND
22	*44*	Not Used	47	*43*	GND
23	*46*	Not Used	48	*45*	GND
24	*48*	Not Used	49	*47*	GND
25	*50*	GND	50	*49*	GND

*** From Histogram Mode LVDS\TTL firmware V104 onwards**

APPENDIX D

VME64X PIN ASSIGNMENT ON NEWWOOD SOLUTIONS 8802/4 IP CARRIER BOARD FOR MCS8522

VME64X PIN ASSIGNMENT ON HYTEC 8002/4 IP CARRIER BOARD FOR MCS8522

ROW A	SIG	ROW B	SIG	ROW C	SIG	ROW D	SIG	ROW E	SIG	ROW F	SIG
P0.A01	D Chan 1+	P0.B01	D Chan 1-	P0.C01	D Chan 2+	P0.DO1	D Chan 2 -	P0.E01	D Chan 3+	P0.F01	GND
P0.A02	D Chan 3 -	P0.B02	D Chan 4+	P0.C02	D Chan 4 -	P0.D02	D Chan 5+	P0.E02	D Chan 5 -	P0.F02	GND
P0.A03	D Chan 6+	P0.B03	D Chan 6 -	P0.C03	D Chan 7+	P0.D03	D Chan 7 -	P0.E03	D Chan 8+	P0.F03	GND
P0.A04	D Chan 8 -	P0.B04	D Chan 9+	P0.C04	D Chan 9 -	P0.D04	D Chan 10 +	P0.E04	D Chan 10 -	P0.F04	GND
P0.A05	D Chan 11+	P0.B05	D Chan 11 -	P0.C05	D Chan 12 +	P0.D05	D Chan 12 -	P0.E05	D Chan 13 +	P0.F05	GND
P0.A06	D Chan 13 -	P0.B06	D Chan 14 +	P0.C06	D Chan 14 -	P0.D06	D Chan 15 +	P0.E06	D Chan 15 -	P0.F06	GND
P0.A07	D Chan 16+	P0.B07	D Chan 16 -	P0.C07	N/C	P0.D07	N/C	P0.E07	D XTrigger	P0.F07	GND
P0.A08	D/XTrigger	P0.B08	N/C	P0.C08	N/C	P0.D08	D XCLK	P0.E08	D /XCLK	P0.F08	GND
P0.A09	D +12V	P0.B09	D AGND	P0.C09	D +12V	P0.D09	D AGND	P0.E09	D -12V	P0.F09	GND
P0.A10	D AGND	P0.B10	D -12V	P0.C10	D AGND	P0.D10	N/C	P0.E10	D AGND	P0.F10	GND
P0.A11	C Chan 1+	P0 B11	C Chan 1 -	P0.C11	C Chan 2+	P0.D11	C Chan 2 -	P0 E11	C Chan 3+	P0.F11	GND
P0.A12	C Chan 3 -	P0.B12	C Chan 4+	P0.C12	C Chan 4 -	P0.D12	C Chan 5+	P0.E12	C Chan 5 -	P0.F12	GND
P0.A13	C Chan 6+	P0.B13	C Chan 6-	P0.C13	C Chan 7+	P0.D13	C Chan 7 -	P0.E13	C Chan 8+	P0.F13	GND
P0.A14	C Chan 8-	P0.B14	C Chan 9+	P0.C14	C Chan 9-	P0.D14	C Chan 10+	P0.E14	C Chan 11+	P0.F14	GND
P0.A15	C Chan 11+	P0.B15	C Chan 11-	P0.C15	C Chan 12+	P0.D15	C Chan 12-	P0.E15	C Chan 13+	P0.F15	GND
P0.A16	C Chan 13-	P0.B16	C Chan 14+	P0.C16	C Chan 14-	P0.D16	C Chan 15+	P0.E16	C Chan 15-	P0.F16	GND
P0.A17	C Chan 16+	P0.B17	C Chan 16-	P0.C17	N/C	P0.D17	N/C	P0.E17	C XTrigger	P0.F17	GND
P0.A18	C/XTrigger	P0.B18	N/C	P0.C18	N/C	P0.D18	C XCLK	P0.E18	C /XCLK	P0.F18	GND
P0.A19	C +12V	P0.B19	C AGND	P0.C19	C +12V	P0.D19	C AGND	P0.E19	C -12V	P0.F19	GND

P0 pin assignment

P1 ROW A	SIGNAL	P1 ROW B	SIGNAL	P1 ROW C	SIGNAL	P1 ROW D	SIGNAL	P1 ROW Z	SIGNAL
P1.A01	D00	P1.B01	N/C	P1.C01	D08	P1.D01	N/C	P1.Z01	N/C
P1.A02	D01	P1.B02	N/C	P1.C02	D09	P1.D02	N/C	P1.Z02	GND
P1.A03	D02	P1.B03	N/C	P1.C03	D10	P1.D03	N/C	P1.Z03	N/C
P1.A04	D03	P1.B04	BG0IN*	P1.C04	D11	P1.D04	N/C	P1.Z04	GND
P1.A05	D04	P1.B05	BG0OUT*	P1.C05	D12	P1.D05	N/C	P1.Z05	N/C
P1.A06	D05	P1.B06	BG1IN*	P1.C06	D13	P1.D06	N/C	P1.Z06	GND
P1.A07	D06	P1.B07	BG1OUT*	P1.C07	D14	P1.D07	N/C	P1.Z07	N/C
P1.A08	D07	P1.B08	BG2IN*	P1.C08	D15	P1.D08	N/C	P1.Z08	GND
P1.A09	GND	P1.B09	BG2OUT*	P1.C09	GND	P1.D09	N/C	P1.Z09	N/C
P1.A10	N/C	P1.B10	BG3IN*	P1.C10	N/C	P1.D10	N/C	P1.Z10	GND
P1.A11	GND	P1.B11	BG3OUT*	P1.C11	BERR*	P1.D11	N/C	P1.Z11	N/C
P1.A12	DS1*	P1.B12	N/C	P1.C12	RESET	P1.D12	+3.3V	P1.Z12	GND
P1.A13	DS0*	P1.B13	N/C	P1.C13	LWORD*	P1.D13	N/C	P1.Z13	N/C
P1.A14	WRITE	P1.B14	N/C	P1.C14	AM5	P1.D14	+3.3V	P1.Z14	GND
P1.A15	GND	P1.B15	N/C	P1.C15	A23	P1.D15	N/C	P1.Z15	N/C
P1.A16	DTACK*	P1.B16	AM0	P1.C16	A22	P1.D16	+3.3V	P1.Z16	GND
P1.A17	GND	P1.B17	AM1	P1.C17	A21	P1.D17	N/C	P1.Z17	N/C
P1.A18	AS	P1.B18	AM2	P1.C18	A20	P1.D18	+3.3V	P1.Z18	GND
P1.A19	GND	P1.B19	AM3	P1.C19	A19	P1.D19	N/C	P1.Z19	N/C
P1.A20	IACK	P1.B20	GND	P1.C20	A18	P1.D20	+3.3V	P1.Z20	GND
P1.A21	IACKIN*	P1.B21	N/C	P1.C21	A17	P1.D21	N/C	P1.Z21	N/C
P1.A22	IACKOUT	P1.B22	N/C	P1.C22	A16	P1.D22	+3.3V	P1.Z22	GND
P1.A23	AM4	P1.B23	GND	P1.C23	A15	P1.D23	N/C	P1.Z23	N/C
P1.A24	A07	P1.B24	IRQ7*	P1.C24	A14	P1.D24	+3.3V	P1.Z24	GND
P1.A25	A06	P1.B25	IRQ6*	P1.C25	A13	P1.D25	N/C	P1.Z25	N/C
P1.A26	A05	P1.B26	IRQ5*	P1.C26	A12	P1.D26	+3.3V	P1.Z26	GND
P1.A27	A04	P1.B27	IRQ4*	P1.C27	A11	P1.D27	N/C	P1.Z27	N/C
P1.A28	A03	P1.B28	IRQ3*	P1.C28	A10	P1.D28	+3.3V	P1.Z28	GND
P1.A29	A02	P1.B29	IRQ2*	P1.C29	A09	P1.D29	N/C	P1.Z29	N/C
P1.A30	A0l	P1.B30	IRQ1*	P1.C30	A08	P1.D30	+3.3V	P1.Z30	GND
P1.A31	-12V	P1.B31	N/C	P1.C31	+12V	P1.D31	N/C	P1.Z31	N/C
P1.A32	+5V	P1.B32	+5V	P1.C32	+5V	P1.D32	+5V	P1.Z32	GND

P1 Pin Assignment

ROWA	SIG	ROWB	SIG	ROWC	SIG	ROWD	SIG	ROWZ	SIG
P2.A01	B +12V	P2.B01	+5V	P2.C01	B AGND	P2.D01	C -12V	P2.Z01	C AGND
P2.A02	B +12V	P2.B02	GND	P2.C02	B AGND	P2.D02	C AGND	P2.Z02	GND
P2.A03	B -12V	P2.B03	N/C	P2.C03	B AGND	P2.D03	C AGND	P2.Z03	N/C
P2.A04	B -12V	P2.B04	A24	P2.C04	B AGND	P2.D04	B Chan 1 +	P2.Z04	GND
P2.A05	N/C	P2.B05	A25	P2.C05	B AGND	P2.D05	B Chan 2 +	P2.Z05	B Chan 1 -
P2.A06	A Chan 1 +	P2.B06	A26	P2.C06	A Chan 1 -	P2.D06	B Chan 2 -	P2.Z06	GND
P2.A07	A Chan 2 +	P2.B07	A27	P2.C07	A Chan 2 -	P2.D07	B Chan 3 -	P2.Z07	B Chan 3 +
P2.A08	A Chan 3 +	P2.B08	A28	P2.C08	A Chan 3 -	P2.D08	B Chan 4 +	P2.Z08	GND
P2.A09	A Chan 4 +	P2.B09	A29	P2.C09	A Chan 4 -	P2.D09	B Chan 5 +	P2.Z09	B Chan 4 -
P2.A10	A Chan 5 +	P2.B10	A30	P2.C10	A Chan 5 -	P2.D10	B Chan 5 -	P2.Z10	GND
P2.A11	A Chan 6 +	P2.B11	A31	P2.C11	A Chan 6 -	P2.D11	B Chan 6 -	P2.Z11	B Chan 6 +
P2.A12	A Chan 7 +	P2.B12	GND	P2.C12	A Chan 7 -	P2.D12	B Chan 7 +	P2.Z12	GND
P2.A13	A Chan 8 +	P2.B13	+5V	P2.C13	A Chan 8 -	P2.D13	B Chan 8 +	P2.Z13	B Chan 7 -
P2.A14	A Chan 9 +	P2.B14	N/C	P2.C14	A Chan 9 -	P2.D14	B Chan 8 -	P2.Z14	GND
P2.A15	A Chan 10 +	P2.B15	N/C	P2.C15	A Chan 10 -	P2.D15	B Chan 9 -	P2.Z15	B Chan 9 +
P2.A16	A Chan 11 +	P2.B16	N/C	P2.C16	A Chan 11 -	P2.D16	B Chan 10 +	P2.Z16	GND
P2.A17	A Chan 12 +	P2.B17	N/C	P2.C17	A Chan 12 -	P2.D17	B Chan 11 +	P2.Z17	B Chan 10 -
P2.A18	A Chan 13 +	P2.B18	N/C	P2.C18	A Chan 13 -	P2.D18	B Chan 11 -	P2.Z18	GND
P2.A19	A Chan 14 +	P2.B19	N/C	P2.C19	A Chan 14 -	P2.D19	B Chan 12 -	P2.Z19	B Chan 12+
P2.A20	A Chan 15 +	P2.B20	N/C	P2.C20	A Chan 15 -	P2.D20	B Chan 13 +	P2.Z20	GND
P2.A21	A Chan 16 +	P2.B21	N/C	P2.C21	A Chan 16 -	P2.D21	B Chan 14 +	P2.Z21	B Chan 13 -
P2.A22	N/C	P2.B22	GND	P2.C22	N/C	P2.D22	B Chan 14 -	P2.Z22	GND
P2.A23	A X Trigger	P2.B23	N/C	P2.C23	A /XTrigger	P2.D23	B Chan 15 -	P2.Z23	B Chan 15+
P2.A24	N/C	P2.B24	N/C	P2.C24	N/C	P2.D24	B Chan 16 +	P2.Z24	GND
P2.A25	A XCLK	P2.B25	N/C	P2.C25	A /XCLK	P2.D25	N/C	P2.Z25	B Chan 16 -
P2.A26	A +12V	P2.B26	N/C	P2.C26	A AGND	P2.D26	N/C	P2.Z26	GND
P2.A27	A +12V	P2.B27	N/C	P2.C27	A AGND	P2.D27	B /XTrigger	P2.Z27	B X Trigger
P2.A28	A -12V	P2.B28	N/C	P2.C28	A AGND	P2.D28	N/C	P2.Z28	GND
P2.A29	A -12V	P2.B29	N/C	P2.C29	A AGND	P2.D29	B XCLK	P2.Z29	N/C
P2.A30	N/C	P2.B30	N/C	P2.C30	A AGND	P2.D30	B /XCLK	P2.Z30	GND
P2.A31	Out+3.3V	P2.B31	GND	P2.C31	Out+3.3V	P2.D31	GND	P2.Z31	Out +3.3V
P2.A32	Out +5V	P2.B32	+5V	P2.C32	Out +5V	P2.D32	PC +5V	P2.Z32	GND

P2 pin assignment

	Denotes pins with thickened tracks which can be used for power inputs