NEWWOOD SOLUTIONS Ltd
Derby Office: 15 Kings Croft, Allestree, Derby, DE22 2FP.
Tel +44 (0)1332 721326

Reading Office: 13 Highfield Road, Tilehurst, Reading RG31 6YR.
Tel +44 (0) 118 9012298

Email: sales@newwoodsolutions.co.uk Web: www.newwoodsolutions.co.uk

PCG8523
Programmable Clock Generator
INDUSTRY PACK
(IP IO module)

USERS MANUAL

PPG8523 PCB Issue 1.0
Firmware Version 8523V101

Document Nos.: 8523/UTM/G/x/1.1
Date: 04/10/2018
Author: MRN

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/10/15	1.0	Use manual issue
05/10/18	1.1	Change from Hytec to Newwood Solutions for contact details

CRITICAL APPLICATIONS DISCLAIMER

THIS PRODUCT FROM NEWWOOD SOLUTIONS LTD USES COMPONENTS THAT ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS IN LIFE-SUPPORT OR SAFETY DEVICES OR SYSTEMS, CLASS III MEDICAL DEVICES, NUCLEAR FACILITIES, APPLICATIONS RELATED TO THE DEPLOYMENT OF AIRBAGS, OR ANY OTHER APPLICATIONS THAT COULD LEAD TO DEATH, PERSONAL INJURY OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE (INDIVIDUALLY AND COLLECTIVELY, “CRITICAL APPLICATIONS”).

FURTHERMORE, SOME COMPONENTS USED IN THIS NEWWOOD SOLUTIONS LTD PRODUCTS ARE NOT DESIGNED OR INTENDED FOR USE IN ANY APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE OR AIRCRAFT, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR.

THE CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF NEWWOOD SOLUTIONS LTD PRODUCT IN CRITICAL APPLICATIONS.

CONTENTS

1. INTRODUCTION

The PCG8523 is a single-width Industry Pack with the following characteristics:-
This clock generator allows the user to select the frequency of a clock signal which is connected to one of the I/O lines of the IP card.
The first five bits in the clock frequency select register are used to select the clock frequencies of 1 Hz to 1MHz in multiples of 1, 2, 5 or 10. (E.g. 0=1Hz, 1=2Hz, 2=5Hz, 3=10Hz and so on to 15=100KHz, 16=200KHz, 17=500KHz, 18=1MHz).

2. Product Specifications

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Data format:	Binary
Clock rates:	From 1MHz to 1Hz in in set steps
Input levels:	TTL/LTTL compatible with jumper selectable 470Ω resistor pull-up to 5V or 3.3V or pull-down with positive edge clocking
Internal clock:	50MHz
Clock accuracy:	+/-50ppm (0.005%)
Power:	+5V @ 250mA typical

3. Application Registers

3.1 Control & Status Register (CSR I/O Address 0)

Write register

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
x	x	x	x	x	x	x	x	x	STrig	ARM	En Gate	En ExTrig H	En ExTrig L	En FP Strob	RST

Read register

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
x	x	x	x	x	x	x	x	EnScan	0	ARM	En Gate	En ExTrig High	En ExTrig Low	En FP Strob	0

RST Reset - writing a 1 to this bit resets all bits in CSR registers to zero.
EnFPStrob Enables 8002/8004 Strobe Lemo input LOW going to start clock.
EnExTrig L Enables External trigger LOW going to start clock
EnExTrig H Enables External trigger HIGH going to start clock
EnGate Enables any of the hardware triggers to act as a gate i.e. as long as the trigger is asserted the clock will be generated.
ARM Arm then wait for Hardware Trigger, Strobe line or STrig to Start clock running. If ARM is removed then clock output is Stopped.
STrig Software start trigger write only. Note EnGate must be
EnScan Read only. This bit indicates that the Scan clock is running.

The front panel lemo on the 8002/8004 is connected to the STROBE line of the all the IP cards. This line can be used to start the clock if the bit **EnFPStrob=1** in the CSR.

Depending on how the jumper J1 is set (see section 5) determines how **EnExTrig L** and **EnExTrig H** are set if the external trigger is used.
With J1 set to pull up the External trigger line then setting **EnExTrig L = 1** will allow a low going signal on External trigger to start the clock.
With J1 set to pull down the External trigger line then setting **EnExTrig H = 1** will allow a high going signal on External trigger to start the clock.

3.2 Register (I/O address 2) Not used

Read/write register.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

3.3 Clock Frequency Select (I/O address 4)

Read/write register.

The first five bits in the clock frequency select register are used to select the clock frequencies of 1 Hz to 1MHz in multiples of 1, 2, 5 or 10. (E.g. 0=1Hz, 1=2Hz, 2=5Hz, 3=10Hz and so on to 15=100KHz, 16=200KHz , 17=500KHz, 18=1MHz).

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	S4	S3	S2	S1	S0

Clock rate Reg (S4 to S0)	Frequency Hz	Clock rate Reg (S4 to S0)	Frequency Hz
00000	1	01010	2KHz
00001	2	01011	5KHz
00010	5	01100	10KHz
00011	10	01101	20KHz
00100	20	01110	50KHz
00101	50	01111	100KHz
00110	100	10000	200KHz
00111	200	10001	500KHz
01000	500	10010	1MHz
01001	1KHz		

4. ID PROM

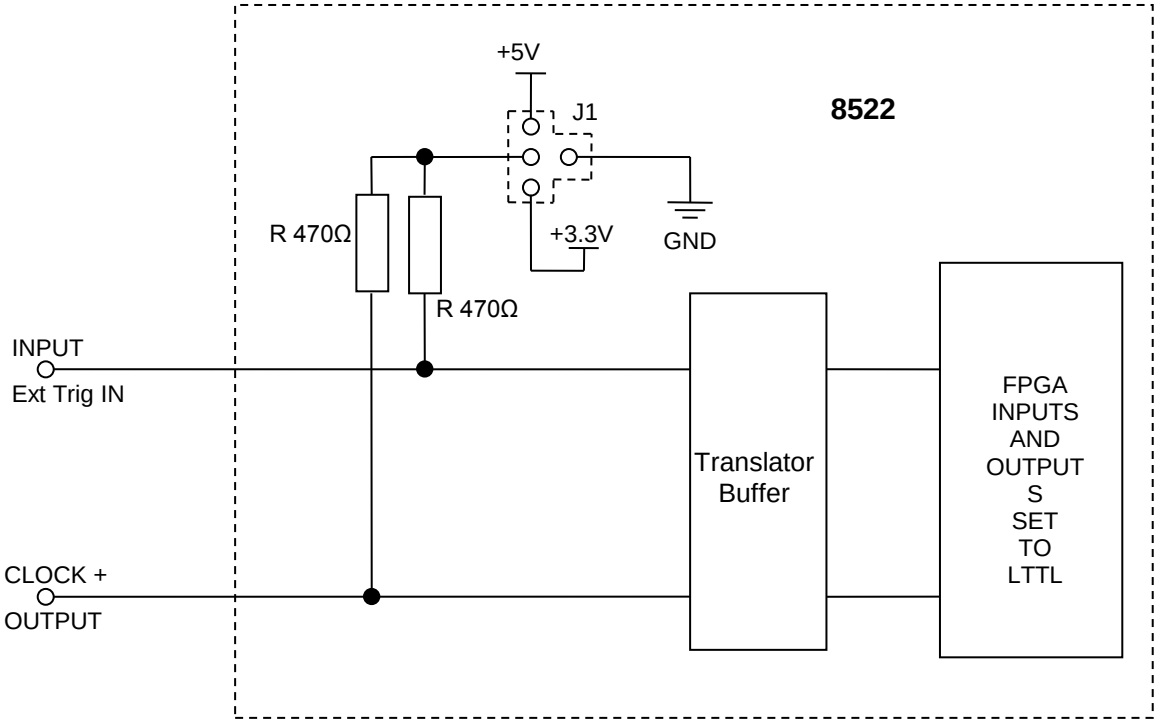
The 8523 IP module includes a configuration ID PROM. The ID information held in the PROM is as detailed below.

The byte addresses of the ID PROM are as below:-

Base+80	ASCII 'VI'	5649h	
Base+82	ASCII 'TA'	5441h	
Base+84	ASCII '4 '	3420h	
Base+86	Murf ID high byte	0080h	
Base+88	Murf ID low word	0300h	
Base+8A	Model number	8523h	
Base+8C	Revision	1101h	This shows PCB Issue 1 and Xilinx V101 means FPGA at issue 1 for PCB issue 1.
Base+8E	Reserved	0000h	
Base+90	Driver ID	0000h	
Base+92	Driver ID	0000h	
Base+94	Flags	0002h	
Base+96	No of bytes used	001Ah	
Base+98	Not used	xxxxh	
Base+9A	Serial Number	xxxxdec	

5. J1 Pull-up or Pull-down For TTL Logic Signals

The jumper J1 allows the user to pull-up to 3.3V or 5V or pull-down to ground.



APPENDIX A

Programmable clock generator IP Board Pinouts.

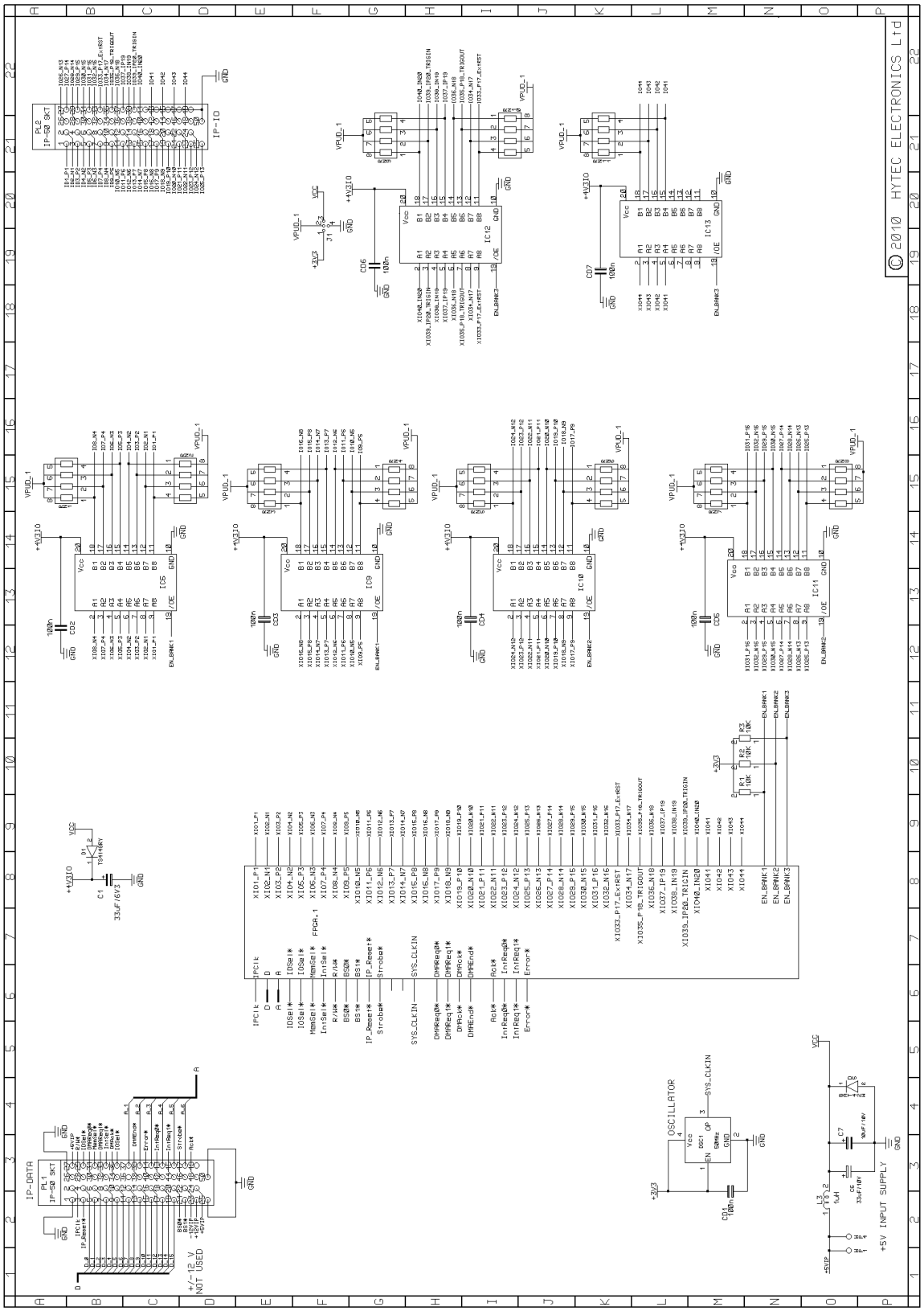
Pin Trans	Pin 8522	Signal	Pin Trans	Pin 8522	Signal
1	*2*		26	*1*	
2	*4*		27	*3*	
3	*6*		28	*5*	
4	*8*		29	*7*	
5	*10*		30	*9*	
6	*12*		31	*11*	
7	*14*		32	*13*	
8	*16*		33	*15*	
9	*18*		34	*17*	
10	*20*		35	*19*	
11	*22*		36	*21*	
12	*24*		37	*23*	
13	*26*		38	*25*	
14	*28*		39	*27*	
15	*30*		40	*29*	
16	*32*		41	*31*	
17	*34*		42	*33*	
18	*36*		43	*35*	ExtTrig +
19	*38*		44	*37*	
20	*40*		45	*39*	CLOCK +
21	*42*		46	*41*	GND
22	*44*		47	*43*	GND
23	*46*		48	*45*	GND
24	*48*		49	*47*	GND
25	*50*	GND	50	*49*	GND

APPENDIX B

HYTEC 8901 Terminal Block Pinouts.

Pin	Signal	Pin	Signal
1		26	
2		27	
3		28	
4		29	
5		30	
6		31	
7		32	
8		33	
9		34	
10		35	
11		36	
12		37	
13		38	
14		39	
15		40	
16		41	
17		42	
18		43	ExtTrig +
19		44	
20		45	CLOCK +
21	AGND	46	
22	AGND	47	
23	AGND	48	
24	AGND	49	
25	AGND	50	AGND

APPENDIX C


© 2010 HYTEC ELECTRONICS Ltd
IP-DATA
IP-10
OSCILLATOR
+5V INPUT SUPPLY
NOT USED