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IP-DIO-8600
User Configurable 48-bit Digital I/O Board
INDUSTRY PACK

USERS MANUAL

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Revision History

The following table shows the revision history for this document.

Date	Version	Change Notes
04/03/2019	1.0	Issued
04/04/2023	1.1	Change tables of pinouts to be more easily read

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1. INTRODUCTION

This is a single-width IP module with user configurable FPGA in the form of a Xilinx Spartan 3 FPGA XC3S200AN-5 with 200,000 system gates, and forty eight channels of user buffered digital input/output.
The 48 digital I/O lines are in 6 groups of 8 bits and can be set as inputs or outputs via the FPGA logic. The I/O lines are fitted with a resistor network which allows a selectable pull up/down voltage of GND, +3.3V or 5V. The unit also has an on-board 50MHz clock oscillator.
The Xilinx FPGA can be configured using free software which can be down loaded from the Xilinx Website
The FPGA logic is configurable via JTAG plug on the IP card.
The I/O buffer devices are bidirectional level translators which have a 24mA drive rating and allow the inputs or outputs to be +5V tolerant.
The optional memory is 16M-bit static RAM organized as 1024K words by 16 bits with a 10ns High-speed access time.
There are also three user selectable jumpers which gives the user the ability for further control of the FPGA firmware by allowing input lines to the FPGA to be pulled low.

2. PRODUCT SPECIFICATIONS

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of input/outputs:	48 (configurable as 3 groups of 16 in or 16 out)
Input level:	TTL
Output level:	TTL 24mA, programmable logic sense high or low true
Input/output termination:	4k7 ohms to 0V, or +3.3V or 5V by jumpered selection
Internal clock:	50MHz oscillator.
Clock accuracy:	+/-100ppm (0.01%)
Power:	+5V @ 250mA typical

3. FPGA Development Tools and Files

The Xilinx FPGA used on the 8600 can be configured using free software which can be down loaded from the Xilinx Website:
https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/design-tools/v2012_4---14_7.html.

3.1 FPGA Pin Outs Constrains File

A User Constrains file detailing the FPGA pin outs is provided with the unit.

3.2 Programming Cable for Xilinx® FPGAs

A low cost solution is the Digilent JTAG HS2 Programmer.
The joint test action group (JTAG) HS2 programming cable is a high-speed programming solution for Xilinx® field-programmable gate arrays (FPGAs). The cable is fully compatible will all Xilinx tools and can be seamlessly driven from iMPACT™, ChipScope™, and EDK. The HS2 attaches to target boards using Digilent's 6-pin, 100-mil spaced programming header or Xilinx's 2x7, 2mm connector and the included adaptor.

3.3 Xilinx XC3S200AN-5 Data Sheet and Design Guides

Data sheets and design guides can be down loaded from the Xilinx website.
Example:
XC3S200AN-5 Data sheet: https://www.xilinx.com/support/documentation/data_sheets/ds557.pdf

4. Industry Pack Standard

The IP Module is a versatile electronic module that provides a convenient level of modularity for implementing a wide range of I/O, control, interface, analogue and digital functions.
Two connectors are used on each IP Module. One is dedicated to control of the IP Module, and is fully specified. The other connector is provided for the IP Module's specific function. Its interface is called the I/O Interface. All 50 signals in the I/O Interface are defined by each IP Module.
The IP standard is defined in the ANSI/VITA 4-1995 (R2002) standard.

5. Jumpers

J1 controls selection of I/O termination voltage for banks 4, 5 and 6

2-4	Terminate data I/O lines to GND
2-1	Terminate data I/O lines to 3.3V
2-3	Terminate data I/O lines to 5V

J6 controls selection of I/O termination voltage for banks 1, 2 and 3

2-4	Terminate data I/O lines to Gnd
2-1	Terminate data I/O lines to 3.3V
2-3	Terminate data I/O lines to 5V

J2, **J3**, **J4** and **J5** User defined in design. When jumper fitted line pulled to GND

User defined Jumpers in design. With jumper fitted line is connected to GND
J2 connected to FPGA pin L14
J3 connected to FPGA pin K14
J4 connected to FPGA pin K13
J5 connected to FPGA pin G13
IMPORTANT NOTE if J2, J3, J4 or J5 are fitted the relevant FPGA pin must be set as an input.

6. Contact Information

For further information on designing with this product contact:
hardware_enquiries@newwoodsolutions.co.uk

7. IP8600 Board I/O Pin Assignments 50-way SCSI-2 connectors

TB8304 is a VME rear transition card with 4 x 50-way SCSI-2 connectors each which can be connected to an 8901 terminal board via 50-way SCSI-2 cable.

DIO8600 Signal	DIO8600 Buffer IC PCB IDENT	DIO8600 FPGA Pinning	DIO8600 50-way SCSI-2 Pinning		VTB8304 50-way SCSI-2 Pinning	VDB8901 Terminal Board	Notes
Set I/O direction Bank 1 FPGA Pin = K15 J6 controls selection of I/O termination voltage							
I/O	12	C8	2		1	1	
I/O	12	D8	4		2	2	
I/O	12	C10	6		3	3	
I/O	12	D9	8		4	4	
I/O	12	K16	10		5	5	
I/O	12	J16	12		6	6	
I/O	12	J14	14		7	7	
I/O	12	H14	16		8	8	
Set I/O direction Bank 2 FPGA Pin = G14 J6 controls selection of I/O termination voltage							
I/O	11	F8	18		9	9	
I/O	11	E7	20		10	10	
I/O	11	C6	22		11	11	
I/O	11	D7	24		12	12	
I/O	11	E10	26		13	13	
I/O	11	D10	28		14	14	
I/O	11	D11	30		15	15	
I/O	11	C12	32		16	16	
Set I/O direction Bank 3 FPGA Pin = G16 J6 controls selection of I/O termination voltage							
I/O	13	F16	34		17	17	
I/O	13	F14	36		18	18	
I/O	13	C15	38		19	19	
I/O	13	B8	40		20	20	
I/O	13	H16	42		21	21	
I/O	13	H15	44		22	22	
I/O	13	F15	46		23	23	
I/O	13	E16	48		24	24	
Set I/O direction Bank 4 FPGA Pin = L16 J1 controls selection of I/O termination voltage							
I/O	6	D13	1		26	26	
I/O	6	C13	3		27	27	
I/O	6	B15	5		28	28	
I/O	6	B14	7		29	29	
I/O	6	A14	9		30	30	
I/O	6	A13	11		31	31	
I/O	6	B12	13		32	32	
I/O	6	A12	15		33	33	
Set I/O direction Bank 5 FPGA Pin = D16 J1 controls selection of I/O termination voltage							
I/O	10	A6	17		34	34	
I/O	10	B6	19		35	35	
I/O	10	A5	21		36	36	
I/O	10	C5	23		37	37	
I/O	10	A4	25		38	38	
I/O	10	B4	27		39	39	
I/O	10	A3	29		40	40	
I/O	10	B3	31		41	41	
Set I/O direction Bank 6 FPGA Pin = H13 J1 controls selection of I/O termination voltage							
I/O	9	C11	33		42	42	
I/O	9	A11	35		43	43	
I/O	9	B10	37		44	44	
I/O	9	A10	39		45	45	
I/O	9	C9	41		46	46	
I/O	9	A9	43		47	47	
I/O	9	A7	45		48	48	
I/O	9	C7	47		49	49	
GND	-	-	49		25	25	
GND	-	-	50		50	50	

8. DIO8600 Configuration to be Used as an 8606/8506 Card I/O Pin

DIO8600 Signal	DIO8600 Buffer IC PCB IDENT	DIO8600 FPGA Pinning	DIO8600 50-way SCSI-2 Pinning		TB8304 50-way SCSI-2 Pinning	VDB8901 Terminal Board	Notes
I/O	6	D13	1		26	26	
I/O	12	C8	2		1	1	
I/O	6	C13	3		27	27	
I/O	12	D8	4		2	2	
I/O	6	B15	5		28	28	
I/O	12	C10	6		3	3	
I/O	6	B14	7		29	29	
I/O	12	D9	8		4	4	
I/O	6	A14	9		30	30	
I/O	12	K16	10		5	5	
I/O	6	A13	11		31	31	
I/O	12	J16	12		6	6	
I/O	6	B12	13		32	32	
I/O	12	J14	14		7	7	
I/O	6	A12	15		33	33	
I/O	12	H14	16		8	8	
I/O	10	A6	17		34	34	
I/O	11	F8	18		9	9	
I/O	10	B6	19		35	35	
I/O	11	E7	20		10	10	
I/O	10	A5	21		36	36	
I/O	11	C6	22		11	11	
I/O	10	C5	23		37	37	
I/O	11	D7	24		12	12	
I/O	10	A4	25		38	38	
I/O	11	E10	26		13	13	
I/O	10	B4	27		39	39	
I/O	11	D10	28		14	14	
I/O	10	A3	29		40	40	
I/O	11	D11	30		15	15	
I/O	10	B3	31		41	41	
I/O	11	C12	32		16	16	
I/O	9	C11	33		42	42	
I/O	13	F16	34		17	17	
I/O	9	A11	35		43	43	
I/O	13	F14	36		18	18	
I/O	9	B10	37		44	44	
I/O	13	C15	38		19	19	
I/O	9	A10	39		45	45	
I/O	13	B8	40		20	20	
I/O	9	C9	41		46	46	
I/O	13	H16	42		21	21	
I/O	9	A9	43		47	47	
I/O	13	H15	44		22	22	
I/O	9	A7	45		48	48	
I/O	13	F15	46		23	23	
I/O	9	C7	47		49	49	
I/O	13	E16	48		24	24	
GND	-		49		50	50	
GND	-		50		25	25	