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IP-SM-8602/1
Stepper Motor Controller
INDUSTRY PACK

Product Specification

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Revision History

The following table shows the revision history for this document.

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12/02/2019	1.0	Issued
01/11/2021	1.1	Base+8A Model number 8602h Amend to Base+8A Model number 8601h with J2 OUT

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1. INTRODUCTION

The Newwood Solutions IP-SM-8602/1 is a single-width Industry Pack stepper motor controller producing four channels of logic level control signals for an external driver system. To see what Newwood Solutions offers for these systems refer to:-

For small (<1amp) motors, the 8909U low cost L/R driver.
For larger (up to 6amps bipolar drive) motors, the MDS8.

An EPICs driver is available for this card. All registers exist within the Industry Pack I/O, ID and Interrupt areas; no memory is present.

Each channel has the following features:-

- A 32-bit step register, which sets the number of steps in the next movement, writeable and readable at any time, which counts down to '0'.
- A 32-bit absolute position up/down counter, which records movements (writeable and readable). This counter counts all movements including JOG. This counter may follow step pulses sent out from the board or count encoder pulses from an external incremental encoder with quadrature outputs.
- A 16-bit Start/Stop Speed Register, which sets the speed at which a movement will start, programmed in steps per second.
- A 16-bit High Speed Register, which sets the speed at which the motor will run after accelerating, programmed in steps per second.
- A 16-bit Ramp Rate Register, which sets the rate at which speed will increase or decrease during ramping, programmed in steps per second per second. Minimum value 64 s/s/s.
- A 16-bit Control and Status Register through which the status of the drive, the controller and the limit switches can be observed (run/stop, hit limit, driver dead etc.).
- A 16-bit Interrupt Mask Register through which controls which CSR bits may generate interrupt.
- Counters can be read on the fly via a shadow register.
- A ‘Common Start’ register through which one or more channels can be started simultaneously, visible within each channel’s register area (write only).
- Each channel has four logic outputs and 8 logic inputs to cater for a wide variety of applications.
- The ability to read the module identity, manufacturer, model, revisions and serial number from an onboard ID ROM.

2. PRODUCT SPECIFICATIONS

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of channels:	4 motors
Max. count:	32 bits.
Data format:	Binary
Max step rate:	62.5KHz
Input levels:	TTL compatible with jumper selectable 4.7kΩ resistor pull-up or pull-down.
Power:	+5V @ 180mA typical

3. Application Registers

Each of the four channels has a set of ten application specific (I/O) registers plus an additional Common Start register, laid out as follows:

3.1 Step Counter (Low) Register (Channel base + 00h)

This readable and writeable register sets the low 16 bits of the desired step count for a 'GO' movement. The actual count of the full 32-bit counter is latched on the read of the high word (see below).

3.2 Step Counter (High) Register (Channel base + 02h)

This readable and writeable register sets the upper16 bits of the desired step count for a 'GO' movement. The actual count of the full 32-bit counter is latched on the read of the high word, so this register should always be read first.

3.3 Absolute Position Counter (Low) Register (Channel base + 04h)

This is the low 16 bits of a 32-bit up/down counter which follows all motor movements. It counts either step pulses being output or encoder pulses received depending on the 'Use Encoder' bit in the CSR (see below). When counting step pulses, it counts UP when the direction bit is '1'.

3.4 Absolute Position Counter (High) Register (Channel base + 06h)

This is the upper 16 bits of a 32-bit up/down counter which follows all motor movements. It counts either step pulses being output or encoder pulses received depending on the 'Use Encoder' bit in the CSR (see below). When counting step pulses, it counts UP when the direction bit is '1'. The contents of this 32-bit counter are latched on reading the high word, so this register should always be read first.

Note that due to the quadrature decoding method used, four counts are derived from each cycle of the encoder pulses, effectively quadrupling the resolution of the encoder. In other words, a 500 step-per-revolution encoder will result in 2000 counts per rotation.

3.5 Start/Stop Speed Register (Channel base + 08h)

This 16-bit register is programmed in steps per second and sets the speed at which all movements will start and end.

3.6 High Speed Register (Channel base + 0Ah)

This 16-bit register is programmed in steps per second and sets the speed at which all movements will take place after the ramp up has completed.
2000 steps/sec on 200 steps/rev motor is 10 rev/second (600 rpm) for example.

3.7 Ramp Rate Register (Channel base + 0Ch)

This 16-bit register is programmed in steps per second per second and sets the rate at which the motor speed will increase or decrease during ramping. It is programmed in steps per second per second and the minimum allowed value is 64. The granularity of the programmed value is also 64, so the available rates are 64, 128, 192 and so on up to 1024, at which time the granularity becomes 256. The maximum allowed value for this register is 50,000 decimal.

3.8 Control and Status Register (Channel base + 0Eh)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
SH	IEN	DN	AB	DIR	OP2	OP1	UE	ED	JOG	GO	FLT	HLIM	+LIM	-LIM	RST

Bit Function
0 RESET – Write '1' clears all bits of all registers.
1 Negative Limit – '1' means the limit switch is open. (Read only).
2 Positive Limit – '1' means the limit switch is open. (Read only).
3 Home Limit – '1' means the limit switch is open. (Read only).
4 Drive Fault – '1' means that the fault input is not energised. (Read only).
5 GO – write '1' to start a movement of the number of steps programmed. Write '0' to soft stop.
6 JOG – write '1' to start a free-running movement. Write '0' to slow down and stop.
7 ED – Encoder Detected – a '1' in this bit indicates that valid clock pulses were detected. (RO)
8 UE – Use Encoder – this means that the absolute position register should count encoder pulses.
9 OP1 controls a spare output (AUX1) on the interface.
10 OP2 controls a spare output (AUX2) on the interface.
11 Direction – '1' is positive, towards the positive limit switch.
12 ABORT – write '1' to stop immediately.
13 DONE – set as '1' by the completion of a movement. Write a one to clear.
14 Interrupt Enable – '1' = enable.
15 Stop at Home. '1' means stop if the Home Limit is encountered.

Limit switches
If motor hits limit switch then motor is stopped. Cannot move motor until direction bit DIR changed to move motor away from limit switch.
The position reg will not be cleared

JOG
When JOG is set it will start the motor turning until it is cleared. If the ramp register is used then will ramping up and counting the number of ramps it took to get to HIGH Speed. This number is held in the 32 bit Step Count register which is first cleared when JOG set. When JOG is cleared the number of counts it took to ramp up held in the Step Count Register is used to ramp the motor down.

3.9 Interrupt Mask Register (Channel base + 10h)

This 16-bit register contains bits corresponding to CSR bits which may be a source of interrupt. The logical AND of bits in this register and those in the CSR will cause the channel and then the IP module to generate an interrupt on IRQ0, provided that the interrupt enable bit has been set in the CSR. Bit 15 of this register has a special function which is that if it is set to '1', then any limit switch opening will cause an immediate stop, independent of direction.

3.10 Interrupt Vector Register (Channel base + 12h)

This 16-bit register is programmed with the 16-bit interrupt vector this channel will respond with when receiving an interrupt acknowledge cycle. An interrupt acknowledge issued by the carrier board to this IP module will automatically be routed to the highest numerical channel currently requesting service.

3.11 Current Speed Register (Channel base + 16h)

This 16-bit register is programmed with the 16-bit interrupt vector this channel will respond with when receiving an interrupt acknowledge cycle. An interrupt acknowledge issued by the carrier board to this IP module will automatically be routed to the highest numerical channel currently requesting service.

3.12 Common Start Register (Channel base + 18h)

This 4-bit register is accessible through the register set of any channel at offset 18h and is write only. Each of bits 0 to 3 corresponds to channel 0 to 3 respectively and writing a '1' to a bit implies that this channel should start immediately, provided that all conditions are met for that to happen (that is no limits set and so on).

4. Channel Addressing

The IO area of the 8602 is split up as follows:

Offset	Contents
00h – 1Eh	Channel 0 registers.
20h – 3Eh	Channel 1 registers.
40h – 5Eh	Channel 2 registers.
60h – 7Eh	Channel 3 registers.

5. ID PROM

The 8602/1 IP module includes a configuration ID PROM. The ID information held in the PROM is as detailed below.

The byte addresses of the ID PROM 8602 **(J2 IN)** are as below: -

Base+80	ASCII 'VI'	5649h
Base+82	ASCII 'TA'	5441h
Base+84	ASCII '4 '	3420h
Base+86	NWS ID high byte	0080h
Base+88	NWS ID low word	0300h
Base+8A	Model number	8602h
Base+8C	Revision	1101h (This shows PCB Issue 1 and FPGA at issue 1)
Base+8E	Reserved	0000h
Base+90	Driver ID	0000h
Base+92	Driver ID	0000h
Base+94	Flags	0002h
Base+96	No of bytes used	001Ah
Base+98	Not used	0000h
Base+9A	Serial Number	xxxxdec

The byte addresses of the ID PROM 8601 **(J2 OUT)** are as below: -

Base+80	ASCII 'VI'	5649h
Base+82	ASCII 'TA'	5441h
Base+84	ASCII '4 '	3420h
Base+86	NWS ID high byte	0080h
Base+88	NWS ID low word	0300h
Base+8A	Model number	8601h
Base+8C	Revision	3301h (This shows PCB Issue 3 and FPGA at issue 1)
Base+8E	Reserved	0000h
Base+90	Driver ID	0000h
Base+92	Driver ID	0000h
Base+94	Flags	0002h
Base+96	No of bytes used	001Ah
Base+98	Not used	0000h
Base+9A	Serial Number	xxxxdec

The PCB issue and FPGA issues for the 8601 ID ROM issue are in line with the original Hytec 8601 boards.

APPENDIX A

PCB JUMPERS

Jumpers J1 and J6

Terminate external interface signals to GND, 5 volts or 3.3 Volts.
Terminate to GND = jumper pins 2 & 4;
Terminate to 3.3 Volts = jumper pins 2 & 1.
Terminate to 5 Volts = jumper pins 2 & 3 (default).

Note: jumper J1 and J6 **MUST** be fitted in the 2-3 default position when this unit is used with open-collector sources, such as Newwood Solutions motor drive systems 8909U and SMDS4.

Jumpers J2

J2 OUT Unit seen as 8601
J2 IN Unit seen as 8602

Jumpers J3 to J5

These jumpers are not in this design.

APPENDIX B

I/O Connector – 50 way I/O Connector on 8602 IP Board

Pin	8602 IP	Trans Pin		Pin	8602 IP	Trans
1	Ch 1 Phase A	26		26	Ch4 Step output	13
2	Ch1 Step output	1		27	Ch 4 Phase B	39
3	Ch 1 Phase B	27		28	Ch4 Dir output	14
4	Ch1 Dir output	2		29	Ch 4 Index	40
5	CH 1 Index	28		30	Ch4 OP1 output	15
6	Ch1 OP1 output	3		31	Reserved I/P16	41
7	Reserved I/P4	29		32	Ch4 OP2 output	16
8	Ch1 OP2 output	4		33	GND	42
9	Ch 2 Phase A	30		34	Ch1 +LIM I/P	17
10	Ch2 Step output	5		35	Ch1 -LIM I/P	43
11	Ch 2 Phase B	31		36	Ch1 HOME LIM I/P	18
12	Ch2 Dir output	6		37	Ch1 FAULT I/P	44
13	Ch 2 Index	32		38	Ch2 +LIM I/P	19
14	Ch2 OP1 output	7		39	Ch2 -LIM I/P	45
15	Reserved I/P8	33		40	Ch2 HOME LIM I/P	20
16	Ch2 OP2 output	8		41	Ch2 FAULT I/P	46
17	Ch 3 Phase A	34		42	Ch3 +LIM I/P	21
18	Ch3 Step output	9		43	Ch3 -LIM I/P	47
19	Ch 3 Phase B	35		44	Ch3 HOME LIM I/P	22
20	Ch3 Dir output	10		45	Ch3 FAULT I/P	48
21	Ch 3 Index	36		46	Ch4 +LIM I/P	23
22	Ch3 OP1 output	11		47	Ch4 -LIM I/P	49
23	Reserved I/P12	37		48	Ch4 HOME LIM I/P	24
24	Ch3 OP2 output	12		49	Ch4 FAULT I/P	50
25	Ch 4 Phase A	38		50	GND	25

APPENDIX C

NEWWOOD SOLUTIONS TRANSITION CARD CONNECTIONS

I/O Connector – SCSI-2 50 way on transition Card 8304 where this feeds ONE IP site:

Pin	Signal		Pin	Signal
1	Ch1 Step output		26	Ch 1 Phase A
2	Ch1 Direction output		27	Ch 1 Phase B
3	Ch1 OP1 output		28	Ch 1 Index
4	Ch1 OP2 output		29	Reserved IP4
5	Ch2 Step output		30	Ch 2 Phase A
6	Ch2 Direction output		31	Ch 2 Phase B
7	Ch2 OP1 output		32	Ch 2 Index
8	Ch2 OP2 output		33	Reserved IP8
9	Ch3 Step output		34	Ch 3 Phase A
10	Ch3 Direction output		35	Ch 3 Phase B
11	Ch3 OP1 output		36	Ch 3 Index
12	Ch3 OP2 output		37	Reserved IP12
13	Ch4 Step output		38	Ch 4 Phase A
14	Ch4 Direction output		39	Ch 4 Phase B
15	Ch4 OP1 output		40	Ch 4 Index
16	Ch4 OP2 output		41	Reserved IP16
17	Ch1 +LIM I/P		42	GND
18	Ch1 HOME LIM I/P		43	Ch1 -LIM I/P
19	Ch2 +LIM I/P		44	Ch1 FAULT I/P
20	Ch2 HOME LIM I/P		45	Ch2 -LIM I/P
21	Ch3 +LIM I/P		46	Ch2 FAULT I/P
22	Ch3 HOME LIM I/P		47	Ch3 -LIM I/P
23	Ch4 +LIM I/P		48	Ch3 FAULT I/P
24	Ch4 HOME LIM I/P		49	Ch4 -LIM I/P
25	GND		50	Ch4 FAULT I/P