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IOC8800
A Modular
DIN-Rail Mounted IOC
2 Industry Pack Carrier

USERS MANUAL

PCB Issue 1.0
Firmware Version 8800V101 –V104

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/04/17	0.1	Initial release of draft version.
15/06/17	0.2	Error Bit Implemented
25/06/17	0.3	Added detailed information on reading Interrupt vector from IP card
10/08/17	1.0	Release of first version Update to FPGA versions

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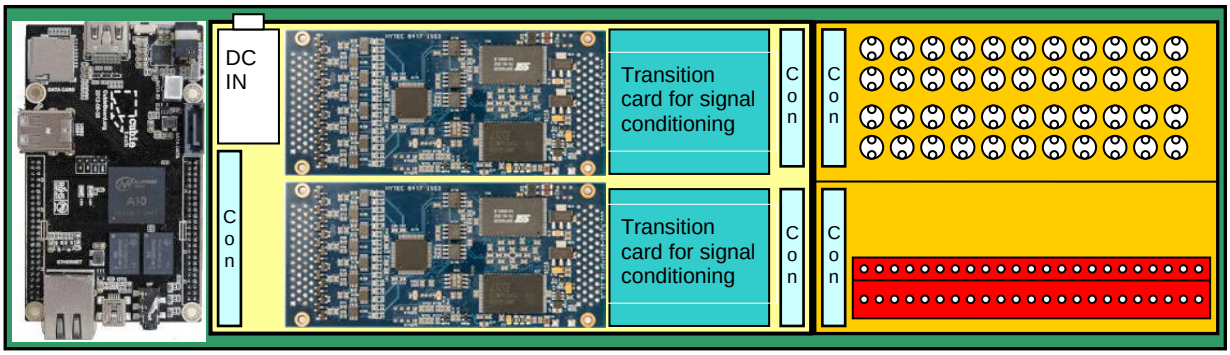
CONTENTS

1. INTRODUCTION

The IOC 8800 is a DIN-RAIL Rack Mounted Input / Output controller, designed to carry up to 2 Single width Industry Packs (IP) card simultaneously.

DIN Rail Mounted PCB Holder



Single-Board Computer. Running Linux and Epics software 10/100M Ethernet plus USB etc.

IPC8800
Two site IP carrier with interconnect logic and plug in Mini Signal Conditioning Boards. This section also has the power input circuitry which requires +/-24V DC supply.

Terminal Boards.
A number of different combinations can be used Such as two 50 way screw terminal blocks or LVDS connections.

MAIN FEATURES :

- **Cost Effective All-in-One IOC solution with flexible I/O options**
- **Compact Alternative to VME or cPCI Crate**
- **Large range of Industry Pack cards available**
- **Low cost 'BeagleBone Black' Single-Board Computer**
- **DC/DC converter slots for plant isolation**
- **Signal Conditioning Boards**
- **Mix and Match I/O**
- **Buffered digital I/O for synchronisation and control of modules**
- **Leds show when board is powered and if any of the thermal fuses have tripped**
- **Ethernet 10/100 Mbps**
- **Software downloads and support including Linux, EPICS, TANGO, Windows**

Using the wide range of Industry Packs available and the power of a small single board processor running Linux (or other operating system) the 8800 delivers a compact DIN rail mounting IOC solution.

The IOC8800 also comes complete with space for the Hytec range of signal conditioning cards (Optical isolation, analogue filtering etc) and our plug-in DC/DC converter cards for plant isolation.

Scsi 50 way high density connectors are used to allow plant connections to our range of signal termination options such as screw terminals, single ended or differential Lemo or miniature LVDS connectors.

1.1 Industry Packs

All Industry Pack card conform to an open specification which defines their key characteristics and ensuring compatibility between suppliers.
On the IOC8800 each Industry Pack has provision for a plug-in Signal Conditioning Board which allows for signal conditioning and plant isolation to be added. The 8800 uses 50-way SCSI II connector so that inexpensive, commercially available cables can be used with Hytec's range of DIN Rail Terminal Boards for connection to plant wiring.
EPICS, Linux component device drivers are available from Hytec for our range of IP cards. These drivers scans the IP slots to determine the current I/O and will auto configure the IP cards allowing the systems to be operational quickly.

1.2 Typical Processor

Low cost 'BeagleBone Black' SBC 1Ghz ARM A8 processor with 512MB DDR3ram, 2GB NAND flash, micro SD card slot, 10/100 Ethernet, 2xUSB, and 2x 200MHz PRU 32-bit microcontrollers.

1.3 FPGA Interface

The logic on the IOC8800 consists of an FPGA which interfaces the Single Board Computer card such as the Beaglebone Black (BBB) to the Industry Packs.
The IP clocks can run at 8MHz or 32MHz and can be individually set per IP card in the main FPGA using registers.
Led indicators on the board show when the IP cards are addressed by the Single Board Computer.
There are 3 buffered digital inputs (TTL, LTTL compatible) to the IOC8800 which can be used for synchronisation and control of the IP modules.

1.4 Signal Conditioning Boards

The IOC has a range of mini plug-in I/O Signal Conditioning Boards, they route all I/O signals via the PCB mounted high density 50-way SCSI-2 sockets to the industry packs. Some boards include sites with the option of fitting R-C low-pass filters which can be selected by jumpers to be in or out of circuit. Additionally, optional plug-in 5V to +/-12V DC-DC converters can be used with some boards to facilitate powering the plant side of isolated analogue circuits.

1.5 Power Supplies And Power Indicators

The unit requires 5V only to operate. The +/-12v if required can be supplied from an external power supply or from the optional plug-in 5V to +/-12V DC/DC converters.
Led lamps are used to show when the board is powered and if any of the thermal fuses have tripped.
LED1 When ON +12V fuse is open (red).
LED7 When ON -12V fuse is open (red).

LED8 When ON +5V fuse is open (red).
LED2 When ON +5V supply is connected (green).

1.6 LED Indicators

LED3 *Could indicates an error (not yet implemented or defined)*
LED4 indicates BBB addressed ioc8800
LED5 indicates Ack from IP A
LED6 indicates Ack from IP B

1.7 DIN Rail Mounted PCB Support

The compact PCB mounting profile provides a modular approach and enables the user to tailor the system to there requirements.
The width of the system is based on the 108mm compact PCB mounting for DIN Rail.

1.8 Inputs On ioc8800

1.8.1 RST-TRIG Lemo Input.

This input goes to both IP card Strobe* lines via the FPGA on the ioc8800. This input is buffered and can be driven to +5V.

1.8.2 Buffered I/O J7 and J8

These I/Os are buffers and can except +5V inputs and can supply LTTL 3.3V outputs. *Not used in current design.*

2. ON BOARD FEATURES

The configuration and control of the 8800 module is achieved by the following registers:

Base	Offset	Register	Description
Base +	0x00	Control & Status Register CB	Set up of 8800 carrier card
Base +	0x01	IP Interrupt Select and IP Status	Selects IP interrupts to be mapped to BBB Allows state of IP INT and Error flags to be monitored
Base +	0x02	Not Use	None
Base +	0x03	Not Use	None
Base +	0x04	Not Use	None

8800 On-Board Registers

To select the 8800 registers **Slot=0x00** and use address lines 1 to 6.

2.1 IOC8800 Control & Status Register

Control (Write)
Address: Base + 0x0000

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
												IP B CLK	IP A CLK	INTEN	Rst

Status (Read)
Address: Base + 0x0000

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
												IP B CLK	IP A CLK	INTEN	Rst

Rst Clears status register to zero when written as a '1'. (Not yet implemented)
INTEN Enable interrupt from 8800 to BBB.

IP A CLK Set IP A clock speed 0 = 8MHz and 1 = 32MHz.
IP B CLK Set IP B clock speed 0 = 8MHz and 1 = 32MHz.

2.2 IP's Control and Status Register

Control (Write)
Address: Base + 0x0001

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
												IPINT Enable B1	IPINT Enable A1	IPINT Enable B0	IPINT Enable A0

This selects which IP interrupt request lines will be enabled.
'1' = corresponding IP card interrupt enabled.

Status (Read)
Address: Base + 0x0001

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
IP ERR				INT REQ B1	INT REQ A1	INT REQ B0	INT REQ A0					IPINT Enable B1	IPINT Enable A1	IPINT Enable B0	IPINT Enable A0

Two interrupt status and one error status bits for each of IP sites A – B.
IP ERR Open drain signal can be driven by any IP card. The Industrial I/O Pack specification states that the error signals indicate a non-recoverable error from the IP module. See your IP documentation for a description of the error signal if used.

2.3 IOC8800 ID ROM Registers

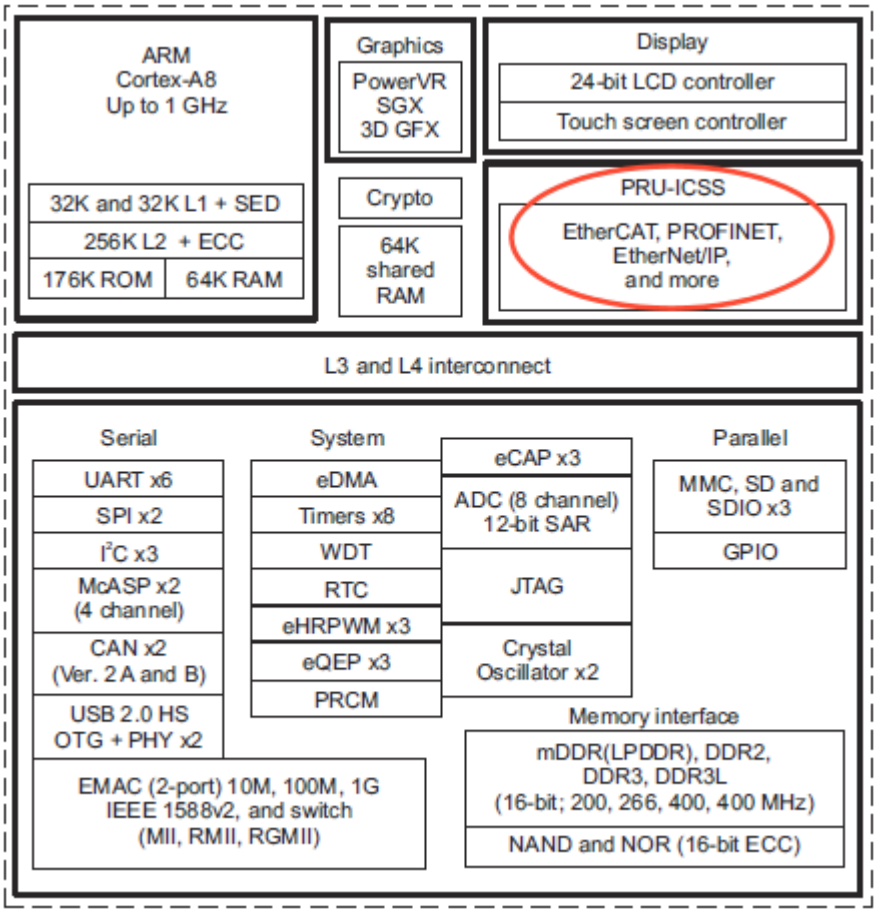
To select the 8800 ID ROM register set **Slot=0x01** and use address lines 1 to 6.

Address Offset	Value	Definition
0x0000	0x 0080	Manufacturer's ID High 8 bits
0x0001	0x 0300	Manufacturer's ID Low 16 bits

0x0002	0x8800	Model Number
0x0003	0xXXXX	Revision
0x0004	0xXXXX	Serial Number

3. BBB 8800 Interface

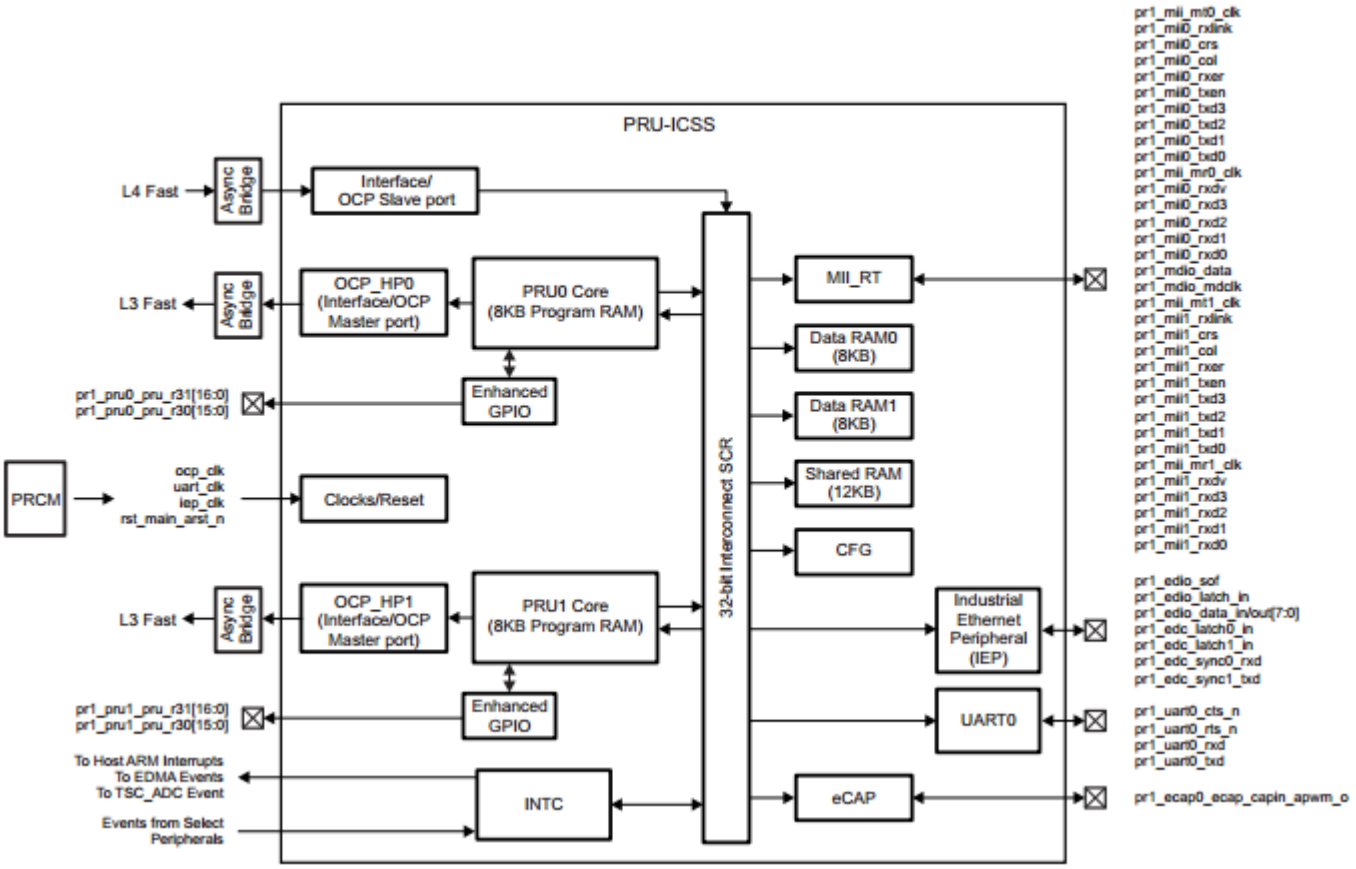
The BBB talks to the FPGA of the 8800 via its 2 **P**rogrammable **R**ealtime **U**nit **S**ub**S**ystem (PRUSSv2 or PRU for short).



The PRUSS consists of:

- Two Programmable Realtime Units (PRU0 and PRU1) and their associated memories (data RAM and instruction RAM) running at 200MHz
- An INTC (Interrupt Controller) for handling system input events. INTC also supports posting events back to the device level host CPUs (e.g. C674x DSP)

Figure 2. PRU-ICSS Integration



Getting the PRUs to Run Programs

This piece of code runs on the ARM processor and set-up and starts the two PRU programs

```
// Driver header file
#include <prussdrv.h>
#include <pruss_intc_mapping.h>

/******************************************************************************

* Explicit External Declarations                                 *

******************************************************************************/


/******************************************************************************

/*Local Macro Declarations                                       */
#define PRU_0   0
#define PRU_1   1
#define AM33XX

int main (void)
{
```

```
/* Initialize the PRU */

prussdrv_init ();

/* Open PRU Interrupt */
ret = prussdrv_open(PRU_EVTOUT_1);
if (ret)
{
    printf("prussdrv_open open failed\n");
    return (ret);
}

/* Get the interrupt initialized */
prussdrv_pruintc_init(&pruss_intc_initdata);


/* Initialize example */
LOCAL_exampleInit();


/* Execute programmes on PRU_0 and PRU_1 */
prussdrv_exec_program (PRU_0, "./ioc_pru_0.bin");
prussdrv_exec_program (PRU_1,   "./pru_1.bin");
```

The user now only has to write to one 32 bit instruction/data and one 16 bit data word depending on the operation required. The instruction words are written to the 8K PRU memory of PRU_1 at address 0x0000 and 0x0001. If the command is a read command then the data read back is stored at address 0x0002.

8K PRU 1 Memory		**Address**
D31…….D16	**D15…….D0**	
	Data read back from IP or 8800	0x0002
	Data 15..0 for memory write	0x0001
Address(22..7) or Data(15..0)	Adrs(6..1)and command bits	0x0000

4. Instruction Word Makeup

Write to 8800 register or IP Registers
For write to 8800 register or IP registers a 32 bit instruction word is used:
Operation Word =((D15… D0<<16)+((A6_A1<<2|(Slot))<<8)+ CntlByte;

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A6	A5	A4	A3	A2	A1	S1	S0	C7	C6	C5	C4	C3	C2	C1	C0

Reading to 8800 register or IP registers
For reading to 8800 register or IP registers a 16 bit instruction word is used:
Operation Word = ((A6_A1<<2|(Slot))<<8)+ CntlByte;

x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	A6	A5	A4	A3	A2	A1	S1	S0	C7	C6	C5	C4	C3	C2	C1	C0

Write to IP memory
For write to IP memory consist of one 32 bit operation word and one 16bit data word:
Operation Word =((A22..A7<<16)+((A6_A1<<2|(Slot))<<8)+ CntlByte;
Data word = (D15… D0)

x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	S1	S0	C7	C6	C5	C4	C3	C2	C1	C0

Read IP Memory
For read IP memory consist of one 32 bit operation word:
Operation Word =((A22..A7<<16)+((A6_A1<<2|(Slot))<<8)+ CntlByte;

A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	S1	S0	C7	C6	C5	C4	C3	C2	C1	C0

4.1 Control and Status Byte (CntlByte)

This byte is written to the 8K memory of Pru 1.
The control and status byte consists of the following:

D07	D06	D05	D04	D03	D02	D01	D00
Enable Flag	Err	R/W	IOC8800 RegSel	IP IntSel	IP MemSel	IP IOSel	IP IDSel

Enable Flag: This tell the IOC8800 that a new operation is ready to be carried out. This bit is automatically cleared by the IOC8800 and tell the BBB that the operation has been carried out.

Err: Read Only bit. If an IP instruction failed to give Ack (8800 unit timed out doing IP op) set to ‘1’.

R/W: Set read =’1’ or write=’0’ for IP or 8800 ops

RegSel: This selects the IOC8800 registers

IDSel: This selects IP ID ROM
The IP ID ROM can be read by writing 0xA1 to the CntlByte. The address bits A6- A1 selects the address read from the ID ROM and Slot selects which IP card is targeted:

- Slot=0 IP card A
- Slot=1 IP card B

Read Operation Word = ((A6_A1<<2|(Slot))<<8)+ CntlByte;

IOSel: This selects IP registers.
The IP registers can be read by writing 0xA2 to the CntlByte. The address bits A6- A1 selects which IP register is read and Slot selects which IP card is targeted:

- Slot=0 IP card A
- Slot=1 IP card B

Read Operation Word = ((A6_A1<<2|(Slot))<<8)+ CntlByte;
Write Operation Word =((D15… D0<<16)+((A6_A1<<2|(Slot))<<8)+ CntlByte;

MemSel: This selects IP memory
The IP memory can be read by writing 0xA4 to the CntlByte. The address bits A22- A1 selects which IP register is read and Slot selects which IP card is targeted:

- Slot=0 IP card A
- Slot=1 IP card B

Operation Word =((A22..A7<<16)+((A6_A1<<2|(Slot))<<8)+ CntlByte;

IntSel: This selects the IP interrupt Vector registers to be read
The IP Interrupt Vector can be read by writing 0xA8 to the CntlByte. The address bit A1 selects which the interrupt vector is read:

- A1=0 Interrupt Vector for IntReq0
- A1=1 Interrupt Vector for IntReq1

Slot selects which IP card is targeted:

- Slot=0 IP card A
- Slot=1 IP card B

Read Operation Word = ((A6_A1<<2|(Slot))<<8)+ CntlByte;

4.2 Low Address And Unit Select Byte

D07	D06	D05	D04	D03	D02	D01	D00
A6	A5	A4	A3	A2	A1	Slot(1)	Slot(0)

Slot(1,0): Slot=00 = IP ‘A’ Slot=01 = IP ‘B’ If RegSel=’1’ then Slot=00 =8800 regs or Slot=01 = 8800 ID Rom

A6..A1: Address used for IP IO locations and ID also for 8800 registers and ID. These lines also form the lower 6 lines in the IP memory address.

4.3 Code Examples

Some example code (adc_ip.c) can be found in root/home/ioc8800.