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VTR2537
1M SAMPLES PER CHANNEL
OCTAL 12bit 50MHZ TRANSIENT RECORDER

USERS MANUAL

For Issue 2 PCB with Xilinx Firmware Version 2537mV201 & 2537sV201

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CONTENTS

1. INTRODUCTION

The VTR 2537 Transient Recorder is a dual height single width VME64 module which digitises the voltage signals present on eight inputs with a resolution of 12 bits and records all 8 channels simultaneously in its on-board SRAM which accepts up to 1M samples per channel.
The memory is accessible from the VME bus when the module is not acquiring data. An interlock between its Busy and Memory Access control bits ensure that there is no conflict of access.
An interrupt is generated whenever the acquisition is stopped and interrupts enabled. Acquisition can be halted either by:
Software Stop command
hardware Stop
after a pre-set number of samples have been stored
when the memory is full.
The sample clock may be internally generated at programmed rates of 0.5, 1, 2, 5, 10, 25 or 50 MHz. The module can also accept an external clock (60MHz max) via a front panel two-pin connector. Different clock rates may be selected for pre or post-trigger.
The module accepts an External Trigger via a front panel Lemo connector.
Front panel LEDs indicate the status of Start/Arm, Stop/Busy, VME access and External Clock Enable conditions.
The module can be operated in a number of different modes by writing to on-board control registers. The basic modes of operation are:-

- Pre-triggered (PT) sampling where the memory is divided into two areas, the first is allocated to pre-trigger samples and the other to post-trigger samples. When the Pre-trigger mode is enabled, data is acquired into the pre-trigger circulating buffer. A change in state of the Trigger (either software or hardware generated) causes the current conversion address of the pre-trigger buffer to be latched in the Trigger Address register so that data can be re-constructed up to the point of trigger. Conversions are then stored in the upper half of the memory until it is full or for a preset number of samples. The Pre-trigger and post trigger clocks can be set to different speeds. **MS=0 PT=1 RM=0**

- Multiple segment mode (MS). Here the memory is divided into a number of pre/post trigger buffers with a minimum size of 2K per buffer. When the module is Armed conversions occur in the first pre-trigger circulating buffer. When triggered conversions are stored in the first post-trigger buffer until it is full. Data is then acquired into the next pre-trigger circulating buffer until triggered again whereupon conversions are then stored in the next post-trigger buffer. This continues until all segments are full or acquisition is stopped. At each trigger the trigger address is stored in a section of memory reserved for these addresses. Up to 256 trigger addresses may be recorded. **MS=1 PT=1 RM=0**

- Software driven Start/Stop mode. A software driven mode wherein acquisition is started and stopped by writing to a control register on the unit. If pre set number of samples register set then acquisition will be stopped when the required number of samples has been reached (the input signal must remain high during this time) **MS=0 PT=0 RM=X**

- Hardware Gate mode. Here the trigger input signal enables the acquisition when true and stops it when false. If pre set number of samples register set then acquisition will be stopped when the required number of samples has been reached (the input signal must remain high during this time) **MS=0 PT=0 RM=X**

- Ring buffer mode (RM). Here the acquisition cycles round the memory until a stop command is issued by software or via the trigger.

2. PRODUCT SPECIFICATIONS

2.1 Power Requirements

+5V @ 3.5A

2.2 Operating Temperature Range

0 to +45 deg Celsius ambient.

2.3 Mechanical

6U single width VME module with access to P1 and P2 connectors and VME64X capability.

2.4 Front Panel Indicators

'VME'	LED illuminates for a minimum of 100msecs whenever the module is accessed via the VME bus.
'START/ARM'	LED indicates that the module has Started in Stop/Start mode or is Armed and is acquiring data Pre-triggered or Multiple segment mode.
'STOP/BUSY'	LED indicates that the module Stopped in Stop/Start mode or that it has been triggered and is actively acquiring data in to post-trigger memory in Pre-triggered or Multiple segment mode.
'External'	LED illuminated when the external clock is enabled.

2.5 Signal Specifications

2.5.1 External Clock

Connector type: EPL 0S 302 Pin 1+, Pin 2-, Screen common.
Signal: Differential PECL with jumper selectable termination of 50 ohms.
Clocks ADC conversions on the rising edge and latches the data on the trailing edge.
60MHz max rate.

2.5.2 Trigger

Connector type: RP-00-250 Single pole Lemo socket
Signal: Hardware Trigger Jumper selectable TTL or ECL (see appendix A).

2.5.3 Analogue Inputs 1- 8

Connector type: EPL 0S 302 Pin 1+, Pin 2-, Screen common.
Signal: Differential +/- with screen (capacitively AC coupled to chassis ground)
Span: +/-1V, bipolar as determined by PCB jumpers.

	+/-0.5V, bipolar as determined by PCB jumpers.
CMRR:	70db @ +/-1V CM
CMV:	+/-6V
Input impedance	100K/100R jumper selectable.
ADC resolution:	12 bits.
Diff. non-linearity:	+/-1 LSB at 12 bits typical. 12 bits no missing codes.
Int. non-linearity:	+/-1.5 LSB at 12 bits typical.
Offset error:	+/-0.5 LSB at 12 bits.
Gain Error:	+/-0.3%FS at 25 deg C
Gain Drift:	+/-26ppm per deg C
Offset Drift:	+/-2ppm per deg C
Bandwidth (ADC):	120MHz
Transient response:	15nS to 0.1% typical for 2V step
SNR:	65dB at 30MHz typical.
SINAD:	65dB at 30MHz typical.
ADC aperture delay:	2nS typical.
ADC aperture jitter:	8pS typical.

3. Signal Gain and Offset

Signal Gain and offset can be adjusted using trim pots 'VR1 OF' (offset) and 'VR2 GN' (gain setting). These have been factory pre-set for the +/-1V bipolar input range running at 10MHz and may need adjustment when other settings are used.

4. Internal and External Sample Clocks

The unit can be set to use either an internal or external sample clock. The selection of the external or internal clocking and the internal clock rates are set by writing to the Control register of the unit.
The external clock signal is PECL and can have a maximum frequency of up to 60MHz .

IMPORTANT NOTE: The unit uses a Delay-Locked Loop (DLL) and for reliably operation the input clock must have a frequency drift of no more than 1ns and a cycle to cycle jitter of less than 300ps.
If the frequency is changed or lock is lost (bit 3 CSR) than a reset on the DLL must be issued. This is achieved by doing a VME write to address Base+02 (all data bits are don't care).

5. Interrupt Settings

The interrupt generated by the unit is set using on board jumpers J12 to J18 see **appendix A** for settings.
The interrupt priority is set using jumpers J9 to J11 see appendix A for settings.

6. Trigger Input

The trigger input is used to trigger sampling in all modes. The trigger input circuitry can be set to operate with various inputs using jumpers JJ1 to JJ9 see **appendix A** for settings.

The trigger must be asserted for a minimum of half a clock cycle of the sample clock.

7. Use of the VME data bus and Memory Access

7.1 Base Address

The module uses A16/D16/D8 (EO) (Even and Odd byte) for accesses to the configuration registers. The base address of the configuration registers is determined by rotary selector switches SW1 and SW2 settings.

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	SW2	SW2	SW2	SW2	SW1	SW1	SW1	SW1	0	CA	CA	CA	CA	0

Addresses are in the range C000 - FFDE
A06 - A13 is the module address determined by the setting of the rotary selector switches SW1 and SW2.
A00 - A04 is the particular configuration register address (e.g. C000 is ID).

7.2 Memory Access

The units base address is stored as an offset in the Memory Offset register and for the 1M sample per channel unit the address lines A24 to A31 can be used as a memory offset. The unit also supports 32 bit VME block transfer mode BLT for memory access.
Memory data may be accessed as bytes, words or longwords using A32/D32/D16/D8 (EO).
Words and bytes are accessed via D15-D00. A1 addresses the low order word of a longword, A0 the high order word (big endian), thus A0 accesses the first conversion, A1 the second, and so on.
Conversions for each ADC are word ordered from 0 to 1M as shown: -
Memory top = Base + 8M words

D31 D16	D15 D00
ADC8 1st to (1M -1)th conversions 512Kx16	ADC8 2nd to 1M th conversions 512Kx16
ADC7 1st to (1M -1)th conversions 512Kx16	ADC7 2nd to 1M th conversions 512Kx16
ADC6 1st to (1M -1)th conversions 512Kx16	ADC6 2nd to 1M th conversions 512Kx16
ADC5 1st to (1M -1)th conversions 512Kx16	ADC5 2nd to 1M th conversions 512Kx16
ADC4 1st to (1M -1)th conversions 512Kx16	ADC4 2nd to 1M th conversions 512Kx16
ADC3 1st to (1M -1)th conversions 512Kx16	ADC3 2nd to 1M th conversions 512Kx16
ADC2 1st to (1M -1)th conversions 512Kx16	ADC2 2nd to 1M th conversions 512Kx16
ADC1 1st to (1M -1)th conversions 512Kx16	ADC1 2nd to 1Mth conversions 512Kx16

Memory base = Value in Memory Offset Register.

7.3 Memory Data

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0	0	0	O/R	AD 11	AD 10	AD 09	AD 08	AD 07	AD 06	AD 05	AD 04	AD 03	AD 02	AD 01	AD 00

2^{nd} conversion

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	O/R	AD 11	AD10	AD 09	AD 08	AD 07	AD 06	AD 05	AD 04	AD 03	AD 02	AD 01	AD 00

1st conversion

ADxx denotes ADC conversion data bit.
O/R denotes out of range bit.

When the ADC input drop below the lower threshold the O/R bit is set giving a digital output of 1000hex. When the ADC exceeds the upper threshold value the O/R bit is set giving a digital output of 1FFFFhex.

7.4 Address Modifiers

Configuration Registers: AM29 or 2D (short non-privileged or supervisory)
Memory: AM09 or 0D (extended non-priv. or supervisory)
BTL: AM0B or 0F (extended non-priv. or supervisory)

8. Firmware Registers

8.1 Manufacture ID (Read)

Address: Base + 00
Value = 8063 (0x1F7F)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1

8.2 Device Type (Read)

Address: Base + 02
Value = 12537 (0x30F9)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	1	0	0	1	1	1	1	0	1	0	0	1

8.3 External Clock DLL Reset (Write)

Address: Base + 02

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Writing to this register will reset the external clock DLL. This should be done when ever the external clock input is changed.

8.4 Control & Status Register (CSR)

Control (Write)
Address: Base + 04

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A32	T5	T4	T3	T2	T1	T0	ARM	I.E.	F	MS	C	SP	ST	PT	Rst

Status (Read)
Address: Base + 04

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A32	T5	T4	T3	T2	T1	T0	ARM	I.E.	F	MS	C	SP	LK	PT	SP/Bsy

A32 Enables acquisition memory access from VME when set to a 1 and disables ADC data acquisition. When set to zero can read trigger address memory.

T5-T3 Set the clock rate for Start/stop mode and High sample clock for Pre trigger or Multiple segment mode sampling.

	Control register bit setting for High clock rate		
Clock Setting	T5 (bit D14)	T4 (bit D13)	T3 (bit D12)
External Clock	0	0	0
0.5MHz	0	0	1
1MHz	0	1	0
2MHz	0	1	1
5MHz	1	0	0
10MHz	1	0	1
25MHz	1	1	0
50MHz	1	1	1

T2-T0 Set the Low clock rate sample frequency for Pre trigger or Multiple segment mode sampling. In triggered Start/stop mode this should be set to zero.

	Control register bit setting for Low clock rate		
Clock Setting Low CLK OFF	T2 (bit D11) 0	T1 (bit D10) 0	T0 (bit D9) 0
0.5MHz	0	0	1
1MHz	0	1	0
2MHz	0	1	1
5MHz	1	0	0
10MHz	1	0	1
25MHz	1	1	0
Ext Clk div 2	1	1	1

ARM Start acquisition in the pre-trigger mode. (This inhibits A32 from being set to disables VME acquisition memory accesses).
In Start/stop mode this arms the module and allows the trigger to start and stop the module.

IE Interrupt Enable - An IRQ is generated if Stop is set. The IRQ number is determined by PCB jumper settings J12 to J18 see appendix A.

F Full flag - Set when the memory has been completely filled.

MS Multi-segment Mode. Multiple pre/post triggered acquisitions can be performed according to the segment size as set in the segment size register at Base + 16h.

RB Ring Buffer mode when set to 1 STOP will not be set on FULL. The acquisition will continue with the address counter wrapping around.

SP Stops acquisition. SP is set by: memory full, triggered stop, or pre-set count Stop.

ST Writing a '1' Start data acquisition , writing a '0'stops data acquisition. This is a write only bit.

LK Shows if the clock is locked (if clock is not locked the data maybe inaccurate).

PT **1 =** Enables Pre/post-trigger acquisition.
0 = Enables Hardware/Software Triggered Start/Stop mode.

SP/Bsy In Pre/post-trigger mode (PT=1) set when the module has been triggered (drives front panel BUSY LED).
In Start/stop trigger mode (PT=0) set whenever the module is Stopped (drives front panel STOP LED).

Rst Clears status register to zero write only.

8.5 Memory Offset (Read/Write)

Address: Base + 06

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A31	A30	A29	A28	A27	A26	A25	A24	X	X	X	X	X	X	X	X

8.6 Conversion Address or Sample Counter (LS) (Read)

Address: Base + 08

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M15	M14	M13	M12	M11	M10	M09	M08	M07	M06	M05	M04	M03	M02	M01	M00

Conversion Address or Sample Counter (MS) (Read)

Address: Base + 0

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	0	0	0	0	0	M18	M17	M16

The conversion address registers gives the acquisition address in a 16bit format, which is also the number of logged samples.

8.7 Interrupt Vector (Read/Write)

Address: Read = Base + 0C, Write = Base + 00

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V09	V08	V07	V06	V05	V04	V03	V02	V01	V00

8.8 Pre-set Count Register (LS) (Read/Write)

Address: Base + 12

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00

Pre-set Count Register (MS) (Read/Write)

Address: Base + 14

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	0	0	0	0	P19	P18	P17	P16

The value written to this register will give the number of samples that will be taken before the Stop bit of the CSR is set to one.

This is implemented using a down counter and includes zero also the samples are written in pairs so only even counts are valid.

i.e. to set pre count to give 800h (2048dec) sample load 1FF in to preset counter.

7.8 Segment size (Read/Write)

Address: Base + 16

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
x	x	x	X	x	x	x	512K	256K	128K	64K	32K	16K	8K	4K	2K

Defines the pre-trigger buffer size in Pre/post-trigger mode and the pre/post-trigger buffer size in Multi-segment mode. Restricted to binary multiples, e.g. 4 (D02=1) sets pre-trigger and post-trigger buffer sizes to 8K.

7.9 Number of Trigger Address (Read Only)

Address: Base + 18

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
x	x	x	x	x	x	x	x	TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0

This gives the number of times the unit has been trigger and has logged the triggered address. Only the first 8 bits used as the trigger address memory is only 256 words in size.
This register is cleared when the unit is Armed.

8.9 VME System Reset

A VME system reset will clear the following registers:

- Control Register
- Status Register
- Memory Offset Register
- Vector Register

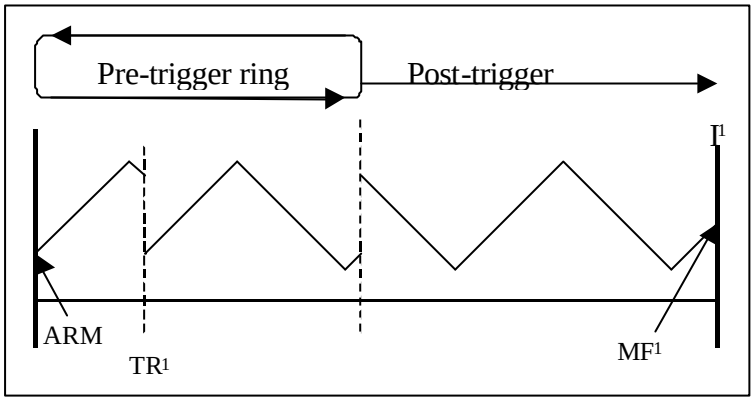
9. Trigger Address Memory (Read)

The data held in this part of the memory is the triggered address and is held in a 32 bit format.
Note: In Multi-segment mode the Trigger Addresses are stored sequetionaly from address 0 to 255 memory locations.

To access this part of the extended memory the A32 bit of the CSR needs to set to 0 then do an extended memory read (AM09 or 0D).

10. MODES OF OPERATION

10.1 Pre Trigger Mode



CSR has the following bits set PT=1 MS=0 RM=0
To start set ARM=1 in CSR

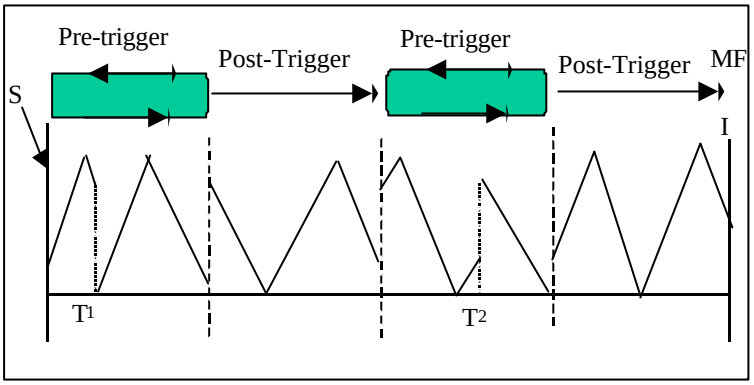
Pre/post-triggered sampling where the memory is divided between that allocated to pre-trigger samples set by the Segment Size register and the remainder to post-trigger samples.
When the Pre/post-trigger mode is enabled, data is acquired into the pre-trigger circulating buffer. A Trigger input (front panel or software) causes the BUSY led to be illuminated and the current conversion address of the pre-trigger buffer to be latched in the Trigger Address register so that data can be re-constructed up to the point of trigger. Conversions are then stored in the post-trigger memory until it is full or for a preset number of samples set by the Pre-set Count register.

The sampling can be halted at any time by writing to the Stop bit of the CSR. To continue first clear the Stop bit then set the Continue bit. This can be done in both the post-trigger and pre-trigger buffers.

Can also continue after the pre-trigger buffer has been filled if less than 512k as set by the Pre-count register. To continue set the continue bit of the CSR.

If LOW clock is set to anything other than T0, T1 and T2 set to zero then the pre-trigger buffer clock is set to clock at LOW clock sample rate, on triggering the sampling clock speed will be set to HIGH clock speed. This also applies when using external clocking if T0, T1 and T2 are set to all ‘1s’ the LOW clock will be set to half the external clock rate.

10.2 Multiple Segmented Mode

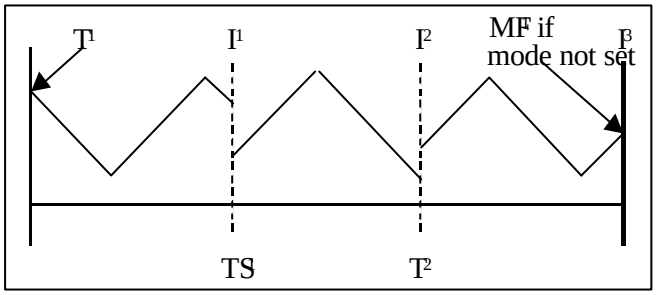


CSR has the following bits set PT=1 MS=1 RM=0
To start set ARM=1 in CSR

Here the memory is divided into a number of pre/post trigger buffers with a minimum size of 2K per buffer. When the module is Armed conversions occur in the first pre-trigger circulating buffer. When triggered (front panel or software) the BUSY led is illuminated and conversions are stored in the first post-trigger buffer until it is full.
Data is then acquired into the next pre-trigger circulating buffer until triggered again whereupon conversions are then stored in the next post-trigger buffer. This continues until all segments are full or acquisition is stopped. At each trigger the trigger address is stored in a section of memory reserved for these addresses. Up to 256 trigger addresses per channel may be recorded.
If LOW clock is set to anything other than T0, T1 and T2 set to zero then the pre-trigger buffer clock is set to clock at LOW clock sample rate, on triggering the sampling clock speed will be set to HIGH clock speed. This also applies when using external clocking if T0, T1 and T2 are set to all '1s' the LOW clock will be set to half the external clock rate.

Note
Preset number of samples set by the Pre-set Count register will be ignored in this mode.

10.3 HardwareTriggered START STOP



T^x = Triggered Start

TS^x =Triggered Stop

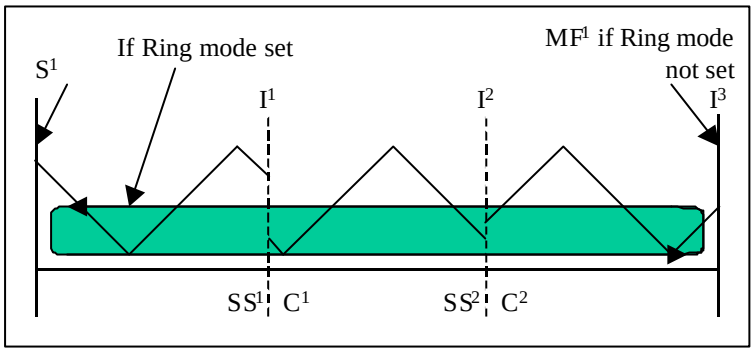
MF^x = Memory full Stop set if RM not

I^x = Interrupt generated if RM not

PT=0 ARM=1 MS=0 RM=X

This can be used with or without Ring Buffer mode set.
When a '1' is written to ARM the address/sample counter is zeroed and the STOP led is illuminated. Trigger going high start acquisition and illuminates the START Led on front panel, taking the trigger low stops the unit acquiring illuminated the STOP led and latches the conversion address in to the Triggered address space. This is the first location in triggered memory space.
In the Stopped condition the memory can be read (once A32 of CSR is set to 1). The acquisitions can then be restarted by taking the Trigger high.
The above sequence can be repeated indefinitely if the ring buffer mode is set. If ring buffer mode is not set, the unit will stop when the memory is full.
If the preset count register is set then the acquisition of data will stop when the number of counts has been reached. During this period the trigger input must stay high otherwise the acquisition of data will stop before the number of counts has been reached.

10.4 Software START, STOP and Continue



PT=0 MS=0 ARM=1 RM=X

This can be used with or without Ring Buffer mode set.
When a '1' is written to ARM the address/sample counter is zeroed and the STOP led is illuminated.
Writing a one to D02 (ST) of the Control register starts data acquisition and illuminates the START Led on front panel, writing a zero to D02 (ST) of the Control stops the unit acquiring and illuminats the STOP led and latches the conversion address in to the Triggered address space. This is the first location in triggered memory space.
In the Stopped condition the memory can be read (once A32 of CSR is set to 1). The acquisitions can then be restarted by writing a one to D02 (ST) of the Control register.
The above sequence can be repeated indefinitely if the ring buffer mode is set. If ring buffer mode is not set, the unit will stop when the memory is full.
If the preset count register is set then the acquisition of data will stop when the number of counts has been reached. During this period the D02 (ST) of the Control register must stay a one otherwise the acquisition of data will stop before the number of counts has been reached.

APPENDIX A

PCB JUMPER and SWITCH SETTINGS

Clock
POS ECL
Single ended J5 Make 1:2 J6 Make 2:3
Differential J5 Make 2:3 J6 Make 1:2

J7 Made puts 50ohm termination on clock input.

VME Short IO Base Address
SW1 and SW2 sets VME SHORT IO base address
SW1 sets address Lines A13 to A10
SW2 sets address Lines A9 to A6

SW1 = 0x0 and SW2 = 0x0 gives a Base address of 0xC000
to
SW1 = 0xF and SW2 = 0xF gives a Base address of 0xFFC0

Interrupts
J9-J11 Priority Make according to required interrupt priority.

Int Priority Level	J9	J10	J11
1	Made	Made	Open
2	Made	Open	Made
3	Made	Open	Open
4	Open	Made	Made
5	Open	Made	Open
6	Open	Open	Made
7	Open	Open	Open

J12 to J18 sets interrupt level.
J12 IRQ1 Make to generate IRQ1*
J13 IRQ2 Make to generate IRQ2*
J14 IRQ3 Make to generate IRQ3*
J15 IRQ4 Make to generate IRQ4*
J16 IRQ5 Make to generate IRQ5*
J17 IRQ6 Make to generate IRQ6*
J18 IRQ7 Make to generate IRQ7*

FPGA Boot

J8 Master Made when Master FPGA (IC50) SPROM installed.
J35 Slave Made when Slave FPGA (IC51) SPROM installed.

Input Terminations
J10 (I/Ps1-8) Term When made 100R is connected across the respective input.

Grounds
LK1 GND to AGND When made connects Analogue Ground to Digital Ground do not remove this link as component damage may result .
LK2 AGND to CGND When made connects Analogue Ground to Chassis Ground.
LK3 GND to CGND When made connects Digital Ground to Chassis Ground.
NB LK2 and LK3 both made connects AGND to GND

Ranges
J3 (I/P chan1 to chan8) Factory set (Must be left open for correct operation).
J4 (I/P chan1 to chan8) Make 1:2 for +/-0.5V input voltage. Make 2:3 for +/-1V input voltage.

Trigger Operation

	JJ1	JJ2	JJ3	JJ4	JJ5	JJ6	JJ7	JJ8	JJ9
ECL-SINGLE ENDED			X		X		X		X
TTL – PULL DOWN TERMINATED		X			X	X			X
TTL – PULL UP TERMINATED	X				X	X			X
TTL – PULL DOWN/UP	X	X			X	X		X	
ECL - DIFFERENTIAL				X					X
AS ABOVE BUT NEGATIVE I/P								X	

J20 to J34 are note used.

Denotes Factory Settings